No. 24-2304

IN THE

United States Court of Appeals

FOR THE FEDERAL CIRCUIT

NETLIST, INC.,

Appellant,

v.

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC,

Appellees.

On Appeal from the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, Nos. IPR2022-00615, IPR2023-00203

OPENING BRIEF FOR APPELLANT NETLIST, INC.

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PATENT CLAIM AT ISSUE

U.S. Patent No. 7,619,912, Claim 16

[pre] A memory module connectable to a computer system, the memory module comprising:

[a] a printed circuit board;

[b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

[c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, [c.i] the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, [c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, [c.iii] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, [c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

[d] a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

[e] wherein the command signal is transmitted to only one DDR memory device at a time.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 2024-2304

Short Case Caption Netlist, Inc. v. Samsung Electronics Co., Ltd.

Filing Party/Entity Netlist, Inc.

Instructions:

1. Complete each section of the form and select none or N/A if appropriate.
2. Please enter only one item per box; attach additional pages as needed, and check the box to indicate such pages are attached.
3. In answering Sections 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance.
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Date: 02/18/2025

Signature: /s/ Jeffrey A. Lamken

Name: Jeffrey A. Lamken

1. Represented Entities. Fed. Cir. R. 47.4(a)(1).	**2. Real Party in Interest.** Fed. Cir. R. 47.4(a)(2).	**3. Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3).
Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities. ☑ None/Not Applicable	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities. ☑ None/Not Applicable
Netlist, Inc.		

☐ Additional pages attached

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

☑ None/Not Applicable ☐ Additional pages attached

Irell & Manella LLP	Hong Annita Zhong	Jason G. Sheasby
Jonathan M. Lindsay	Phillip Warrick	Michael W. Tezyan
Michael Fleming		

5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

☑ Yes (file separate notice; see below) ☐ No ☐ N/A (amicus/movant)

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). **Please do not duplicate information.** This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

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☑ None/Not Applicable ☐ Additional pages attached

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STATEMENT OF RELATED CASES

No appeal in or from this proceeding was previously before this or any other appellate court. The following cases may directly affect or be directly affected by this Court's decision in this case: *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2:22-cv-00293 (E.D. Tex.); *Netlist, Inc. v. Micron Technology Texas, LLC*, No. 2:22-cv-00294 (E.D. Tex.); *Netlist, Inc. v. Google LLC*, No. 3:09-cv-05718 (N.D. Cal.). In addition, on January 21, 2025, this Court ordered that this appeal and the following appeals be treated as companion cases and assigned to the same merits panel: Nos. 25-1286 (lead), 25-1296 (member). ECF No. 22.

INTRODUCTION

Claim 16 of Netlist's '912 patent has been subjected to three exhaustive inter partes reexaminations: one sought by Google, another by Smart Modular, and a third by Inphi. It survived sprawling PTO proceedings spanning 10 years that involved myriad unpatentability grounds; five office actions; more than twenty briefs; two appeals to the PTAB; and an appeal to this Court. It survived because the Examiner and the Board adopted—and Netlist accepted—a construction of a key term to require that claimed "ranks" contain ***two or more*** memory devices. That construction reflected industry standards, which required ranks to contain multiple devices.

But when this IPR petition was filed by Google's supplier, Samsung, the Board reversed course below and found the claim unpatentable. It did not identify new art. It changed its construction so the claimed ranks can contain only ***a single*** memory device—a construction ***diametrically opposed*** to the construction the Board applied in the reexamination. That about-face is troubling as a matter of agency consistency. But it is also improper as a matter of patent law. The consensus in the reexamination about the meaning of "rank" in claim 16—among the Examiner, Netlist, and the Board there—is powerful prosecution-history intrinsic evidence skilled artisans would rely on to understand that term. The Board in this IPR never suggested otherwise. And the Board was required to "exclude any interpretation that was disclaimed during prosecution." *Arendi S.A.R.L. v. Google LLC*, 882 F.3d 1132,

1135 (Fed. Cir. 2018). But the Board did the opposite—departing from the claim's text, the specification, and industry standards in the process.

Worse, the sole reference on which the Board relied—Ellsberry—does not teach claim 16's subject matter even under the Board's new construction. And Ellsberry was not even prior art to claim 16. The '912 patent claims priority to ***two*** filings—Netlist's '436 patent and '244 provisional—that antedate Ellsberry. The Board declared that neither filing provides written-description support for claim 16. But the "register" the '436 patent supposedly does not disclose was conventional already—and the '436 patent disclosed it by reciting "sequential logic," which undisputedly requires "a register" or its "equivalent." The Board's analysis of the '244 provisional is even more flawed. Post-grant review procedures serve an important purpose in our patent system. But they were not designed as vehicles for relitigating issues until a different PTAB panel reaches a different result.

JURISDICTIONAL STATEMENT

The Board had jurisdiction under 35 U.S.C. §§6, 318(a). It issued a final written decision on April 17, 2024. Appx1-56. Director review was denied on July 10, 2024. Appx57-59. Netlist appealed on September 10, 2024. Appx109. This Court has jurisdiction under 28 U.S.C. § 1295(a)(4)(A) and 35 U.S.C. §§ 141(c), 319.

ISSUES PRESENTED

In this IPR, the Board ruled that claim 16 is obvious in light of the Ellsberry reference. The Board previously upheld the same claim in three earlier inter partes reexaminations, and this Court affirmed. The issues presented are:

1. Whether the Board's construction of claim 16 was erroneous, where it contradicts the construction the Board adopted in finding the same claim patentable during prior reexaminations.

2. Whether the Board's obviousness determination was unsupported by substantial evidence.

3. Whether the Board's determination that Ellsberry is prior art is erroneous, where the '912 patent claims priority to two filings that antedate Ellsberry and provide written-description support for claim 16.

STATEMENT OF THE CASE

This appeal concerns Netlist's patented technology for increasing the capacity and speed of memory modules while reducing power usage. For its inventions, Netlist received U.S. Patent No. 7,619,912 ("the '912 patent") in 2009. The patent then spent a decade in reexamination proceedings in which the Examiner and the Board repeatedly affirmed claim 16's patentability. This Court affirmed. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020). In this IPR, however, the Board invalidated claim 16 over Ellsberry—a reference considered during initial

examination—by adopting a claim construction diametrically opposed to the one it adopted during reexamination.

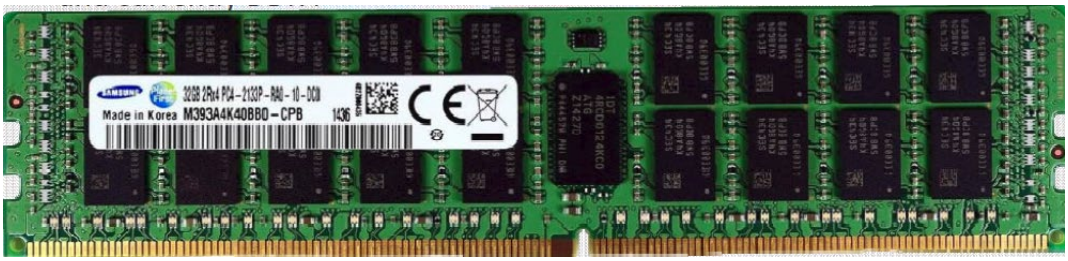
I. TECHNOLOGICAL BACKGROUND

Computers need increasingly more memory to support sophisticated applications such as artificial intelligence. Appx19694. Increasing the number of memory modules—circuit boards with memory chips—quickly ceased to be an option. Appx11604. Computers have a limited number of slots into which memory modules may be installed. Appx96(32:29-31). To increase the memory that could be installed into each computer, manufacturers needed to increase the capacity of each memory module. Appx96(32:29-31).

Restrictions imposed by industry standards, and the cost of higher-capacity memory devices, significantly limited manufacturers' ability to do so. Appx11664; Appx81(2:39-41). But Netlist's '912 patent provided a new approach—"rank multiplication" with individually addressable memory devices—for expanding the capacity of standards-conforming memory modules while reducing cost, increasing speed, and reducing power usage. Appx81(2:16-23, 2:39-40); Appx86(12:39-43); Appx83(5:1-5).

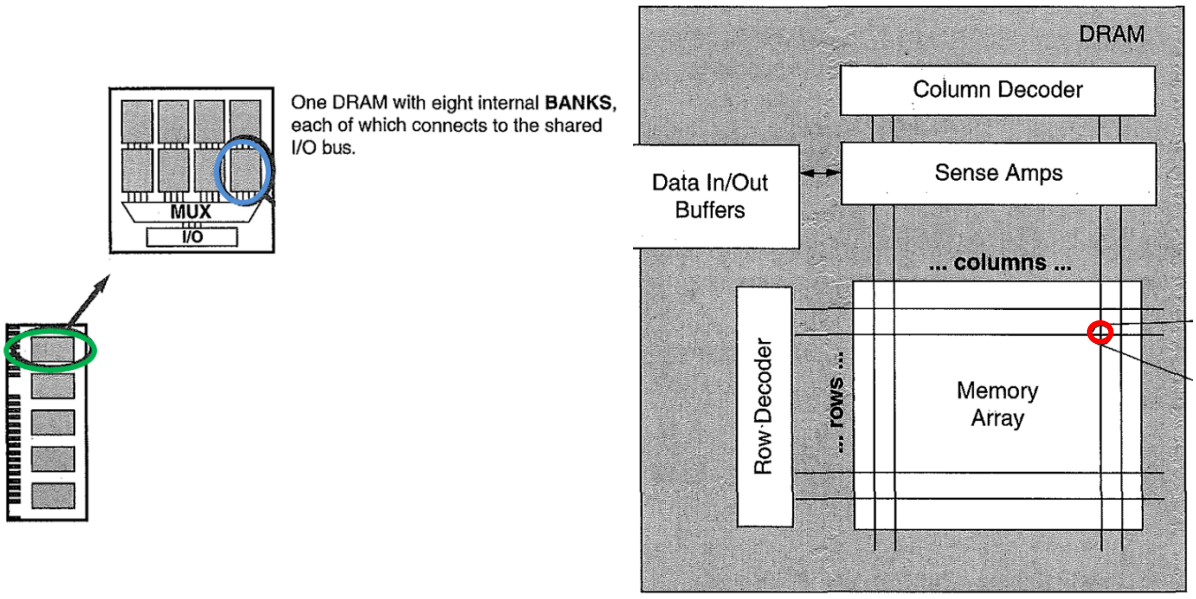
A. Memory Modules and DRAM

Memory modules store data in dynamic random-access memory ("DRAM") chips. Appx81(1:25-36). A memory module includes a circuit board (green) with individual DRAM chips (black rectangles) attached. Appx81(1:25-27).



Appx20251. The gold edge connector on the bottom of the module plugs into a slot on the computer's motherboard, making the memory on the module available to the computer. Appx83(6:4-11); Appx20250.

As shown below, on the left, a DRAM chip (green) includes a plurality of memory "banks" (blue). Appx11608. As shown on the right, each memory bank includes "memory array[s]" consisting of a grid of storage cells (*e.g.*, red circle) arranged in "rows" and "columns." Appx11606; Appx11608.



Appx11608; Appx11606 (annotated). When the CPU's "memory controller" stores data to (writes) or retrieves data from (reads) a storage cell, it locates the desired cell by specifying its "address" in terms of a "bank address," "row address," and "column address." Appx11606-08; Appx11699.

B. Industry Standards and Cost Limit Memory-Module Capacity

The capacity of a memory module—the amount of data it can store—depends on the capacity of each DRAM chip and the number of DRAM chips on the module. Appx81(2:24-25). Capacity can be increased by either increasing the ***capacity of each DRAM chip***, or increasing the ***number*** of DRAM chips.

Cost posed a barrier to increasing individual chip capacity. Higher-capacity DRAM chips are generally more expensive per unit of capacity than lower-capacity chips. Appx83(5:1-5). For example, two 256-Mb DRAM devices together may cost less than one 512-Mb device, even though two 256-Mb devices together have 512

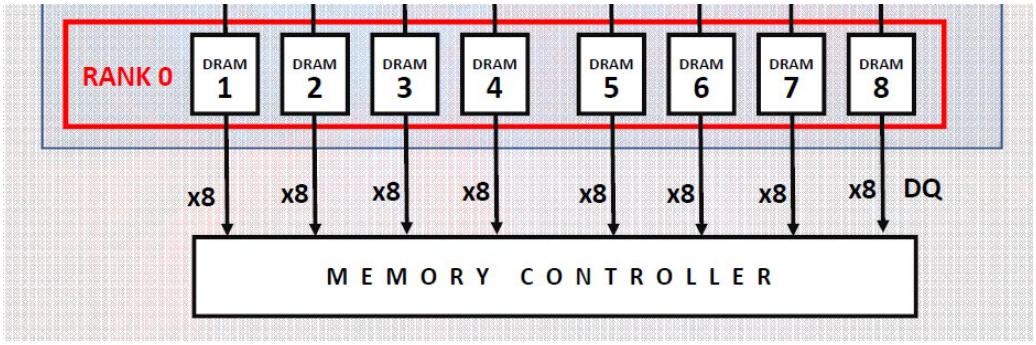
Mb of capacity. Appx82-83 (4:47-5:5). To increase capacity using available, cost-effective DRAM chips, memory-module makers sought ways to increase the number of DRAM chips on each memory module. Appx83 (5:1-5).

Industry standards, however, were a barrier to increasing the number of DRAM chips on each module. To ensure interoperability, the industry group JEDEC sets standards for DRAM memory modules. Appx11709. The "vast majority" of DRAM memory modules follow "JEDEC specifications." Appx18284 (¶19). The relevant JEDEC standard—"DDR" ("Double Data Rate")—limits the number of memory chips on each module in two ways. Appx20259-344.

First, the CPU's memory controller reads/writes a set number of bits at a time in parallel. Appx11809. The ***memory module*** must read/write that number of bits—known as the module's "bit width"—simultaneously. Appx11809. Relevant JEDEC "DDR" standards specify modules of "64" or "72" bits. Appx12184; Appx11699 & n.1; Appx18460 (¶255). Memory modules that did not comply with those standard bit widths would not function correctly. Appx11699-700.

Individual ***DRAM chips*** also must read/write a set number of bits in parallel—4, 8, or 16 bits at a time under the JEDEC DDR standard. Appx86 (12:39-55); Appx11267-70. Thus, multiple DRAM chips must work in concert to produce the 64- or 72-bit width the DDR standard requires. Appx11703. To achieve that, DRAM chips on each memory module are organized into "ranks," where each rank

consists of multiple chips operating together to read/write the required number of bits at a time. Appx11703-04; Appx20253; *see* Appx19644. For example, to form a 64-bit-wide memory module, DRAM chips may be organized into ranks of 8 chips each, where each chip is 8 bits wide (8 × 8 = 64). Appx18455.



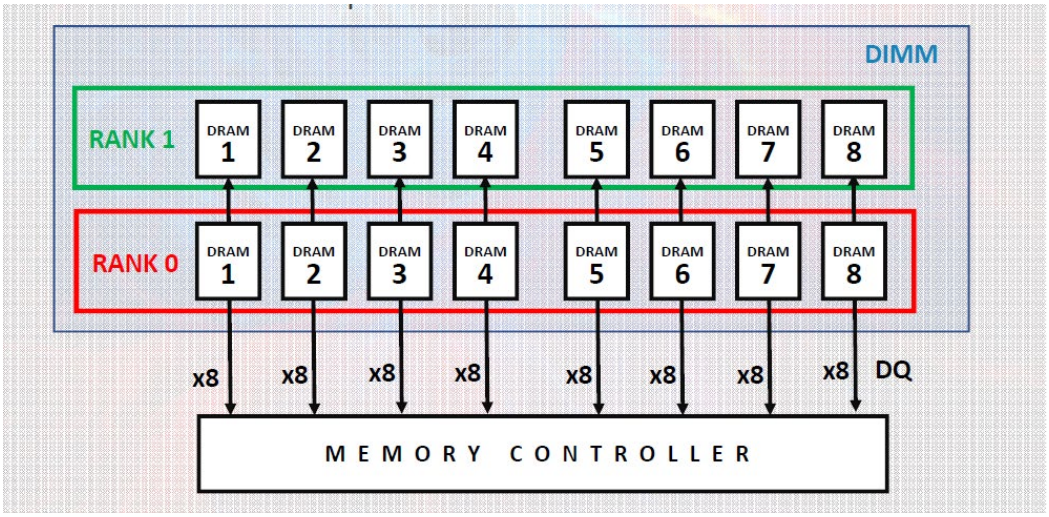
Appx20253 (cropped). Alternatively, the chips may be organized into ranks of 16 memory chips, where each chip is 4 bits wide (16 × 4 = 64). Appx18455.

As Petitioner Micron recognized, "[t]he term rank was created by JEDEC" to describe an arrangement of memory chips adding up to the "64 or 72 bits" required for the "module." Appx19644. The term "rank"—referring to a "line of soldiers ranged side by side," *Webster's New International Dictionary* 2061 (2d ed. 1934)—aptly described DRAM chips arranged side-by-side to provide the memory module's bit width, as shown above. Appx19644.

Second, the JEDEC DDR standards limited the number of ranks in each memory module. Appx81(2:39-40). Under the standard, the memory controller provided one or more "chip-select" signals that are used to distinguish between ranks in each memory module. Appx81(2:34-41). The number of chip-select signals

available under the standard typically limited each memory module to at most two ranks. Appx81(2:34-41).

Those requirements—memory-module bit-width and a maximum of two rank-select signals—limited the number of DRAM chips on, and thus the total capacity of, each module. The number of chips per rank was dictated by the required bit width of the memory module; and the number of ranks per memory module was limited by the number of chip-select signals. Appx11699 & n.1 (bit width); Appx84(7:23-27) (chip-select). For example, memory modules could be 64-bits wide and support up to two ranks. Appx11699 & n.1; Appx84(7:23-27). If available DRAM chips were 8 bits wide, each rank would have 8 chips (8 × 8 = 64), and each module would have 16 chips (2 ranks of 8 chips each). Appx18455.



Appx20253.

II. NETLIST INCREASES MEMORY CAPACITY BY ENABLING STANDARD MEMORY MODULES TO SUPPORT ADDITIONAL RANKS

A pioneer in memory technology, Netlist has developed, manufactured, and supplied cutting-edge memory products to companies including IBM, Dell, HP, and Apple.

Netlist devised a way to cost-effectively increase memory-module capacity—by increasing the number of ranks—while maintaining compatibility with JEDEC standards. Netlist's improved memory modules increased server memory capacity using more, cheaper, lower-capacity DRAM chips (instead of costly higher-capacity chips). That increased performance without requiring changes to existing memory controllers or motherboards. Netlist also invented a way for memory controllers to send commands to ***individual*** DRAM devices in a rank—in contrast to the prior art that broadcasted commands to ***all*** devices in the rank. That enabled sending individually tailored power-management and calibration commands to each DRAM chip to optimize that chip's performance and power usage.

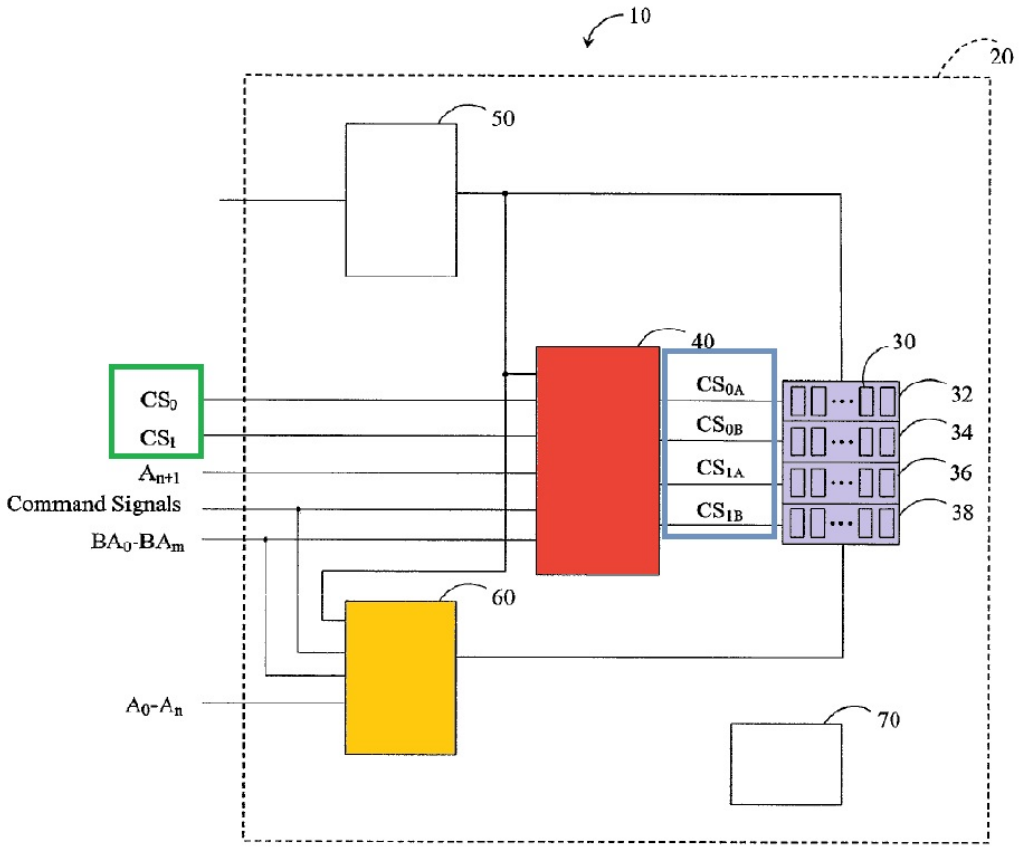
A. Netlist Invents a Technique for "Rank Multiplication" and Targeting Commands to a Single DRAM Chip

Netlist's patented invention overcame the barrier to greater numbers of ranks that industry standards had imposed. It allowed the memory module to have more ranks of lower-capacity chips (*e.g.*, four ranks of lower-capacity chips) while ***appearing*** to the CPU to have the smaller number of ranks of higher-capacity chips

the JEDEC DDR standard required (*e.g.*, two ranks of higher-capacity chips). Appx84(7:5-19); Appx96(32:27-49).

1. To achieve that result, Netlist engineers placed a logic circuit inside the memory module. That circuit intercepts chip-select and address signals intended to control the smaller number of ranks; it then creates additional signals to control the larger number of ranks actually present in the module. Appx83-84(6:55-7:6); Appx63(Fig. 1A). Memory-controller signals designed to control just two ranks of memory devices, for example, can be utilized to control four ranks.

Figure 1A of the '912 patent illustrates an embodiment of the invention:



Appx63 (Fig. 1A) (annotated). A memory module (10) has DRAM chips arranged in four ranks (32, 34, 36, and 38, purple). Appx83 (5:22-25; 6:31-35). The CPU's "memory controller" sends a set of control and address signals, including ***two*** chip-select signals (CS_0 and CS_1 in green box) to control ***two*** ranks. Appx84 (7:35-53); Appx86 (11:43-48). A "logic element" (40, red) receives those signals and generates ***four*** chip-select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} in blue box) for the ***four*** ranks located on the memory module. Appx86 (11:62-67). Meanwhile, a "register" (60, orange) receives and buffers address signals and sends them to "the appropriate ranks of memory devices." Appx84 (7:43-53). The logic element and register can be "separate components" or "portions of a single component." Appx83 (5:37-42).

2. Netlist also invented "per-DRAM addressability" ("PDA"). Conventionally, memory controllers broadcast commands—such as for configuring DRAM chips—simultaneously to ***all*** DRAM chips in a rank, which "operate[d] in lockstep." Appx11702. PDA enabled memory controllers to isolate "only one" DRAM chip in the rank at a time—out of the several in the rank—and send commands to that chip alone. Appx84 (8:50-54); Appx105 (7:20-24); *see* Appx18298-301 (¶¶40-43).

Per-DRAM addressability provided significant benefits. Appx19343. It saved power by allowing the memory controller to put "a single DRAM device" in a rank into a "maximum power-saving" mode. Appx19333. PDA also enabled memory controllers to tune key configuration parameters to individual DRAM

devices, maximizing each chip's speed and power usage. Micron Technology, Inc., *Technical Note: DDR4 Point-to-Point Design Guide* 1, 12-14 (2020), https://www.mouser.com/pdfDocs/Micron_DDR4_Design_Guide.pdf. PDA now is part of JEDEC's specifications. Appx16531-33; Appx19287.

B. The PTO Awards Netlist the '912 Patent

Netlist's '912 patent covers its rank-multiplication and per-DRAM addressability innovations.

Claim 16 is reproduced below:

[pre] A memory module connectable to a computer system, the memory module comprising:

[a] a printed circuit board;

[b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

[c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,

[c.i] ***the logic element receiving a set of input signals from the computer system***, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,

[c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,

[c.iii] ***the circuit generating a set of output signals in response to the set of input signals***, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,

[c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and ***transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks***; and

[d] a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

[e] wherein the command signal is transmitted ***to only one DDR memory device at a time***.

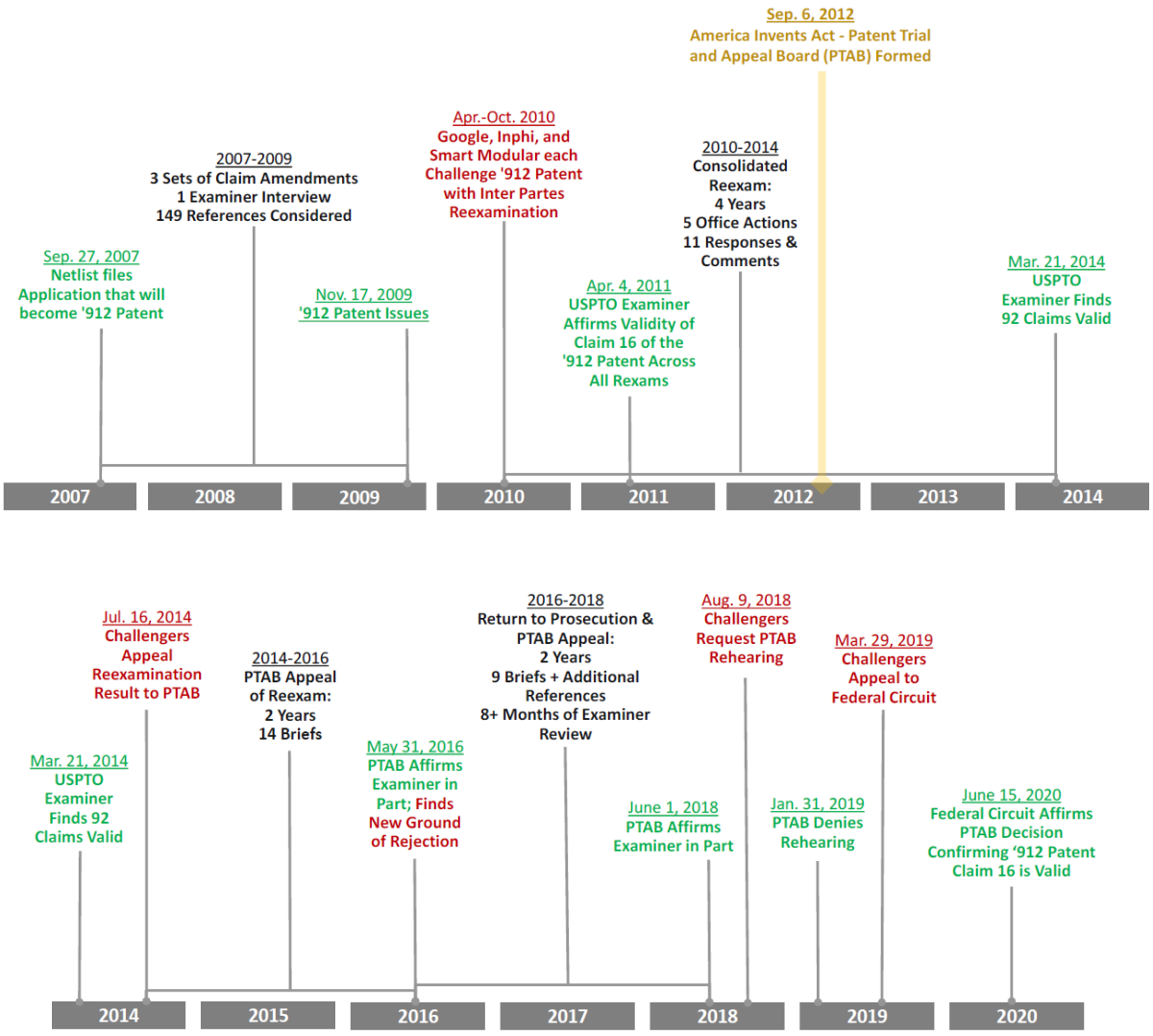
Appx103(3:9-43) (emphasis added). Limitation 1[c.i]-[c.iii] reflects rank multiplication, while limitations 1[c.iv] & 1[e] reflect per-DRAM addressability.

C. Claim 16 Survives Multiple Inter Partes Reexaminations and Is Restated to Its Current Form

Claim 16 has an extensive prosecution history. Originally, the preamble and limitations [a]-[d] were recited in independent claim 15. Appx10650-51. Claim 16 originally depended from claim 15 and further recited what is now claim 16's limitation [e]: "wherein the command signal is transmitted to only one DDR memory device at a time." Appx10651.

Shortly after the '912 patent issued, Google, Smart Modular Technologies, and Inphi each sought reexamination of the patent, including claims 15 and 16.

Appx10487. The reexamination ultimately consumed over ten years, including two appeals to the Board and an appeal to this Court:



Appx21244-45.

1. In the first round of reexamination, the Examiner found claim 15 unpatentable, but upheld claim 16. The Examiner rejected the argument that claim 16 was obvious in view of Amidi. "The claims," the Examiner explained, "require

transmission of a command signal to only one DDR memory device at a time"—*i.e.*, "only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Appx6375 (emphasis added). The claim thus was not disclosed by prior art where, as in Amidi, a command is "transmitted to ***all devices***" in a rank simultaneously. Appx6413 (emphasis added). Based on the Examiner's determination, Netlist amended the claims to restate claim 16 as an independent claim and cancel claim 15. New claim 16 incorporated the limitations of original independent claim 15 along with the limitations of original dependent claim 16 (with no other changes). Appx5615-16; Appx5652.

One requester argued that Amidi taught sending a signal to only one memory device at a time by teaching a "rank" that purportedly "encompasses" just "'***one memory device***.'" Appx6951-52 (emphasis added). When "only one rank is selected," it urged, "the command signal will be sent to only a single memory device"—the single device in the rank. Appx6952. The Examiner reiterated that Amidi did not teach what claim 16 required—"transmit[ting] a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Appx7337 (emphasis added).

2. The Board upheld the Examiner's decision. Claim 16, it held, "'require[s] transmission of a command signal to only one DDR memory device at a time'"—*i.e.*, "'***to only one DDR memory device at a time when there is a plurality***

of memory devices in a rank.'" Appx10561 (emphasis altered). Because Amidi taught that signals were transmitted to "***multiple*** memory devices at a time," it did not render claim 16 obvious. Appx10561. However, the Board remanded to the Examiner for consideration of new grounds as to certain claims. Appx9614; Appx10032. The Board denied rehearing on all the claims it had upheld. Appx10647.

3. The patent was then subjected to a ***second*** round of reexamination in the same proceeding. Appx9788-89. A second appeal to the Board followed, which found that the prior decision to uphold claim 16 "remains affirmed." Appx10251. The Board again denied rehearing. Appx10373-84.

Requesters appealed, challenging the Board's decision to uphold claim 16. *See* Inphi.Br.48-49 in *Google LLC v. Netlist, Inc.*, No. 19-1720 (Fed. Cir.). This Court affirmed without opinion. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

III. PROCEDURAL HISTORY

This is the fourth post-grant attempt to invalidate claim 16. After the prior attempts by Google and others failed, Samsung initiated this IPR. This time, the Board concluded claim 16 was obvious. The Board, however, pointed to no material difference in the asserted prior art—it relied on a reference the Examiner considered during initial examination. Instead, the Board adopted a new construction of claim

16 that contradicted the construction the Examiner and Board had adopted in upholding claim 16 during reexamination.

A. Samsung's Petition

Samsung's Petition invoked three putative prior-art references: Ellsberry, Amidi, and Perego-422. Netlist urged the Board to deny the Petition as cumulative and abusive. Ellsberry and Amidi were considered during initial examination—they are listed on the face of the '912 patent—and Perego-422 is similar to another Perego reference considered during prosecution. Appx295-96. Samsung, moreover, was Google's main supplier of infringing memory modules and had been aware of the earlier reexamination but chose not to participate. Appx296-301. The Board instituted review nonetheless. Appx482-89.

The Board relied only on Ellsberry, an abandoned patent application, No. 2006/0277355, filed June 1, 2005 and published December 7, 2006. Appx52. Ellsberry teaches "expand[ing] the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device." Appx11904-05 (¶26). Ellsberry incorporates the JEDEC standard (in part) by reference and aims to "comply with industry standards." Appx11903 (¶9); Appx11908 (¶50).

As shown in Ellsberry's Figure 2, Ellsberry's memory system uses a control unit 204 (blue box) and multiple switches 206 and 208 (red boxes) to control a

number of memory chips (212, 214, 216, 218, 222, 224, 226, 228, green box). Appx11903-06(¶¶28-29, 35). The control unit receives "address and command" signals from the computer's memory controller (through interface 202), and outputs address and command signals (transmitted through wires 220) to control the memory chips. Appx11906(¶39).

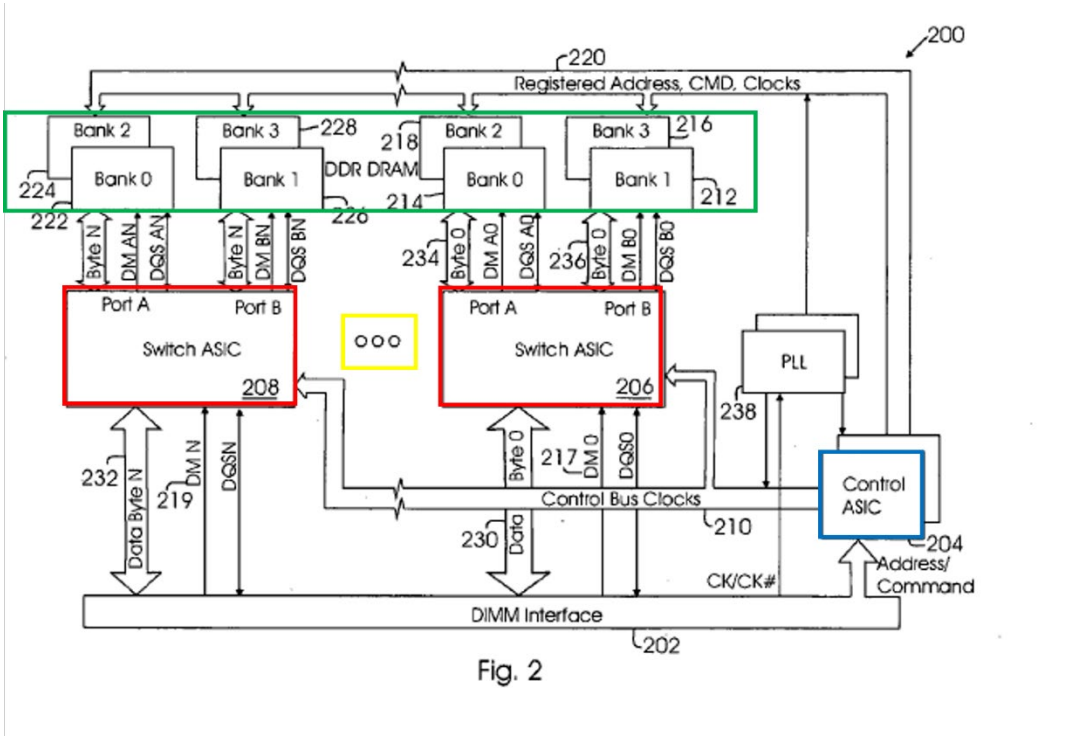


Fig. 2

Appx11885 (annotated).

In Ellsberry, memory chips are organized into "banks" (mapped by the Petition to the claimed "ranks"). Appx11906(¶35) (Ellsberry); Appx202 (Petition). In the image above, there are four banks, "Bank 0" through "Bank 3," each including multiple memory chips. Appx11905(¶30). For example, "Bank 1" includes memory chips 212 and 226, while "Bank 2" includes memory chips 218 and 224.

Appx11905(¶30). Ellsberry undisputedly sends command signals to all DRAM devices in each rank at the same time. Appx11905(¶30).

Each "switch ASIC" and its associated memory chips also constitute a "data group." Appx11905(¶30). As shown above, Ellsberry's memory module features a plurality of data groups—two shown in the image above, with ellipses (yellow box) indicating there are more that are not shown. Appx11905(¶30).

B. The Board's Final Written Decision

The Board determined that claim 16 was obvious in view of Ellsberry.

1. *Whether Skilled Artisans Would Understand Claim 16's "Ranks" Necessarily Include Multiple DRAM Chips*

The Board addressed whether Ellsberry discloses "per DRAM addressability"—*i.e.*, that command signals can be sent "to ***only one*** memory device" as claim 16 requires. Appx84(8:50-54) (emphasis added); Appx105(7:20-24). The Board did not find that Ellsberry teaches or suggests "transmitting [a] command signal" to "***only one*** DDR memory device at a time" in a rank having a plurality of memory devices. Appx50 (emphasis added); *see* Appx103(3:35-36, 42-43). To the contrary, it was undisputed that in Ellsberry, signals are sent to ***all*** the DDR memory devices in a "bank" (which the Board equated with claim 16's "rank"); if there are four DDR devices in a rank, all four get the command. *See* Appx140.

The Board thus posited that "the dispositive issue for claim construction" is "whether 'rank' can include just '***one*** memory device.'" Appx14 (emphasis added).

Ellsberry, the Board stated, disclosed sending commands to a single ***bank*** (rank) at a time. Appx43. The Board asserted that, ***if each bank in Ellsberry has only a single chip***, then sending a command to an entire bank at a time would teach or suggest claim 16's requirement of sending commands to a single chip at a time. Appx46-50. (As explained below, the Board determined that Ellsberry also disclosed ranks that have just "one memory device." Appx50.)

The Board rejected Netlist's argument that "***claim 16 requires*** sending a command to a single device that is ***in a multi-device rank***." Appx51 (emphasis added). The Board never disputed that, in issuing claim 16, the Examiner and the Board previously agreed with Netlist that the claims require sending "'a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.'" Appx10561 (emphasis modified); *see* pp. 15-17, *supra*. Nor did the Board dispute that skilled artisans reading that intrinsic record would understand that claim 16 requires sending the command to one device in a multidevice rank. But the Board, without explanation, dismissed that prosecution history—reflecting the Board's and Netlist's express understanding of the claim's scope—as erroneous. The "reexamination," it declared, "do[es] not elucidate the proper construction of 'rank.'" Appx23.

The Board also rejected Netlist's reliance on claim 16's text. Appx15. Claim 16, Netlist urged, addressed "a type of memory ***standardized by JEDEC***."

Appx950-51 (emphasis added). JEDEC DDR standards required memory modules to read/write 64 or 72 bits at a time, but JEDEC-compliant memory chips were only 4, 8, or 16 bits. Appx952. Consequently, Netlist argued, skilled artisans would understand claim 16's "rank" must contain multiple memory chips working together to meet the overall module's bit-width requirement. Appx952; pp. 7-9, *supra*. The Board, however, merely re-asserted, without explanation, that claim 16 "does not preclude the possibility that a rank could have a single memory device." Appx15.

The Board indicated that the '912 patent's specification does not explicitly state that a rank must include multiple memory devices. Appx18. It did not dispute that skilled artisans reading claim 16's prosecution history—including the Examiner's and its own prior statements—would understand that claim 16 is limited to multi-device ranks. Instead, it cited three instances in the specification, Table 1, Figure 6B, and Example 2, that it believed could include a single-device rank. Appx15-23. It did not explain why those three instances—even if they ***could*** include a single-device rank—would overcome an artisan's understanding that claim 16 complied with JEDEC standards or the prosecution history.

2. *Priority from the '436 Patent and the '244 Provisional*

The Board also rejected Netlist's arguments that Ellsberry was not prior art because the '912 patent was entitled to an earlier priority date. Appx30. The '912 patent, Netlist urged, was entitled to the earlier priority dates of U.S. Patent No.

7,286,436 ("the '436 patent") or U.S. Provisional 60/588,244 ("the '244 provisional"). Appx30.[1]

The '436 Patent. The '912 patent claims priority from the '436 patent. *See* Appx25. The Board held that, although the '436 patent predates Ellsberry, it lacks written-description support for the "register" required by limitation 16[c]. Appx31-32. The Board nowhere denied that registers were commonplace when the '436 patent was filed—or that patents need not disclose what is known in the art. But it rejected Netlist's argument that skilled artisans would understand that the '436 patent's "programmable-logic device (PLD) 642" contains a register. Appx30. Netlist pointed out that the programmable logic device performs "sequential logic" and thus must "include a register to store state values." Appx30. Both parties' experts agreed that skilled artisans would recognize that sequential logic requires "a ***register*** or an equivalent" device. Appx18693-94(117:16-118:20) (Samsung's expert) (emphasis added); Appx18345-46(¶78) (Netlist's expert).

The Board nonetheless held that the '436 patent does not describe a register because it does not "mention" a "register." Appx31. The Board acknowledged the expert consensus that skilled artisans would recognize that the reference to

[1] The Board also found Ellsberry was a prior-art "printed publication" that could be considered in an IPR under 35 U.S.C. §311(b), even though Ellsberry, a patent application that never issued as a patent, was not public as of the '912 patent's latest possible priority date. Appx35.

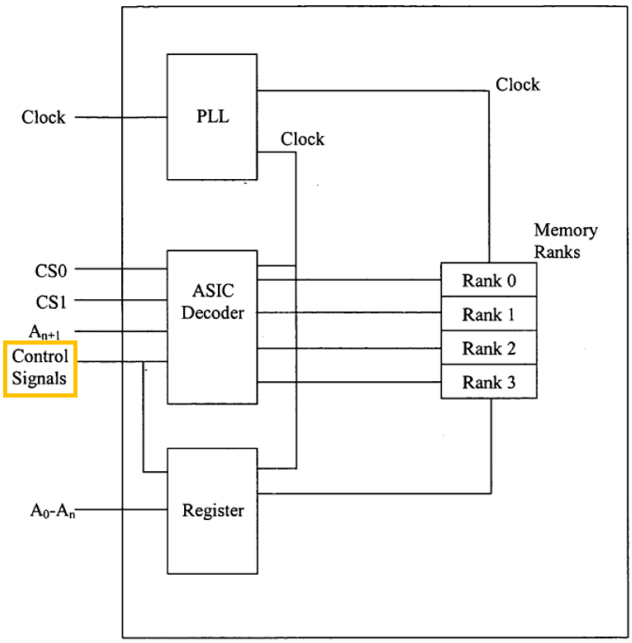
sequential logic requires a register or equivalent device. Appx31. But the Board declared that "other types of devices, such as flip-flops and memory" could perform the same function. Appx31. For the latter determination, the Board invoked a ***2024*** website the Board had found on its own. *See* Appx1583. The Board did not explain how that could somehow reflect a skilled artisan's understanding in 2005.

Although no party requested construction of the "register" limitation, the Board ***sua sponte*** ruled that the '912 patent's "logic element" and the "register" must be "two different things." Appx31-32. Based on that construction, it ruled that the '436 patent's register did not support claim 16, because the '436 patent describes any register as "included in the logic element." Appx31-32. The Board did not mention the '912 patent's disclosure that the "logic element" and the "register" can be "portions of a single component." Appx83(5:37-43).

Finally, the Board faulted Netlist for addressing written-description support only for "'each disputed limitation,' i.e., those raised by Petitioner." Appx33. To establish priority, the Board asserted, Netlist had to discuss "all limitations of claim 16," even those that were undisputed. Appx33-34. The Board did not mention Board precedent holding that a patent owner's written-description showing need only be "commensurate in scope with the specific points and contentions raised by the petitioner." *See, e.g.*, *Lupin Ltd. v. Pozen, Inc.*, IPR2015-01775, Paper 15, at 10-11 (PTAB Mar. 1, 2016); Appx1537.

The '244 Provisional. The '912 patent independently claims priority from the '244 provisional, which also predates Ellsberry. Appx25. The Board held that the '244 provisional did not provide written-description support for a "bank address signal" as limitation 16[c] requires. Appx26-30.

The Board did not dispute that "bank address signals" were, at the time of the '244 provisional, well known. In addition, limitation 16[c] requires a "logic element" to receive a "set of input signals from the computer system," including "bank address signals." Appx103 (3:17-21). The '244 provisional does not use the term "bank address signals," but does disclose "control signals," as shown in Figure 1:



Appx2344 (annotated). Under then-applicable JEDEC standards for DRAM memory modules, "control signals" ***necessarily*** included bank address signals.

Appx18313-19 (¶¶62-64). Without bank address signals, basic operations like "read" and "write" would not work—without knowing the bank, the memory module could not locate the cell it wants to read from or write to. Appx18315-16 (¶63).

In the relevant timeframe, Netlist pointed out, "'***90%*** of DRAM production [was] in compliance with the [JEDEC DDR] standards.'" Appx1263 (quoting *Rambus Inc. v. FTC*, 522 F.3d 456, 459-61 (D.C. Cir. 2008)) (emphasis added). Indeed, the first page of the '244 provisional refers to "personal computer[s]." Appx2283 (¶1). As Samsung's expert confirmed, skilled artisans would understand that to mean JEDEC-compliant memory devices. Appx18649 (73:9-15). Netlist also presented evidence that the '244 provisional uses "specific terminology" indicating that its memory module is a "JEDEC-style memory module"—for example, referring to JEDEC standard chip-select signals "CS0 and CS1," and using the term "rank," which JEDEC created. Appx18313-14 (¶60).

The Board did not engage with that evidence on the merits. Instead, it ruled that, to find written-description support for bank address signals, skilled artisans would have to make a "chain" of "inferences": (1) "that the '244 provisional pertains to DDR memory modules"; (2) "that DDR DRAMs use bank address signals according to the JEDEC standards"; (3) "that bank address signals are not mentioned in the '244 provisional"; (4) "that bank address signals would be included as part of the control signals"; and (5) "that the bank address signals are used for rank multiplica-

tion." Appx29-30. The Board deemed that "chain of inferences too long and speculative" to conclude the inventors possessed the "bank address" limitation. Appx30. The Board did not acknowledge that the second through fourth steps were undisputed. Nor did it mention that its fifth step—using bank address signals for rank multiplication—was not a claim requirement. And that step was disclosed regardless.

SUMMARY OF ARGUMENT

I. Limitation 16[e] requires "transmitting [a] command signal" to a memory device in a selected "rank[ ]," "wherein the command signal is transmitted to ***only one DDR memory device*** at a time." Ellsberry teaches sending commands to every memory device in a rank "***simultaneously***." Appx1021 (emphasis added); *see* Appx1551. To find limitation 16[e] satisfied, the Board construed it to cover sending a command to ***all*** memory devices in a putative "rank" that includes just ***one*** memory device. Appx14.

A-B. The Board's construction defies the prosecution history, the Board's own prior construction, and a disclaimer. During reexamination, the Examiner construed claim 16 to require sending a command to "only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." The Board and this Court affirmed. The Board in this case was not free to disregard that history. The claims, moreover, recite JEDEC's "DDR" standard, which precludes single-

device ranks. The specification, which cites JEDEC's standards, uniformly provides for ranks having more than one memory device. The Board's contrary decision improperly defies the intrinsic evidence and its own prior decisions. Even if the Board were not bound by its prior construction, the APA required it to explain why it reached the opposite result here. The Board failed to do that.

C. The Board's construction attempts to interpret "rank" in the abstract rather than in the context of the claims, specification, and prosecution history. Claim differentiation cannot support the Board's decision, much less override prosecution history. And the Board misapprehended the specification—erroneously concluding that abbreviated examples that illustrate operational details somehow show that claim 16's ranks can have just one memory device.

II. Even if sending a command to a single-device "rank" could satisfy claim 16, Ellsberry does not teach single-device ranks. The Board pointed to Ellsberry's Figure 12, but misunderstood what that figure shows—***part*** of a rank, not an entire rank with just one memory device. The Board recognized that aspect of Ellsberry in a prior IPR, but it again ignored its earlier decision here.

III. The Board's determination that Ellsberry is prior art to the '912 patent cannot be sustained because the patent claims priority to ***two*** filings that antedate Ellsberry.

A. The ’912 patent is entitled to priority from Netlist’s ’436 patent. The Board asserted that the ’436 patent does not disclose a “register.” But registers were well known at the time. And there was no dispute that skilled artisans would recognize the ’436 patent’s disclosure of “sequential logic” to require a “register or an equivalent” device. That constitutes disclosure. The Board’s *sua sponte* ruling that the “register” and “logic element” must be “two different things,” Appx31, was both improper and plainly wrong. And the Board’s insistence that Netlist should have addressed undisputed limitations contravenes its own precedent.

B. The ’912 patent is also entitled to priority from the ’244 provisional. The Board ruled that the ’244 provisional does not disclose “bank address signals.” Appx29-30. But bank address signals were well known at the time of the ’912 patent. And it was undisputed that the ’244 patent discloses “control signals,” which the JEDEC standards required to contain bank address signals. The Board’s response—that the ’244 provisional might not be referring to JEDEC-compliant memory devices—defies precedent and the unrebutted evidence. And the Board’s reference to a “chain” of five “speculative” inferences, Appx30, overlooks that four of the five were effectively undisputed or irrelevant.

C. Ellsberry was not a “patent[ ]” or a “printed publication[ ]” on the ’912 patent’s critical date and thus is not prior art under 35 U.S.C. § 311(b).

STANDARD OF REVIEW

Obviousness is a question of law, reviewed de novo; underlying factfindings are reviewed for substantial evidence. *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886 (Fed. Cir. 2024). Claim construction is reviewed de novo, including the Board's evaluation of intrinsic evidence. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 808 (Fed. Cir. 2021). Sufficiency of written description is reviewed for substantial evidence, but the Board's interpretation of precedent regarding the written-description requirement is reviewed de novo. *Falkner v. Inglis*, 448 F.3d 1357, 1362 (Fed. Cir. 2006). Board decisions must be vacated if they are "arbitrary, capricious, an abuse of discretion," "not in accordance with law," or "unsupported by substantial evidence." *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 992 (Fed. Cir. 2017).

ARGUMENT

It is said that doing the same thing over and over again, while expecting different results, is the definition of insanity. For challengers to Netlist's patent, however, it turned out to be sound litigation strategy. Netlist's '912 patent has been subject to post-grant challenge after post-grant challenge. Almost immediately upon issuance, it was hit with three inter partes reexaminations by Google and others. Over the ensuing decade, those reexaminations generated over a dozen asserted grounds of unpatentability, twenty-plus briefs, five office actions, two appeals to the

Board, and an appeal to this Court. When the dust settled, the Examiner and the Board upheld the patent's claim 16, and this Court affirmed. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020). But the ordeal continued. Samsung, Google's supplier of infringing memory devices, continued the campaign against claim 16 by filing this IPR—the fourth administrative challenge to the claim. And ***this*** time, the Board declared claim 16 unpatentable.

Did Samsung discover some previously unknown, silver-bullet prior art? No. The Board's decision rested entirely on Ellsberry, a reference listed on the face of the '912 patent and considered during initial examination. The Board justified invalidating claim 16 this time based on a claim construction ***directly contrary*** to the construction that the Board and the Examiner previously adopted—and Netlist accepted—in the prior reexaminations. The Board never explained why it could disregard that part of the intrinsic record—or why skilled artisans would ignore that powerful evidence of meaning in reading the claims.

That is not how claim construction—or administrative law—is supposed to work. The PTO is not a casino where patent challengers can keep pulling the slot machine, in hopes that the ***next*** Board panel will turn up their desired result. A patent claim does not change meaning from proceeding to proceeding or from panel to panel. That is especially true where, as here, the Examiner and Board adopt a claim construction and the patent owner agrees to that construction: Those repre-

sentations effect a disclaimer of alternative constructions that is ***binding*** on the patentee and the Board alike.

Those principles foreclose the Board's about-face here. In the prior reexaminations, the Examiner and Board construed claim 16 to require ***multiple*** memory devices in a rank: The claim, they ruled, requires transmission of a command signal "to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Appx7337, Appx10561 (emphasis added). Netlist accepted that construction, not merely by defending the Examiner's decision before the Board, but also by restating claim 16 in light of that construction. That constituted a clear disclaimer of single-device ranks, which the Board was not free to disregard. Yet it did precisely that below. This time, the Board held claim 16 ***does*** encompass single-device ranks. And it ruled that Ellsberry rendered the claim obvious because it (purportedly) disclosed sending a command signal to only one DDR memory device at a time ***if*** there was only one memory device in a rank.

The defects with the Board's decision run deeper still. The Board's newly minted construction defies the claim language and specification, as well as the industry standards they incorporate. Ellsberry does not teach what the Board professed to find in it. And Ellsberry is not even prior art: Netlist antedated it with ***two*** filings that disclose claim 16's invention.

I. THE BOARD'S RULING THAT CLAIM 16 COVERS A "RANK" HAVING ONLY ONE DRAM DEVICE REQUIRES REVERSAL

Claim 16 requires "transmitting [a] command signal to at least one DDR memory device of [a] selected one or two ***ranks***," "wherein the command signal is transmitted to ***only one DDR memory device*** at a time." Appx103 (3:35-43) (emphasis added) (limitations 1[c] & [e]). There was no dispute Ellsberry teaches sending commands to ***every*** DRAM device in a rank "***simultaneously***." Appx1021 (emphasis added); *see* Appx1551. That is the opposite of selectively sending commands "to only one DDR memory device at a time." To find limitation 16[e] satisfied nonetheless, the Board construed that limitation to cover sending commands to ***all*** memory devices in a "rank" where the rank happens to "include only one memory device." Appx14.

That construction directly contradicts the Board's ***own*** construction when claim 16 was issued; it defies the prosecution history; it contravenes the claim's text; and it makes no sense. During a lengthy reexamination, the Examiner construed original dependent claim 16 (now limitation 16[e]) to require "'transmit[ting] a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.'" Appx6375 (emphasis added); *see* Appx7231; Appx7337; Appx7494. The Examiner understood claim 16 only applies to—and only makes sense in the context of—ranks that have more than one memory device. Netlist disclaimed any construction that would cover sending commands to all

devices in a rank, merely because a rank may have one device in it. The Board in turn agreed that claim 16 requires "'transmit[ting] a command signal ***to only one DDR memory device at a time when there is a plurality of memory devices in a rank***,'" upholding the claim in the reexamination on that basis. Appx10561 (emphasis Board's). And this Court affirmed. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

That history forecloses the Board's effort to impose the opposite construction here. The meaning of a claim does not change simply because there is yet another challenge before a different PTAB panel. More fundamentally, the Examiner's and Board's prior construction is part of the intrinsic evidence to which skilled artisans would look to determine the claim's scope. The Board never explained why the Patent Office's own view of the claim during the reexamination—when claim 16 issued—would not be determinative to any reader of the intrinsic record. Indeed, Netlist accepted that construction, disclaiming a broader scope. Reversal must follow.[2]

[2] All the Petition's combinations urge that claim 16 is obvious in view of prior art involving single-device ranks. Appx189-91; Appx237-39. If limitation 16[e] requires the capability to transmit a command signal to a single device in a multi-device rank, the Petition fails on all grounds.

A. Claim 16 Covers Sending Commands to Only One DRAM Among Multiple DRAMs in a Rank—Not Sending a Command to *Every* DRAM in a "Rank" That Happens To Have Only One DRAM

Claim construction "seeks to accord a claim the meaning it would have to a person of ordinary skill in the art at the time of the invention." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004). That requires looking to the entire intrinsic record, including "'the written description and the prosecution history.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). This Court thus has warned against looking at "'ordinary meaning . . . in a vacuum,'" or fixating on the "abstract meaning of words rather than on the meaning of claim terms within the context of the patent." *Id.* at 1313, 1321.

Here, the Board strained to give claim 16 an expansive meaning that, in view of the invention's nature and prosecution history, it simply cannot bear. The whole point of the invention—of individual DRAM-chip addressability—is to send a command to one device in a rank without sending it to the other devices in the rank. Claim 16 thus provides for "transmitting [a] command signal to at least one DDR memory device of [a] selected one or two ***ranks***," wherein "the command signal is transmitted to ***only one DDR memory device*** at a time." Appx103(3:35-43) (emphasis added) (limitations 1[c] & [e]). That language, by its terms, refers to sending the command to only one of the multiple memory devices in a rank—not

broadcasting it to every memory device in the rank when it just so happens the rank allegedly has only one device.

1. The prosecution history makes that undisputable. Prosecution history, "'***including reexamination proceedings***,'" *Infinity Comput. Prods., Inc. v. Oki Data Am., Inc.*, 987 F.3d 1053, 1059 (Fed. Cir. 2021) (emphasis added), is "intrinsic evidence" for claim construction, *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999). And where, as here, the patentee "disavowed a potential interpretation of" the claim "during prosecution" by accepting the "Examiner's" construction, that disavowal is binding in subsequent proceedings, ***including on the Board***. *Elkay*, 192 F.3d at 979; *see Biogen Idec, Inc. v. GlaxoSmithKline LLC*, 713 F.3d 1090, 1095 (Fed. Cir. 2013). The "Board in an inter partes review ***can[not]*** ignore statements made in a prior reexamination," and "***must*** 'exclude any interpretation that was disclaimed.'" *VirnetX Inc. v. Mangrove Partners Master Fund, Ltd.*, 778 F. App'x 897, 910 (Fed. Cir. 2019) (emphasis added); *see Arendi S.A.R.L. v. Google LLC*, 882 F.3d 1132, 1136 (Fed. Cir. 2018).

Here, limitation [e] of independent claim 16 was dependent claim 16 before the reexamination. Appx97(34:57-59); *see* pp. 14-16, *supra*. In the reexamination, the Examiner upheld claim 16 over a prior-art reference, Amidi, by construing the claim to require "only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Appx6375 (emphasis added). Amidi taught sending

commands "to ***all devices***" in a rank—regardless of how many there were—and thus did not teach the claim. Appx6413 (emphasis added). It thus was irrelevant whether Amidi theoretically could send commands to only one device at a time where the "rank" had only "'one memory device.'" Appx6911. A command in Amidi would ***not*** be sent to just one memory device "when there is a plurality of memory devices in a rank," as claim 16 requires. Appx7231. Netlist accepted the construction by canceling independent claim 15 and restating claim 16 to incorporate the limitations of original claim 15 while retaining the requirement of original dependent claim 16 that the Examiner had upheld. Appx5615-16.

The Board upheld the Examiner. Appx10560-61. It agreed that claim 16 requires "'transmit[ting] a command signal ***to only one DDR memory device at a time when there is a plurality of memory devices in a rank***.'" Appx10561 (emphasis Board's). The Board ruled that Amidi did not teach that requirement, because it taught the conventional approach of sending a command to all "memory ***devices***" in a rank. Appx10561-62 (emphasis Board's). Like the Examiner, the Board did not deny the possibility that a rank in Amidi could include only one memory device, such that sending a command to all memory devices in a rank would entail sending a command to only one memory device. *See* Appx6911. Indeed, one of the requesters argued that Amidi disclosed precisely that. *See* p. 16, *supra*. But that could not satisfy claim 16, which requires sending a command signal "'to only

one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.'" Appx10561 (some emphasis omitted). This Court affirmed. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

Those rulings are dispositive here. Skilled artisans would understand the meaning of claim 16 from that prosecution history. *Elkay*, 192 F.3d at 979. Indeed, Netlist "disavowed" any "potential interpretation of" claim 16 that would encompass a single-device rank. *Id.* After the Examiner construed claim 16 to require sending a command to "only one DDR memory device at a time when there is a plurality of memory devices in a rank," Appx6375, Netlist accepted that construction and restated the claims accordingly, Appx5615-16. This case is indistinguishable from *Elkay*, where this Court treated the patentee's acceptance of the Examiner's construction as a disclaimer of any alternative construction. That disclaimer is binding on Netlist and the Board alike. *See VirnetX*, 778 F. App'x at 910. That should have ended the matter.

2. Regardless, claim language confirms the Examiner's prior construction. Skilled artisans read claim terms in view of the "intrinsic evidence," including material "cited in [the] patent." *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005). Industry "standard[s]" "reference[d]" in a patent are highly relevant to claim construction and "'treated as intrinsic evidence.'" *Vizio, Inc. v. Int'l Trade Comm'n*, 605 F.3d 1330, 1337 (Fed. Cir. 2010); *see LG Elecs.,*

Inc. v. Bizcom Elecs., Inc., 453 F.3d 1364, 1375 (Fed. Cir. 2006), *rev'd on other grounds*, *Quanta Comput. Inc. v. LG Elecs., Inc.*, 553 U.S. 617 (2008); *Wellman Inc. v. Eastman Chemical Co.*, 642 F.3d 1355, 1367-68 (Fed. Cir. 2011) (skilled artisans "interpret[ ]" patent disclosures in view of "standard industry guidance").

Here, the claims reference JEDEC's "DDR" standard. Appx103(3:13-16). The specification cites several DDR standards and incorporates one by reference. Appx62; Appx86(12:40-41). Indeed, "[t]he term rank was ***created by JEDEC***." Appx19644 (emphasis added); *see* p. 8, *supra*. And "'***90%*** of DRAM'" devices implement that standard. Appx1263. Skilled artisans thus would understand the contents of a "rank" in claim 16 to reflect how that term was used in JEDEC DDR standards cited by the patent.

JEDEC standards ***preclude*** memory modules with one DRAM chip per rank. Consistent with the Examiner's and the Board's earlier construction of claim 16, the "ranks" necessarily consisted of multiple DRAM chips. As explained above, the bit-width of the memory ***chips*** in a rank must ***add up*** to the bit-width of the ***memory module***. *See* pp. 7-9, *supra*. The cited standards specify memory-module bit-widths of 64 or 72 bits, but DRAM-chip bit-widths of 4, 8, or 16 bits. Appx17358; Appx81(2:4-15, 2:20-23); Appx18454-55(¶247); Appx18460-61(¶255); Appx20263. Thus, each rank must have multiple DRAM chips, *e.g.*, four 16-bit DRAM chips to form a 64-bit memory module. Appx18455.

JEDEC's use of "rank" to refer to an arrangement of multiple DRAM chips reflects the word's dictionary meaning. In ordinary usage, "rank" refers to a "line" of multiple items or people, such as a "row of squares" on a chessboard, or a "line of soldiers ranged side by side." *Webster's New International Dictionary* 2061 (2d ed. 1934). A "rank" of one item—*e.g.*, one DRAM chip—makes no sense in JEDEC's usage or the term's origins.

The JEDEC standards cited in the patent and recited in the claim thus required ranks of multiple DRAM chips—they did not permit a putative "rank" with only one DRAM device. Skilled artisans would have understood claim 16's requirement of sending a "command signal . . . to only one DDR memory device at a time" as sending it to ***one among multiple*** devices—not sending it to all devices in a rank and it somehow turns out that there is a rank with only one device (contrary to the standard). That was how the Board, the Examiner, and Netlist ***all*** construed the claim years ago in the reexaminations. *See* pp. 14-17, *supra*.

3. The specification points the same way. It cites or incorporates by reference several JEDEC standards, Appx62; Appx86(12:40-41), which require more than one DRAM device per rank, *see* p. 39, *supra*. The specification's embodiments, consistent with JEDEC standards, likewise depict ranks having multiple DRAM chips. *See* Appx81(1:50-2:23) (referring to 64-bit and 72-bit memory modules); Appx85(9:38-10:30) (ranks comprising "eight 512-Mb memory

devices"); Appx86(11:15-42); Appx86(12:39-55) (Table 3A specifying 4, 8, or 16 bit-width chips "as specified by JEDEC standard[s]").

The invention's stated "purpose," Appx83(5:1-5), compels the same result. *See Kaken Pharm. Co. v. Iancu*, 952 F.3d 1346, 1352 (Fed. Cir. 2020). As the specification explains, memory-module makers had ***already*** "increased" memory-module capacity by "***increasing the number of memory devices per rank***." Appx81(2:23-26) (emphasis added). That is, they had used more DRAM chips in each rank to increase total capacity. The invention sought to ***further*** enhance capacity by "increasing the number of ranks" and to provide other benefits by allowing for per-DRAM addressability. Appx81(2:23-28). Skilled artisans would understand that claim 16 was addressing memory modules that already had a large "number of memory devices per rank"—not one device per rank.

B. The Board's Contrary Construction Defies the Intrinsic Evidence and Its Own Prior Decisions

The Board did not dispute what the record makes clear: The Examiner and Board had previously ruled claim 16 requires transmitting a command to "only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Appx6375 (emphasis added); Appx7231; Appx7337; Appx7494. And Netlist accepted that construction and restated the claims accordingly. Appx10649.

1. Seeking to reach a different result in ***this*** case, the Board suggested that the "language of claim 16 does ***not preclude*** the possibility that a rank could have a

single memory device," or that skilled artisans might not understand the claims to incorporate JEDEC standards. Appx14-15 (emphasis added); Appx51. But those assertions defy what the Board, the Examiner, and Netlist said during the reexamination that produced claim 16. The Board never explained why skilled artisans, reading that intrinsic record, would not have understood the claims consistent with the Examiner's and the Board's clear and repeated articulation. Nor could it: Under this Court's precedents, "[w]e look at what an ordinarily skilled artisan would understand about claim scope ***from reading the prosecution history***." *Blackbird Tech LLC v. ELB Elecs., Inc.*, 895 F.3d 1374, 1378 (Fed. Cir. 2018) (emphasis altered).

Nor was the Board free in this case to simply ignore Netlist's disclaimer. "Arguments and amendments made during the prosecution of a patent application . . . ***must*** be examined to determine the meaning of terms in the claims." *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995) (emphasis added). Likewise, "the Board in an inter partes review can[not] ignore statements made in a prior reexamination." *VirnetX*, 778 F. App'x at 910. And where such statements reflect disavowal of claim scope, the "Board ***must*** 'exclude any interpretation that was disclaimed during'" the earlier proceeding. *Id.* (emphasis added). Whatever the Board might now think the claim should mean ***absent*** that history, the

claim's meaning became fixed in view of a prosecution history and disclaimer the Board has no authority to erase.

2. Regardless, the Board must explain departures from prior rulings. *See Jicarilla Apache Nation v. U.S. Dep't of Interior*, 613 F.3d 1112, 1119-20 (D.C. Cir. 2010); *BASF Corp. v. Enthone, Inc.*, 749 F. App'x 978, 985 (Fed. Cir. 2018). "[A]n agency changing its course . . . is obligated to supply a reasoned analysis for the change." *Motor Vehicle Mfrs. Ass'n of U.S., Inc. v. State Farm Mut. Auto. Ins. Co.*, 463 U.S. 29, 42 (1983). That did not happen here.

Rather than explain ***why*** it departed from the prior construction, the Board announced that the Examiner's prior decision did not "elucidate the proper construction of 'rank.'" Appx23. The Board characterized the Examiner as having "merely" faulted Requester for failing to explain "why one would transmit a command signal to only one DDR memory device at a time when ***Amidi*** teaches there are a plurality of memory devices in a rank." Appx493-94 (emphasis added). That, the Board asserted, "is not the same as stating that claim 16 requires a plurality of memory devices in a rank." Appx493-94. The Board's view of whether the Examiner had "engag[ed] in claim construction," of course, "is not dispositive as to whether claim construction occurred." *Google LLC v. EcoFactor*, *Inc.*, 92 F.4th 1049, 1056 (Fed. Cir. 2024). Clearly, the Examiner had done so.

The full sentence reads: "Requester has not provided a reasonable explanation as to why ***one skilled in the art would transmit a command signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank***." Appx6374-75 (emphasis added). The Examiner was not addressing any argument about what ***Amidi*** taught. Instead, the Examiner was stating that the requester had not shown claim 16 obvious because the requester offered no reason "why" "one skilled in the art" would do what ***claim 16*** requires—"transmit[ting] a command signal to only one DDR memory device . . . ***when there is a plurality of memory devices in a rank***." Appx6375 (emphasis added). The Examiner repeated that same statement several more times in response to different arguments—none of which turned on the number of memory devices per rank in Amidi. Appx7231; Appx7337; Appx7494. The Examiner's statements plainly "establish[ed] a limit to the scope of" claim 16, and thus issued "a construction of the claim." *EcoFactor*, 92 F.4th at 1056; *see also Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1350 (Fed. Cir. 2001). "[A] person of ordinary skill" reading the prosecution history would so understand, foreclosing the Board's contrary protestation. *Tech. Props. Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1359 (Fed. Cir. 2017).

The Board also failed to acknowledge ***its own prior reasoning*** on appeal of the Examiner's ruling in the reexamination. There, the Board agreed with the Examiner and Netlist that sending commands to all devices in the rank is insufficient

to meet limitation 16[e], because the device must allow access to a specific cell in "'one DDR memory device at a time when there is a plurality of memory devices in a rank.'" Appx10561 (emphasis omitted). It found claim 16 nonobvious for that very reason. Appx6375; Appx6413. If the claim's text and prosecution history do not themselves foreclose the Board's new view—and they do—the Board must at least provide a reasoned explanation for changing its view. *State Farm*, 463 U.S. at 42; *Jicarilla*, 613 F.3d at 1119-20. It did not.

C. The Board's Construction Cannot Be Sustained Regardless

Given the Examiner's and the Board's prior construction—and Netlist's disclaimer—this Court could stop here. But the Board's effort to justify its new construction independently fails. Defying *Phillips*'s direction that claim terms should not be construed in a "vacuum" or in "the abstract," 415 F.3d at 1313, 1321, the Board ignored important clues—that claim 16 uses JEDEC terms; that the word "rank" itself is a JEDEC term; and that the specification incorporates the JEDEC standard by reference. *See* Appx14-15. Instead, it searched for ***conclusive proof*** that the term "rank" can ***never*** consist of a single device. Appx14-15. It insisted the "language of claim 16 does ***not preclude*** the possibility that a rank could have a single memory device." Appx14-15 (emphasis added). And it appeared to require that the specification ***explicitly state*** in all examples that it is referring to multi-device ranks, interpreting anything less as an example of a single-device-rank

disclosure. *See* Appx23; pp. 48-50, *infra*. But claims must be fairly construed—not expanded at the cost of all context and content.

1. For example, the Board dismissed JEDEC's requirements because "claim 16 does not require any particular bit width." Appx51. But even if the patentee had "not act[ed] as its own lexicographer" by "incorporat[ing]" the JEDEC "standard," the "standard remains" relevant "intrinsic evidence" on the "meaning of the claim term to one of ordinary skill in the art." *LG Elecs.*, 453 F.3d at 1374-75. Skilled artisans would understand claim 16 used "rank" consistent with the JEDEC "DDR" standard—which excludes "ranks" of a single device. *See* p. 39, *supra*.

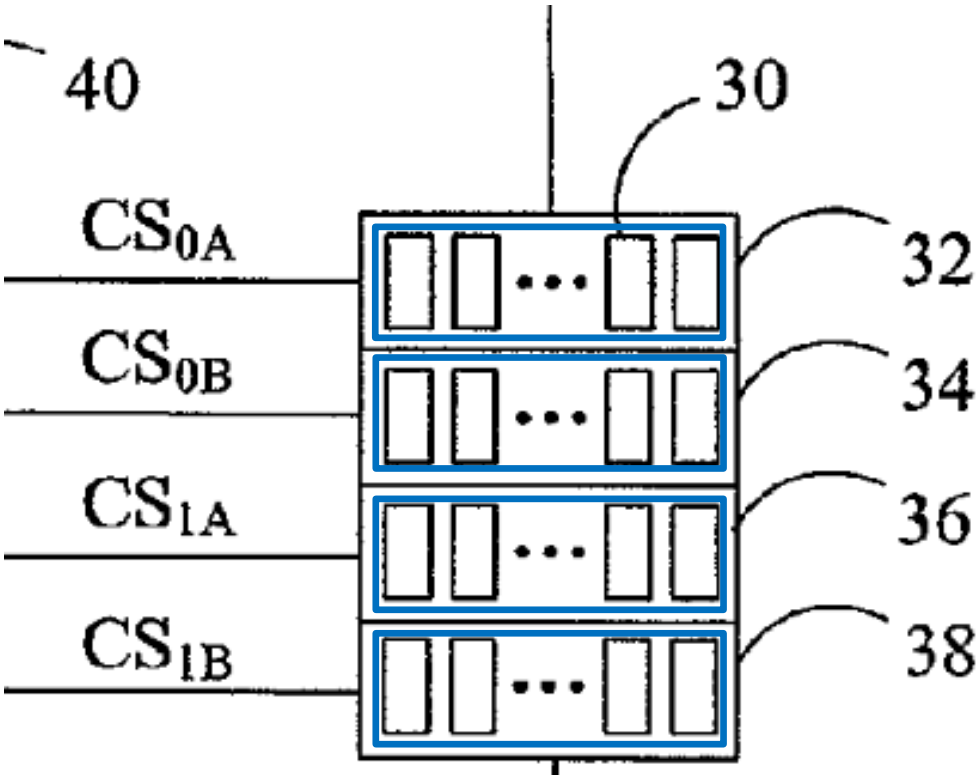
2. Nor does claim differentiation support the Board's view. Claim 55, which depends from claim 1, requires that "each rank of the first number of ranks comprises a ***plurality*** of the DDR DRAM chip packages." Appx104(5:53-65) (emphasis added). The Board thought claim 55 "implie[d] that each of the ranks recited in claim 1 could include a single memory device" because, "[o]therwise, the limitation would be superfluous." Appx15. But "the presumption that an independent claim does not have a limitation that is introduced for the first time in a dependent claim" is most applicable "'when the limitation in dispute is the ***only meaningful difference*** between an independent and dependent claim.'" *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004) (emphasis added). Not so with claim 55, which adds a new structural limitation to claim 1. It specifies

that "the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system." Appx104(5:59-62). Inferences drawn from additional differences are weak at best—and certainly cannot overcome prosecution history.

Indeed, much of claim 55 repeats what was already in claim 1. For instance, claim 55 states that claim 1's "DDR memory devices" are "dynamic random-access memory (DRAM) chip package[s]." Appx104(5:55-56). But that is true by definition. Appx83(6:15-16) (emphasis added). Claim 55 recites that claim 1's memory devices have a "bit width." Appx104(5:53-56). That is true inherently. *See e.g.,* Appx81(1:44, 1:63). Claim 55 defines the "bit width" of each of the first number of ranks as "equal to the summed bit widths of the DDR DRAM chip packages of the rank." Appx104(5:58-59). But that was true in claim 1 as well—it is simply the definition of the bit width of a physical rank. *See* Appx18374(n.4). There is no reason to read claim 55's statement that ranks comprise a "plurality" of DDR chips any differently—as doing anything other than (like other passages) repeating requirements claim 1 imposes already. Indeed, the "only meaningful difference" between claim 55 and claim 1 is the "non-volatile memory device." *See Liebel-Flarsheim*, 358 F.3d at 910. The Board erred in attempting to "distinguish" the wrong "limitation" "from its counterpart in another claim." *Kraft Foods, Inc. v. International Trading Co.*, 203 F.3d 1362, 1368 (Fed. Cir. 2000).

3. The Board did not deny the specification consistently uses "rank" to refer to ranks with multiple memory devices, or that every embodiment depicted in the figures has multiple memory devices per rank. *See* pp. 40-41, *supra*. Instead, the Board pointed to three portions of the specification and insisted they show that ranks could have just one memory device. Appx15-23 (citing Appx84(7:55-8:64); Appx70(Fig. 6B); Appx89-90(17:28-20:53)). Even if one were to ignore ***everything else*** pointing the opposite way, those passages offer the Board no support. Each example the Board characterized as depicting a rank with one memory device is a "simplified" drawing or description that focuses on one or a pair of memory devices to illustrate an aspect of the invention and thus "omits" other memory devices in those same ranks. *Starhome GmbH v. AT&T Mobility LLC*, 743 F.3d 849, 857 (Fed. Cir. 2014). The Board cannot draw conclusions from "simplified" drawings and depictions that contradict "the consistent and unambiguous detailed teachings of the specification." *In re Andersen*, 743 F.2d 1578, 1581 (Fed. Cir. 1984).

The Board relied on Table 1 and its corresponding description as supposedly addressing single-device ranks. Appx17-18; *see* Appx84(7:56-58). But Table 1 refers to the embodiment in Figure 1A, *see* Appx84(7:35-60), and uses identical labels, *see Ironworks Pats. LLC v. Samsung Elecs. Co.*, 798 F. App'x 621, 625 (Fed. Cir. 2020). And, as shown below, Figure 1A depicts ranks (32, 34, 36, 38, blue boxes) having multiple memory devices per rank.



Appx63 (Fig. 1A) (annotated).

Table 1's textual description is not to the contrary. Appx18. The Board noted that it mentions selecting ***two*** ranks and sending a command to "***both*** memory devices," as if that meant each rank has just "***one*** memory device." Appx18 (emphasis added). But nothing in that description suggests those are ***the only memory devices*** in the respective ranks. The passage simply describes the operation of ***one of the*** memory devices in each rank to illustrate the invention.

Figure 6B depicts using "isolation device 120 to avoid collisions between memory devices 'a' and 'b' of different ranks." Appx18-19. That again does not mean that each rank has one memory device ("a" or "b"). Appx19. Instead, as with Table 1, the specification merely illustrates an aspect of the invention—dealing with

data "collision[s]"—by zooming-in on a pair of memory devices in two respective ranks. Appx92(24:31-34). Nothing suggests that those two devices are the ***only ones*** in their respective ranks.

Finally, Example 2 reproduces "Verilog" code describing the operation of certain hardware circuits in the memory modules. Appx87(14:10-13). As with Table 1 and Figure 6B, Example 2 shows the operation of a pair of devices, one in each of two ranks, without suggesting that each rank only has one device. Skilled artisans would understand that the described hardware circuits would be duplicated for the "other" devices in each rank. Appx18297-98(¶40); Appx1563(71:5-17). Regardless, the Board's effort to find single-device ranks in the specification cannot overcome the PTO's prior construction, the prosecution history, and Netlist's disclaimer.

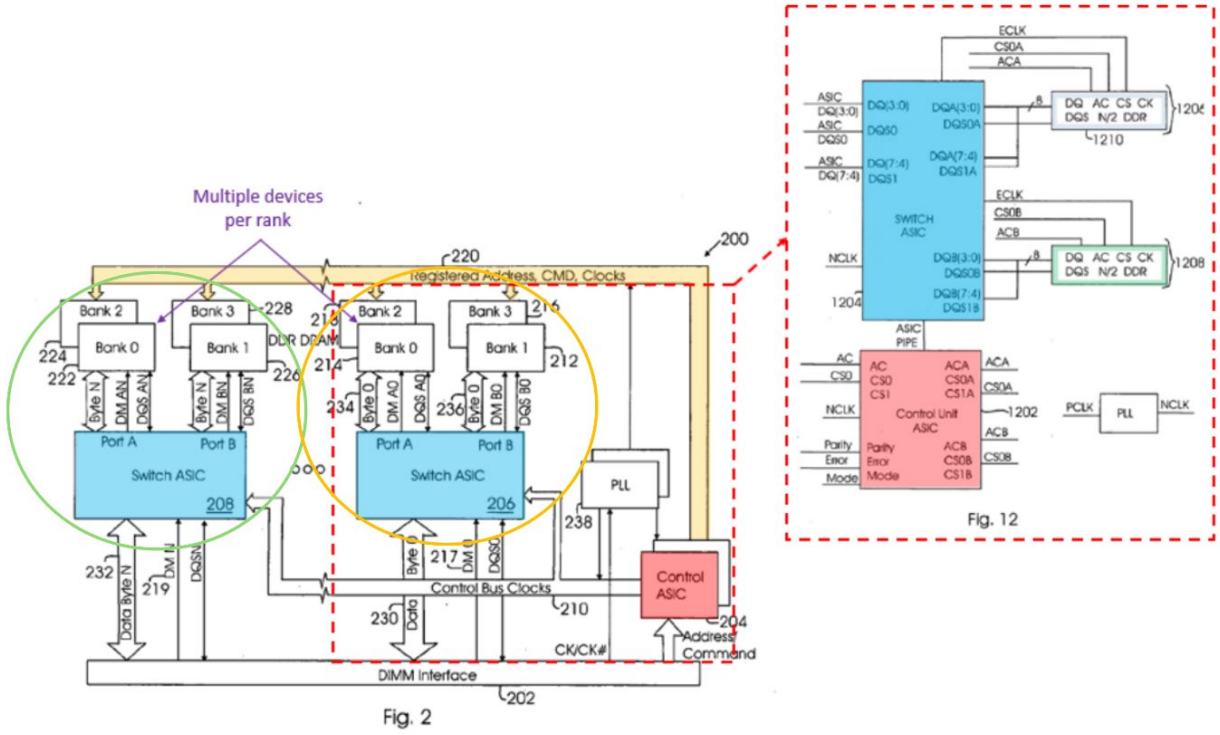
II. THE BOARD'S DETERMINATION THAT ELLSBERRY TEACHES CLAIM 16 IS UNSUPPORTED EVEN UNDER THE BOARD'S ERRONEOUS CONSTRUCTION

Besides, Ellsberry does not teach sending a command to only one device in a rank. It teaches sending commands to all devices in a rank, and nowhere discloses a single-device rank.

A. Ellsberry's Figure 12 Does Not Show a Single-Device Rank

The Board invoked Ellsberry's Figure 12 as showing a memory module with ranks having only one memory device. Appx50. Figure 12 does not show a rank with only one memory device (chip); it shows a "data group" that contains only ***part***

of a rank. Ellsberry's memory module organizes memory chips into both "***banks***" (which the Board identified as "ranks") and "***data groups***." Appx11906(¶35) (emphasis added); *see* pp. 19-20, *supra*. Each data group includes one memory device ***from each rank***. Ellsberry's Figure 2, on the left below, depicts a whole memory module including a plurality of data groups; Figure 12, on the right below, depicts one data group. Appx18450-51(¶¶240-41).



Appx18450(¶240) (showing Fig. 2, left, and Fig. 12, right; annotated).

Figure 2 shows a memory module with at least two data groups (circled in orange and green). Appx11905(¶30). Each data group has one switch ASIC (blue) and four memory chips. Appx11905(¶30). The memory module also has four banks

(or ranks), which ***cut across*** the data groups. Appx11929-30. As shown on the left above, "Bank 0" (putative rank 0) has one memory chip (222) in one data group (green circle) and another chip (214) in the other data group (orange circle); the rank thus has ***two*** memory chips total. The same is true for Banks 1-3. Since Ellsberry teaches multiple data groups in a memory module, Appx11905(¶30), there are multiple memory chips per rank (one for each data group) as well. Appx18451(¶241).

Figure 2 "does not provide details on how each switch ASIC is connected to the different memory banks"; that detail is provided in "Figures 10-13." Appx18451(¶241). Thus, while Figure 12 depicts a data group with one memory chip in bank 1206 and one memory chip in bank 1208, Appx11908(¶55), those banks do not consist of just one memory chip. Instead, the module has ***other data groups***—not shown in Figure 12 but shown in Figure 2—with additional memory chips that ***also*** belong to bank 1206 and bank 1208. Appx18450(¶240). Figure 12 thus is just a "simplified" schematic, which "omit[s]" an element that "is not needed to explain the [embodiment]." *Starhome*, 743 F.3d at 857.

The Board's conclusion that Ellsberry's Figure 12 shows a memory module with one memory chip per rank also overlooks Ellsberry's purpose—to "***expand[] the memory capacity*** of a memory module." Appx11903(¶10) (emphasis added). "Reducing the number of devices per rank (to one device per rank) would reduce

rather than expand the capacity of the memory module." Appx18456(¶248). It would also be technically and economically non-sensical. Appx18458-59(¶252). If Ellsberry provided for single-device ranks, it would not use a costly switch memory module architecture; it would just use higher-density memory devices. Appx18458-59(¶252). Skilled artisans would not view Figure 12 to disclose a single-device rank contrary to Ellsberry's purpose. *Cf. Medtronic, Inc. v. Teleflex Innovations, S.a.r.l.*, 69 F.4th 1341, 1349 (Fed. Cir. 2023).

A single-device rank design would also render Ellsberry non-compliant with JEDEC standards. Ellsberry acknowledges and incorporates JEDEC standards. Appx11907-08(¶50). And the Petition relied on JEDEC standards to map ***other*** claim 16 limitations to Ellsberry. *See, e.g.*, Appx41-42; *see* Appx18454-55(¶247); Appx18460(¶255). If a rank in Ellsberry had only one memory device, as the Board posited, Figure 12 would show an 8-bit memory module. Appx48-51. But 8-bit modules were not then in use and would have violated JEDEC standards. Appx18458(¶251); Appx18460(¶255). Skilled artisans would not have understood Ellsberry and Figure 12 to be non-compliant with industry standards. The Board failed to consider that compelling evidence.

B. The Board's Conclusion Contradicts Its Own Prior Rulings

The Board's determination here that Ellsberry's Figure 12 discloses an entire memory module with just one memory chip per rank contradicts its findings in a

prior Netlist IPR involving Ellsberry. There, the Board agreed Ellsberry's memory modules have "'***multiple*** . . . Data Group[s]'"—units of one switch ASIC and the associated memory chips. Appx11929 (emphasis added); *see* pp. 50-52, *supra*. Consistent with that, the Board found that Figures 11 and 13, which, like Figure 12, depict ***one*** data group, reflect only "part of" the multi-data-group module shown in Figure 2. Appx11959; Appx11966; *see* Appx11986 (noting Ellsberry "relate[s]" "Figures 10, 11, 12, and 13" to "Figures 2, 5, and 6").

The Board's effort to characterize Figure 12 as a standalone memory module here, Appx51, cannot be reconciled with its prior determination that it shows ***part*** of a memory module—one of multiple data groups. Appx11986. If the Board is going to change its mind about what a figure means, it must acknowledge and explain that change. *Jicarilla*, 613 F.3d at 1119. The Board did not. And the Board must address evidence that undermines its position. *See TQ Delta, LLC v. CISCO Sys., Inc.,* 942 F.3d 1352, 1357 (Fed. Cir. 2019). But the Board ignored Netlist's extensive evidence of Figure 12's meaning.

III. THE BOARD'S DETERMINATION THAT ELLSBERRY IS PRIOR ART CANNOT BE SUSTAINED

Ellsberry was not even prior art. The '912 patent claims priority to ***two*** Netlist filings that ***each*** antedate Ellsberry's June 1, 2005 filing date—the '436 patent (priority date March 7, 2005), and the '244 provisional application (priority date

May 28, 2004). Appx101. The Board's refusal to accord claim 16 priority to either of those filings cannot be sustained.

A. The Board Clearly Erred in Determining That Netlist's '436 Patent Lacks Written-Description Support for Claim 16

Limitation 16[c] recites a "circuit comprising a logic element and a ***register***." Appx103(3:17-18) (emphasis added). The '436 patent supports that limitation by disclosing "sequential . . . logic." Appx2503(18:3-11). Both parties agreed that "sequential logic" requires "a ***register*** or an equivalent." Appx18693-94(117:16-118:20) (Samsung's expert) (emphasis added); Appx18693(117:19-21) (Samsung's expert: "[s]equential logic" incorporates "logic functions and registers"); Appx18345-46(¶78) (Netlist's expert). The Board nonetheless denied that the '436 patent provides "written description support" for the claimed "register." Appx34. The Board's reasoning defies precedent and logic alike.

1. *The Board's Determination That the '436 Patent Does Not Disclose a "Register" Defies Law and Logic*

A claim is entitled to the priority date of an earlier filing where that earlier filing provides "written description" support for the claim. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571 (Fed. Cir. 1997). A disclosure provides written-description support where it "'allow[s] one skilled in the art to ***visualize or recognize*** the identity of the subject matter . . . described.'" *Alcon Research Ltd. v. Barr Labs., Inc.*, 745 F.3d 1180, 1190-91 (Fed. Cir. 2014) (emphasis added). The disclosure

need not use "the exact terms [as the] claim . . . *in haec verba*"—"***equivalent***" or even broader "language" can be "sufficient." *Nalpropion Pharms., Inc. v. Actavis Labs. FL, Inc.*, 934 F.3d 1344, 1350 (Fed. Cir. 2019) (emphasis added); *see Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357, 1364 (Fed. Cir. 2018).

a. The '436 patent discloses "sequential . . . logic" to generate signals for rank multiplication. Appx2503(18:3-11). That discloses the register. Samsung's expert agreed that "sequential logic" requires a "'register or an equivalent.'" Appx18693-94(117:16-118:20); *see* Appx18693(117:17-21). Netlist's expert similarly testified that "sequential logic" would incorporate a "register." Appx18345-46(¶78). Skilled artisans reading the disclosure of "sequential logic" thus would "visualize or recognize" the claimed "register."

The Board seized on Samsung's expert's testimony that "sequential logic" requires a "register or ***equivalent***." Appx31 (emphasis added). In the Board's view, disclosing sequential logic is insufficient to support the claimed register because sequential logic could incorporate ***equivalent*** "devices ***other than a register***." Appx31 (emphasis added). But "sequential logic" means registers or their equivalents—skilled artisans reading that term will immediately envisage the registers. Indeed, when prompted to explain "sequential logic," Samsung's expert defined it as requiring a "register or equivalent"—with registers as the baseline for equivalency. Appx18693-94(117:16-118:20). Skilled artisans directed to consider

"registers" and their "equivalent[s]" would find it hard to imagine equivalents to a register without first thinking of the register to which they definitionally must be equivalent.

Both experts agreed, moreover, that using registers for sequential-logic functions was commonplace at the time of filing. *See* Appx18693-94(117:16-118:20); Appx18345-46(¶78). "[A] patent need not teach, and preferably omits, what is well known in the art." *Hybritech Inc. v Monoclonal Antibodies, Inc.* 802 F.2d 1367, 1384 (Fed. Cir. 1986). Just as a patent on a lightbulb need not spell out the existence of electricity, the '436 patent did not need to spell out the existence of registers when they are conventional—much less when the "textbook" definition of sequential logic includes registers. Appx18693-95(117:16-119:18).

Besides, to provide written-description support, a disclosure need only use "equivalent language." *Nalpropion*, 934 F.3d at 1350. The '436 patent discloses "sequential logic," which all agree requires a "register"—the term used in claim 16—or devices "equivalent" to registers. Appx18694(118:16-20). It is hard to imagine a clearer example of an earlier filing using "equivalent language." *Nalpropion*, 934 F.3d at 1350. Indeed, *Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357 (Fed. Cir. 2018), makes this an *a fortiori* case. There, the claims recited a "light guide," while the earlier filing referred to a "fibre optics bundle." *Id.* at 1362. It was undisputed that a "'fiber optic bundle' is a ***type*** of light guide." *Id.*

(emphasis added). The earlier filing's use of equivalent language was sufficient to support the claim. *Id.*

The Board's observation that "sequential logic" could potentially refer to devices "other than a register"—so long as they are "equivalent" to registers—is irrelevant. Appx31. An earlier disclosure need not ***rule out*** all embodiments apart from what is claimed. *See, e.g.*, *Hologic*, 884 F.3d at 1358-59; *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1567 (Fed. Cir. 1991). The question is whether the disclosure "'reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date'"—not whether skilled artisans would imagine variations ***other*** than what is claimed. *Hologic*, 884 F.3d at 1361.

b. To reach the opposite result, the Board sleuthed the internet. The Final Written Decision invoked a website the Board accessed in ***2024***—cited nowhere in the trial record—to assert that sequential logic could encompass "other types of devices" besides registers, "such as flip-flops and memory." Appx31; *see* Appx21376. But that reach beyond the record defies the APA: Netlist was entitled to "notice and a fair opportunity to meet the grounds of rejection." *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1301 (Fed. Cir. 2016). The Board cannot conjure a new set of register-substitutes for the first time in its Final Written Decision.

Besides, there is no evidence that the Board's ***2024*** website visit reflects skilled artisans' knowledge as of the '436 patent's ***2005*** filing date. Appx2482; *see*

Appx21376-77. The website at most evidences skilled artisans' knowledge in ***2024***. That is "legally irrelevant" to how skilled artisans would understand the '436 patent's disclosure "as of [its] filing date." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1355 (Fed. Cir. 2010) (en banc).

Skilled artisans, moreover, would understand the '436 patent's disclosure of "sequential logic" to refer to the function of registers, not "flip-flops" or "memory." In the '436 patent, the register is used to store incoming command and address signals so their values can be used to generate additional chip-select signals for rank multiplication. Appx2503(18:6-11). Flip-flops cannot store signal values. The Board's cited website distinguishes "simple" "flip-flops" from "more complex . . . registers." *Sequential Logic Circuits*, https://www.electronics-tutorials.ws/sequential/seq_1.html (accessed Feb. 16, 2025). Moreover, storing signal values to and retrieving them from "memory" would be far too slow for the invention to work. That Netlist had no opportunity to make these points below illustrates why the APA requires notice of "'the matters of fact . . . asserted'" and an opportunity "'to submit rebuttal evidence . . . as may be required for a full and true disclosure of the facts.'" *Dell*, 818 F.3d at 1301 (quoting 5 U.S.C. §§554(b)(3), 556(d)).

2. *The Board's Requirement of a Separate "Logic Element" and "Register" Is Procedurally Improper and Incorrect*

The Board ruled that claim 16—which recites a "circuit" that "comprises a logic element and a register," Appx103(3:17-18)—requires the logic element and

register to be "***two different things***." Appx31 (emphasis added). The Board then ruled that the '436 patent's disclosure was inadequate because, according to the Board, the disclosed register was "included in the logic element." Appx32.

That *sua sponte* claim construction was improper. Petitioner ***never*** argued the logic element and register must be separate components. The Board is not "free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). "Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *Id.* That alone requires reversal. *Id.*

The Board's construction is also wrong. The claimed "circuit" "***comprises*** a logic element and a register." Appx103(3:17-18) (emphasis added). That means that both are part of the same "circuit"—not separate components. *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009). Moreover, the specification—the "'single best guide to the meaning of a disputed term,'" and "[u]sually . . . dispositive," *Phillips*, 415 F.3d at 1315—states that the "logic element" and "register" may be "***portions of a single component***." Appx83(5:37-43) (emphasis added).

That overcomes the Board's effort to infer that the logic element and register must be "different things" because they are recited separately. Appx32. The pre-

sumption that "list[ing] elements separately" implies their separateness is overcome when the specification says otherwise. *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231 (Fed. Cir. 2011). In *Powell*, for example, the claim listed a "cutting box" and "dust collection structure." *Id.* at 1231-32. Because the specification taught "the cutting box may also function as a 'dust collection structure,'" however, this Court concluded that the cutting box and dust collection structure need not be "separate components." *Id.* Similarly, in *Linear Technology Corp. v. ITC*, 566 F.3d 1049 (Fed. Cir. 2009), the Court concluded that the claimed "second circuit" and "third circuit" need not be "completely distinct," because the specification depicted embodiments where they "share[d] common components." *Id.* at 1055. Likewise here, the specification's statement that the "logic element" and "register" may be "portions of a single component" overrides any inference that the claim requires separate components. Appx83(5:37-43).

Regardless, the '436 patent discloses a "logic element" that is separate from the "register." Appx31. It was undisputed that the '436 patent discloses "sequential . . . logic." Appx2503(17:41-45; 18:6-11). Samsung's expert conceded "sequential logic" necessarily requires two distinct components—"***both*** . . . a register or an equivalent, ***plus*** . . . logic functions." Appx18694(118:16-20) (emphasis added). Even if claim 16 requires the "logic element" and "register" to be "different things," Appx31-32, the '436 patent teaches that.

3. *The Board's Ruling Defies Precedent and the APA*

The Board also asserted that Netlist failed to show written-description support for claim 16 by addressing only "disputed" limitations, rather than "all of the limitations." Appx32-33. That defies precedent. When the patentee "attempts to antedate an asserted prior art reference" in an IPR, the patentee has a "burden of production" to produce evidence to support priority. *Medtronic, Inc. v. Teleflex Innovations S.À.R.L.*, 68 F.4th 1298, 1303 (Fed. Cir. 2023). "Once that burden is met," the "burden shifts back to the petitioner"—and the "burden of persuasion" always rests with petitioner. *Id.*

The Board has interpreted that burden-shifting framework to require patentees to address ***only*** "the specific points and contentions raised" in the petition. *Lupin Ltd. v. Pozen, Inc.*, IPR2015-01775, Paper 15, at 10-11 (PTAB Mar. 1, 2016); *Fitbit, Inc. v. BodyMedia, Inc.*, IPR2016-00707, Paper 9, at 10-11 (PTAB Sept. 8, 2016); *Mission Integrated Techs., LLC v. Clemente*, No. IPR2023-01285, 2024 WL 752892, at *8 (PTAB Feb. 23, 2024); *Lumi Legend Corp. v. Manehu Prod. All., Inc.*, PGR2024-00014, 2024 WL 3656822, at *4 (PTAB Aug. 5, 2024). The ***petitioner*** must "identify[], specifically" how the prior disclosure "allegedly lack[s] §112 support for the claims," and the patentee need only respond to those points. *Lupin*, *supra*, at 11.

The Board's assertion that Netlist had to address "all of the limitations of claim 16," Appx33, defies the Board's own precedent. The Board's failure to follow its "established precedent" (or articulate any reason for departure) violates the APA and requires vacatur. *Jicarilla*, 613 F.3d at 1119.

B. Netlist Also Was Entitled to the Priority Date of the '244 Provisional Application

Limitation 16[c] recites a "logic element receiving . . . input signals comprising . . . ***bank address signals***." Appx103(3:18-21) (emphasis added). The '244 provisional discloses a decoder that receives "control signal[s]." Appx2338(¶5); Appx2342. And bank address signals undisputedly are "control signal[s]" in the JEDEC standard. Appx173; Appx18315-19(¶¶62-64); Appx11193. The provisional thus discloses receipt of bank address signals.

1. The Board found that insufficient to disclose bank address signals because there were "other types of DRAM devices" besides JEDEC-compliant devices. Appx30. But skilled artisans "interpret[]" patent-application disclosures in view of industry "standard[s]." *Wellman*, 642 F.3d at 1367-68. Skilled artisans thus would have read the '244 provisional's disclosure of "control signals" in view of JEDEC standards. Indeed, "'90%'" of DRAM devices comply with JEDEC standards. Appx1263. And the '244 provisional uses "specific terminology" indicating a "JEDEC-style memory module." Appx18313-14(¶60). It refers to JEDEC chip-select signals, "CS0" and "CS1," and uses the term "rank," which was

created by JEDEC. Appx18313-14(¶60). The '244 provisional's first paragraph also refers to memory modules used in "personal computer[s]," which Samsung's expert conceded would refer to JEDEC-compliant "DDR2 or DDR device[s]." Appx18649(73:9-15).

Samsung, moreover, conceded that "JEDEC standard[s]" specify "control" signals that "include[] bank address signals." Appx176; *see* Appx18315-16(¶63). The standards provide for key commands to include bank address signals. Appx11277. Indeed, Samsung conceded that basic operations like "read" and "write" could not be performed without bank address signals. Appx173-74; *see* Appx1202. Skilled artisans thus would have read the '244 provisional's "control" signals to include bank address signals. The Board did not meaningfully consider that evidence, requiring vacatur. *Lee*, 277 F.3d at 1344. So does its unexplained failure to "interpret[]" disclosures in provisional applications in view of industry "standard[s]." *Wellman*, 642 F.3d at 1367-68.

The Board's assertion that Netlist was "infer[ring]" that skilled artisans would consider the standard in reading the '244 provisional, Appx30, is no answer. That simply is the law. *See Wellman*, 642 F.3d at 1367-68. And if the Board thought skilled artisans would have done otherwise here the Board had to provide reasoned analysis explaining why. *Power Integrations, Inc. v. Lee*, 797 F.3d 1318, 1323 (Fed. Cir. 2015). It did not.

2. The Board identified five steps it deemed a "speculative" "chain" of inferences. Appx29-30. But four of those five were effectively undisputed.[3] A single step is not a "chain," and one disputed step is not a "speculative" chain. *Lee*, 277 F.3d at 1344-45.

The ***only*** disputed step was whether skilled artisans would "infer that the bank address signals are used for rank multiplication." Appx30. But claim 16 does not recite that the bank address signals are "used for rank multiplication." It is more precise: The bank address must be among the "set of input signals" received by the "logic element," which "generat[es] a set of output signals in response to the set of input signals." Appx103(3:17-37). Figure 1 of the '244 provisional depicts just that: Control signals (necessarily including bank address signals) are communicated to the "Decoder" (claim 16's "logic element"), and modified output signals are transmitted to DRAM devices. Appx2339(¶¶9-10); Appx2344. The Board also ignored that bank address signals were "well known in the art," and thus did not need to be disclosed. *Hybritech*, 802 F.2d at 1384. Regardless, the '244 provisional discloses that "control signals"—which inherently include bank address signals in

[3] Those were: (1) "that the '244 provisional pertains to DDR memory modules" (not reasonably disputed, *see* pp. 63-65, *supra*); (2) "that DDR DRAMs use bank address signals according to the JEDEC standards" (undisputed); (3) "that bank address signals are not mentioned in the '244 provisional" (undisputed, and indeed the premise of the debate); and (4) "that bank address signals would be included as part of the control signals" (undisputed).

JEDEC-standard memory modules—are used as "[i]nput [s]ignals" for rank-multiplication. Appx2340(¶11); *see* Appx2340-41(¶19); Appx2341-42(¶23).

C. Vacatur Is Required for Additional Reasons

The Board can find claims unpatentable in an IPR "only on the basis of prior art consisting of ***patents or printed publications***." 35 U.S.C. §311(b) (emphasis added). Ellsberry never issued as a "patent." And because it was not published until ***after*** the challenged patent's critical date, Appx11884, it was not a prior-art "printed publication" that the Board could invoke in this IPR proceeding. Appx995-97; Appx1000. Because the Board relied solely on Ellsberry, its decision must be vacated. While *Lynk Labs, Inc. v. Samsung Elecs. Co.*, 125 F.4th 1120 (Fed. Cir. 2025), currently forecloses this argument, Netlist preserves it for further review. Likewise, for issue-preservation purposes, Netlist urges that *Thryv Inc. v. Click-to-Call Technologies LP*, 590 U.S. 45 (2020), should be reconsidered.

CONCLUSION

The Board's decision should be reversed or vacated.

February 18, 2025

Respectfully submitted,

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ADDENDUM

ADDENDUM TABLE OF CONTENTS

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571-272-7822

Paper 96
Entered: April 17, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
Dismissing Patent Owner's Motion to Submit Supplemental Information
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners in this proceeding. *See* Paper 58.

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claim 16 ("challenged claim") of U.S. Patent 7,619,912 C1 (Ex. 1001, "the '912 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7) to the Petition. Samsung filed an authorized Preliminary Reply (Paper 14), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 15). The Board instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 20 ("Institution Decision" or "Inst. Dec.").

Patent Owner requested Rehearing and Precedential Opinion Panel review of the Institution Decision. Paper 25. While that request was pending, the Board authorized Patent Owner to file a motion seeking additional discovery on the issue of whether Google was a real party in interest, which would bar the Petition under 35 U.S.C. § 315(b). Paper 32. Patent Owner then filed the Motion for Additional Discovery (Paper 34), Petitioner opposed (Paper 36), and Patent Owner replied in support of its Motion (Paper 37).

The Director granted *sua sponte* review (Paper 38) of the Institution Decision, entered a stay of the proceeding, and dismissed the Request for Rehearing and Precedential Opinion Panel Review (Paper 39). The Director then issued a Decision (Paper 40) denying Patent Owner's Request for Rehearing, granting-in-part and denying-in-part Patent Owner's Motion for Additional Discovery, lifting the stay, and remanding the case to the panel for further proceedings consistent with the Director's Decision.

We entered an Order for Petitioner to complete the additional discovery as authorized by the Director, and for the parties to propose a briefing schedule for the additional discovery. Paper 42. Petitioner filed the authorized additional discovery as exhibits and a Summary of Responses to the Additional Discovery (Paper 46) along with a Motion to Seal (Paper 43), which we granted (Paper 49). We then authorized a schedule for the parties to brief the applicability of the additional discovery to the issue of whether Google was a real party in interest and the Petition thus time-barred under 35 U.S.C. § 315(b). Papers 51–57. After consideration of the evidence, we determined by Order on Remand from the Director (Paper 62 (parties and Board), Paper 64 (public)) that Google was not a real party in interest and that this proceeding thus was not time-barred.

After briefing on the additional discovery but before our Order on Remand from the Director, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("the Micron entities") filed a petition and requested joinder to this proceeding. IPR2023-00203, Papers 1, 3. We granted the Micron entities' petition for *inter partes* review and joined them as parties on the petitioner side of this case. *Id.* at Paper 8. A copy of that institution decision was entered in this proceeding. Paper 58. We refer to Samsung and the Micron entities together as "Petitioner" in this Decision.

Under authority delegated by the Director, due to the joinder, we adjusted the one-year period for issuing the Final Written Decision to April 19, 2024 and modified the due dates applicable to this proceeding. Paper 63.

During the trial, Patent Owner filed a Response (Paper 67) ("PO Resp."), Petitioner filed a Reply (Paper 77) ("Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 80) ("PO Sur-Reply").

Patent Owner also requested authorization to submit supplemental information from parallel litigation concerning the deposition of Micron's corporate representative who had allegedly taken inconsistent positions impacting the merits of this *inter partes* review. Ex. 3017. We issued an Order (Paper 71) authorizing Patent Owner to file a Motion to Submit Supplemental Information. Patent Owner filed the Motion (Paper 72), Petitioner opposed (Paper 75), and Patent Owner replied in support of its Motion (Paper 76). We dismiss Patent Owner's Motion to Submit Supplemental Information for reasons explained later in this Decision.

Patent Owner then contended that Petitioner's Reply contained new arguments, and Petitioner contended that Patent Owner's Sur-Reply contained new arguments, and each requested authorization to file a motion to strike new arguments in the other's briefing. Ex. 3020. We denied these requests (*id.*) but permitted the parties to file one-page statements identifying new arguments in the other party's briefings, which they did. Papers 86 and 87.

Petitioner and Patent Owner requested oral argument. Papers 84 and 85. A hearing was conducted on January 31, 2024, and the transcript is in the record. Paper 95.

Petitioner objected to evidence (Papers 45, 68, 83) and filed a Motion to Exclude (Paper 89). Patent Owner opposed Petitioner's Motion to Exclude (Paper 90), then amended its opposition (Paper 91), and Petitioner replied (Paper 92) in support of its Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claim is unpatentable.

B. Real Parties in Interest

Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC are the identified real parties in interest on the petitioner side. Pet. 1; IPR2023-00203, Paper 3, 1.

Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

C. Related Matters

The parties advise that the '912 patent is related to the following pending matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:21-cv-00293 (E.D. Tex. filed Aug. 1, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00294 (E.D. Tex. filed Aug. 1, 2022)
- *Netlist, Inc. v. Google LLC*, 3:09-cv-05718 (N.D. Cal. filed Dec. 4, 2009)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2023-00203 (PTAB filed Nov. 18, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454 (U.S. Patent 11,093,417)

- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00455 (U.S. Patent 9,858,215)
- U.S. Patent Application No. 17/403,832.

Petitioner contends that the '912 patent is related to the following matters, which are no longer pending:

- *Netlist, Inc. v. Inphi Corporation*, No. 2-09-cv-06900 (C.D. Cal. filed September 22, 2009)
- *Inter Partes* Reexamination 95/000,578 (U.S. Patent 7,619,912);
- *Inter Partes* Reexamination 95/000,579 (U.S. Patent 7,619,912);
- *Inter Partes* Reexamination 95/001,339 (U.S. Patent 7,619,912)
- *Inter Partes* Reexamination 95/000,546 (U.S. Patent 7,289,386)
- *Inter Partes* Reexamination 95/000,577 (U.S. Patent 7,289,386)
- *Inter partes* Reexamination 95/001,337 (U.S. Patent 7,636,274)
- IPR2014-00882 (U.S. Patent 7,881,150)
- IPR2014-00883 (U.S. Patent 8,081,536)
- IPR2015-01021 (U.S. Patent 8,081,536)
- IPR2017-00549 (U.S. Patent 8,756,364)
- IPR2017-00667 (U.S. Patent 7,532,537)
- IPR2017-00668 (U.S. Patent 7,532,537)

Paper 79, 2–3 (Petitioner's Updated Mandatory Notices); Paper 81, 1–2 (Patent Owner's Third Updated Mandatory Notice).

D. Overview of the '912 Patent (Ex. 1001)

The '912 patent is titled "Memory Module Decoder" and is directed to a memory module that is connectable to a computer system. Ex. 1001, codes (54), (57). Figure 1A of the '912 patent is reproduced below.

Figure 1A:

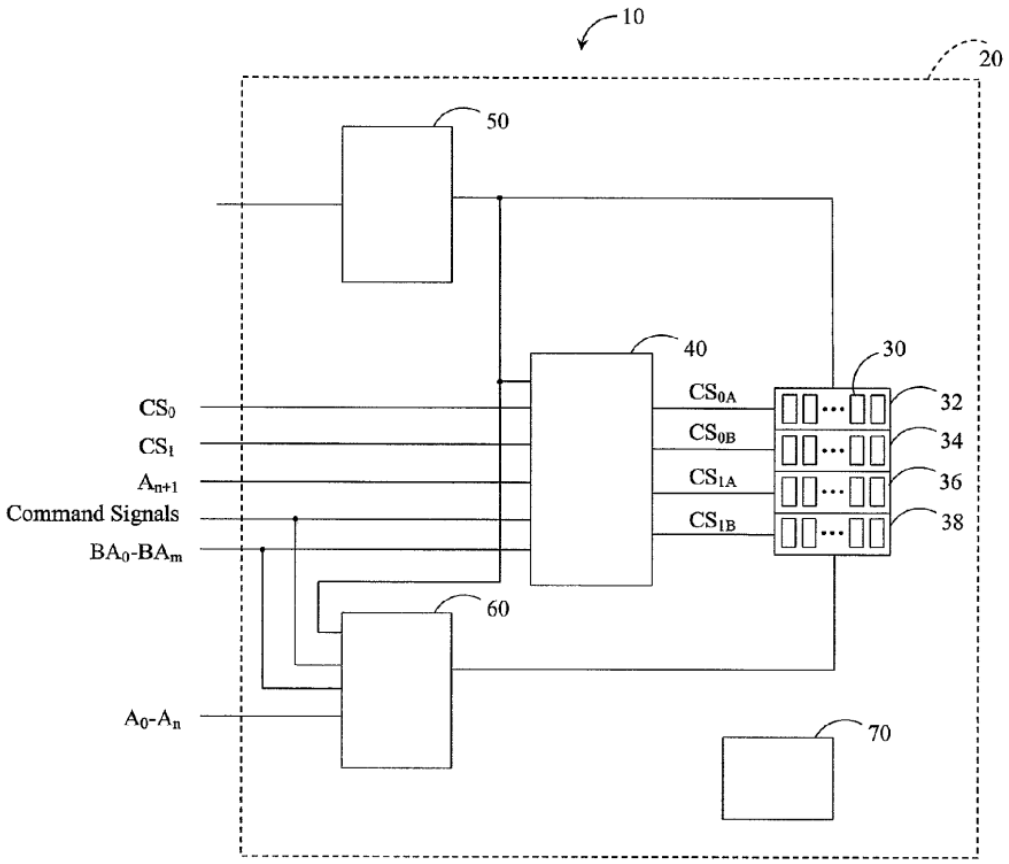


Figure 1A shows a memory module 10 with printed circuit board 20 and memory devices 30 connected to the printed circuit board. *Id.* at 5:9–11. Memory devices 30 are arranged in ranks 32, 34, 36, 38. *Id.* at 22:35–37. The memory devices 39 may be double-data rate (DDR) dynamic random-access memory (DRAM) devices. *Id.* at 6:12–16. The memory module 10 further comprises logic element 40 coupled to the printed circuit board 20. *Id.* at 5:13–14. Logic element 40 receives a set of input control signals and

generates output control signals for select memory devices 30. *Id.* at 5:14–21. Phase-lock loop device 50 and register 60 are also mounted on printed circuit board 20. *Id.* at 5:25–27. The phase-lock loop device 50 generates clock signals to memory devices 30, logic element 40, and register 60. *Id.* at 5:28–31. Register 60 receives and buffers control signals including address signals, and transmits corresponding signals to appropriate memory devices 30. *Id.* at 5:31–36.

In Figure 1A, logic element 40 receives a set of input control signals from the computer system that include chip-select signals CS_0–CS_1, address signal A_{n+1}, and bank address signals BA_0–BA_m. *Id.* at 7:35–53. To the computer system, the memory module has only two ranks selectable with either CS_0 or CS_1. *Id.* at 6:55–7:19. However, logic element 40 generates a set of output control signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} corresponding to the four ranks 32, 34, 36, 38 of memory devices 30. *Id.* at 6:61–63. Logic element 40 also receives command signals (e.g., read or write) from the computer system and transmits the command signal to memory devices on the selected rank of the memory module. *Id.* at 6:55–61, 7:43–53.

E. Claim 16 of the ’912 Patent

Claim 16 of the ’912 patent is an independent claim, and the only claim that is challenged in this proceeding. Claim 16 is reproduced below with Petitioner’s identifiers shown in bold brackets.

> **[16.pre]** A memory module connectable to a computer system, the memory module comprising:
>
> **[16.a]** a printed circuit board;
>
> **[16.b]** a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, **[16.b.i]** the plurality

of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

[16.c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, **[16.c.i]** the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal**, [16.c.ii]** the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, **[16.c.iii]** the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, **[16.c.iv]** wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

[16.d] a phase-lock loop device coupled to the printed circuit board, **[16.d.i]** the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

[16.e] wherein the command signal is transmitted to only one DDR memory device at a time.

Ex. 1001, *Inter Partes* Reexamination Certificate, 3:9–43.

A. Evidence

Petitioner relies on the following references:

Reference		Date	Exhibit No.
Perego-422[2,3]	US 7,363,422 B2	Apr. 22, 2008	1035
Amidi[4]	US 2006/0117152 A1	Jun. 1, 2006	1036
Ellsberry[5]	US 2006/0277355 A1	Dec. 7, 2006	1037

Pet. 4, 14–22.

Petitioner further relies upon the Declaration of Dr. Andrew Wolfe (Ex. 1003). Patent Owner relies on the Declaration of Dr. Michael C. Brogioli (Ex. 2062). The parties deposed each other's experts and rely on those depositions in their arguments (Ex. 1101; Ex. 2103). The parties submitted other evidence into the record, which we will address herein as necessary.

[2] Although the Petition refers to this reference as "Perego," we refer to it as "Perego-422" to distinguish it from another reference of record by the same inventor, U.S. Patent 7,356,639 ("Perego-639") (Ex. 1061).

[3] Petitioner contends that Perego-422 is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 14.

[4] Petitioner contends that Amidi is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 18.

[5] Petitioner contends that Ellsberry is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 20.

B. Asserted Challenges to Patentability

Ground	Claim Challenged	35 U.S.C. §	Reference(s)/Basis
1	16	§ 103(a)	Perego-422
2	16	§ 103(a)	Perego-422, Amidi
3	16	§ 103(a)	Ellsberry

Pet. 4.

II. ANALYSIS

A. Principles of Law

In an *inter partes* review, a petitioner bears the burden of persuasion to prove "unpatentability by a preponderance of the evidence." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)); *see* 37 C.F.R. § 42.1(d) (2021).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Env't Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.* at 696–97.

Petitioner contends that a person of ordinary skill in the art ("POSITA") in the field of memory module design in 2004 or 2005 would have an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 5. Petitioner contends such person would have been familiar with various standards of the day, including JEDEC industry standards, and would have been knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* at 6.

Patent Owner applies the skill level of a POSITA proposed by Petitioner for this proceeding. PO Resp. 4.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifiers "at least" before years of education and experience because they render the level ambiguous

and may encompass levels that are beyond ordinary. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '912 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

C. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a POSITA in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner contends that "rank" refers to "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module." Pet. 12 (citing Ex. 1003 ¶ 74).

Patent Owner argues that "rank" should be construed as "a predetermined set of DRAMs on a memory module that act together to send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DRAMs on the memory module." PO Resp. 4.

Patent Owner argues that the parties' dispute over claim construction can be narrowed to the following issue: "whether 'rank' can include just 'one memory device.'" *Id.* Petitioner agrees that this is the dispositive issue for claim construction. Pet. Reply 1. For the following reasons, we determine that the intrinsic evidence of the '912 patent shows that the claim term "rank" may include only one memory device.

Starting with the intrinsic evidence, we begin our analysis by observing that claim 16 of the '912 patent recites "a plurality of double-data-rate (DDR) memory devices." Ex. 1001, 3:13–14 (reexamination certificate). The claim further recites "a first number of DDR memory devices arranged in a first number of ranks" and "a second number of DDR memory devices arranged in a second number of ranks." *Id.* at 3:15–16, 3:23–24 (reexamination certificate). The only restrictions in the claim on the first and second numbers of memory devices and ranks are that "the second number of DDR memory devices [is] smaller than the first number of DDR memory devices" and "the second number of ranks is less than the first number of ranks." *Id.* at 3:25–28 (reexamination certificate). Hence, the

language of claim 16 does not preclude the possibility that a rank could have a single memory device.

Claim 55 of the '912 patent depends from claim 1 and recites "each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages." *Id.* at 5:56–59 (reexamination certificate); *see also* Pet. Reply 7. This implies that each of the ranks recited in claim 1 could include a single memory device. Ex. 1001, 1:29–31 (reexamination certificate). Otherwise, the limitation would be superfluous. Claim 55 informs how "rank" should be understood in claim 16.

The specification of the '912 patent similarly describes its memory module without restriction on the specific number of memory devices that can be included in each rank (except that the second number of memory devices or ranks must be less than the first number of memory devices or ranks). *Id.* at 3:3–14 (summary), 6:64–7:18.

During the trial, the parties disputed at length the meaning of the "Logic Tables" section of the '912 patent. *Id.* at 7:55–9:21; Pet. 12–13; PO Resp. 6–10; Pet. Reply 9–10. The disputed paragraph from this section is shown below.

> The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. *In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory* devices

> *to ensure that the memory content of the memory devices remains valid over time.* Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Ex. 1001, 8:44–64 (emphasis added). Patent Owner argues that the '912 patent consistently describes memory devices as part of multi-device ranks and thus that a POSITA would understand this passage as referencing a memory module with at least two ranks, each rank having at least two memory devices. PO Resp. 7 (citing Ex. 1001, 6:31–38, 20:64–65, 22:34–35; Figs. 1A, 1B, 2A, 3A; Ex. 2062 ¶¶ 106–107). Petitioner contends that the language emphasized in the block quoted paragraph above means that the selected rank has only one memory device. Pet. Reply 9–10 (citing Ex. 1001, 8:48–60; Ex. 1100, 11–12; Ex. 1098/2063, 5–6).

The disputed paragraph may be better understood with reference to Table 1, shown below, and Figure 1A (*see* § I.D).

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1

TABLE 1-continued

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.

2. A_{n+1} is an active high signal.

3. 'x' is a Don't Care condition.

4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

Ex. 1001, 7:60–8:18.

In Table 1, states 1, 2, 4, 5 select only one rank with chip select signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}, which are active low ("0") and inactive high ("1"). *See id.* at 8:19–42 (describing what is selected in each logic state). States 3 and 6, however, pair the ranks together so that when CS_{0A} and CS_{0B} are activated, CS_{1A} and CS_{1B} are deactivated, and vice versa. States 3 and 6 permit two smaller memory devices to emulate a larger one.

The first two emphasized sentences above (*id.* at 8:47–54) could be interpreted both as Petitioner and Patent Owner propose. Under Patent Owner's interpretation, the "selected rank" includes the "one memory device or the other memory device" each in multi-device ranks. Under Petitioner's interpretation, the "selected rank" may be the one memory device connected to C_{S1A} of the pair of memory devices connected to chip select signals CS_{1A} and CS_{1B}.

However, the subsequent emphasized sentences (*id.* at 8:54–60) could only be understood in favor of Petitioner's interpretation. If "the command signal is passed through to both associated ranks" and "the command signal is sent to both memory devices," each rank must have only one memory device. Thus, we agree with Petitioner that this passage means that a rank may have only one memory device.

Patent Owner argues that this paragraph of the '912 patent (*id.* at 8:44–64) must be read in conjunction with its Figures which show multiple memory devices per rank. PO Resp. 7 (citing Ex. 1001, 6:31–38, 20:64–65, 22:34–35, Figs. 1A, 1B, 2A, 3A; Ex. 2062 ¶¶ 106–107). However, the disputed paragraph refers to "certain embodiments" which do not necessarily correspond exactly to what the Figures depict, and the Figures are described as "exemplary" and "compatible with" or "in accordance with certain embodiments described herein." *See, e.g.*, Ex. 1001, 3:32–48. We find no statement here or elsewhere in the '912 patent that a rank must include multiple memory devices, and cannot include a single memory device.

The "Back-to-Back Adjacent Read Commands" section of the '912 patent provides another example of single-device ranks. Ex. 1001, 23:26–25:67; *see* Pet. Reply 7–13. This section relates to solving a problem that occurs when back-to-back read commands cross the memory boundaries between ranks of memory devices, and memory controllers must take measures to avoid data collisions or interference. Ex. 1001, 23:60–67. Back-to-back adjacent read commands are referred to as "BBARX" in the '912 patent. *Id.* This section explains that the circuit of Figure 6B of the '912 patent uses isolation device 120 to avoid collisions between memory

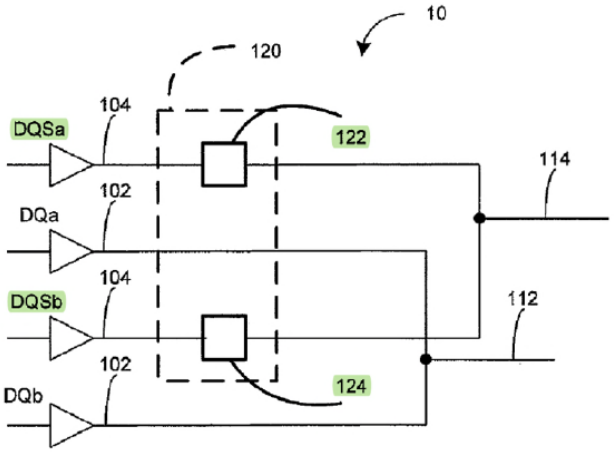
devices "a" and "b" of different ranks. *Id.* at 24:1–58. This section thus supports that a rank may have only one memory device.

The '912 patent provides Examples 1 and 2 of Verilog code relating to the operation of field-effect transistor (FET) switches used to avoid conflicts during back-to-back read operations (which the '912 patent refers to as "BBARX"). *Id.* at 14:24–20:53, 23:60–67. Patent Owner argues that Example 2 of this code shows that FET switches are used to send a command to a single memory device in a rank of multiple memory devices and shows that the ranks discussed in the "Logic Tables" section of the '912 patent include multiple memory devices. PO Resp. 26 (citing Ex. 1003 ¶¶ 36–43). Petitioner disagrees, contending that code relates to FET switches on the DQS[6] strobe lines, not the command lines, and thus does not relate to the "Logic Tables" section which discusses the command signal, not the DQS strobe lines. Pet. Reply 11–13.

We agree with Petitioner that the Verilog code of Example 2 relates to enabling and disabling FET switches on the DQS strobe lines, not the command lines. Petitioner provides an annotated version of Figure 6B shown below.

[6] The JEDEC DDR standards refer to data signals as "DQ", data strobe signals as "DQS", control signals as "RQ", and clock signal as "CK". Pet. 30 (citing Ex. 1003 ¶ 124).

Figure 6B:



Id. at 11 (citing Ex. 1001, 24:39–58, Fig. 6B). Figure 6B shows isolation device 120 connected between logic element 40 and memory devices 30 (e.g., memory devices "a" and "b"). Ex. 1001, 3:65–67, 24:1–58. Isolation device 120 comprises switches 122, 124 (e.g., FETs), which control when respective DQSa and DQSb strobe signals are output to memory devices "a" and "b" on common strobe line 114. *Id.* at 24:31–38.

Petitioner also provides an annotated version of an excerpt from Example 2 of the Verilog code at Exhibit 1001, 19:1–53, shown below:

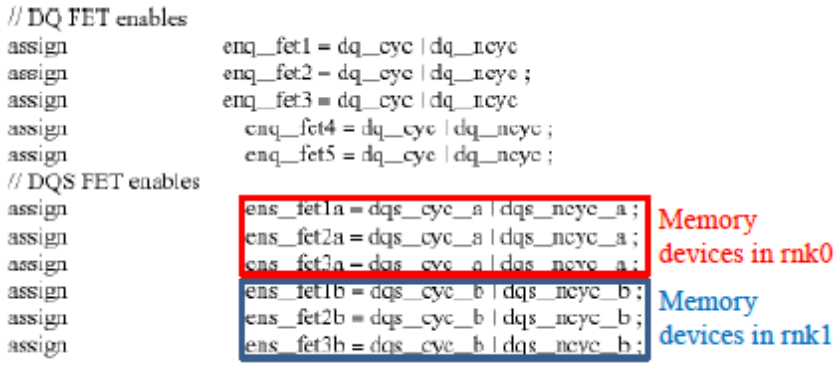
```
always @(posedge clk_in)
 begin
 if (
    (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
  | rd0_o_R3                                                // 1st cyc of rd brst
  | rd0_o_R4                                                // 2nd cyc of rd brst
  | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
  | (wr0_o_R1)                                              // pre-am wr
  | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
  | (wr0_o_R4)                                              // post-wr cyc (chgef9)
  | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1 (chgef9)
   )
                en_fet_a <= 1'b1;                           // enable fet
 else
                en_fet_a <= 1'b0;                           // disable fet
 end
```

Pet. Reply 13. Petitioner contends that the code highlighted in green indicates when to enable/disable the same FET switches on the DQS strobe lines (not the command lines) to switch the strobe line between data bursts, as stated in the comments section of the code, to avoid problems due to BBARX. *Id.* at 12–13. The highlighted code is followed on the same lines by comments "//1st cyc of rd brst" and "//2nd cyc of rd brst" which refer to a first read cycle followed by a second read cycle, i.e., which is a BBARX situation that presents the possibility of a collision of DQS data strobe signals for the memory devices 'a' and 'b' sharing common strobe line 114 shown in the '912 patent's Figure 6B above. The code stating "en_fet_a <= 1'b1" and "en_fet_a <= 1'b0" refers to enabling and disabling, respectively, the FET 122 for the DQS signal for memory device 'a' shown in Figure 6B. Ex. 2062 ¶ 40. From inspection of Figure 6B and the code of Example 2, we agree with Petitioner that the code of Example 2 relates to enabling and disabling a FET 122 on the DQS data strobe line, not the command line discussed in the "Logic Tables" section of the '912 patent.

Dr. Brogioli offers testimony explaining the Verilog code in the '912 patent and, specifically, contrasting Verilog code Examples 1 and 2. Ex. 2062 ¶¶ 36–43. Dr. Brogioli testifies that, in Example 2, "[s]ignal 'en_fet_a' is used to enable or disable the FET switch for memory device 'a' in physical rank 0 (rnk0), and 'en_fet_b' is used to enable or disable FET switch for memory device 'b' from physical rank 1 (rnk1)." *Id.* ¶ 40. According to Dr. Brogioli, "[b]y providing for the selective enabling or disabling of the FET switch associated with memory device 'a' or memory device 'b,' Example 2 teaches how to transmit a command to a single memory device on a physical rank of multiple memory devices." *Id.*

> Dr. Brogioli testifies that
>
> Example 1 provides for the generation of ***multiple*** control signals to control ***multiple*** DQS signals from ***multiple*** memory devices in each rank. This is achieved by using multiple FET switches: fet1a, fet2a, and fet3a to control DQS signals from three different memory devices belonging to the same physical rank (rnk0); and fet1b, fet2b, and fet3b to control DQS signals from 3 different memory devices belonging to the same physical rank (rnk1).

Id. ¶ 42. Dr. Brogioli annotates a portion of the Verilog Example 1 as shown below.



Id. In the annotated Verilog code above, Dr. Brogioli notes that the code for fet1a, fet2a, and fet3a corresponds to "Memory devices in rnk0" and that the code for fet1b, fet2b, and fet3b corresponds to "Memory devices in rnk1."

Id. Dr. Brogioli opines that

> Example 1 teaches enabling or disabling the DQ and DQS lines for a plurality of memory devices in each corresponding rank, not a single memory device. But as explained above, Example 2, teaches selectively enabling or disabling of the FET switch associated with memory device "a" or memory device "b" in each corresponding rank.

Id. ¶ 43.

Even if we were to accept Dr. Brogioli's testimony that the FETs control transmission of commands (*id.* ¶ 40), we do not agree with

Dr. Brogioli's conclusion that Example 2 involves multiple memory devices in each rank. As his testimony for Example 1 makes clear, the Verilog code specifically identifies multiple FETs when there are multiple memory devices in each rank. *Id.* ¶ 42. Example 2, however, identifies commands for two FETs, which Dr. Brogioli acknowledges are in separate ranks. *Id.* ¶ 40. Thus, "en_fet_a" would appear to pertain to memory device a, which is the memory device of rank 0 just as "en_fet_b" pertains to memory device b, which is the memory device of rank 1. Dr. Brogioli does not identify Verilog code in Example 2 that controls other memory devices in each rank, suggesting that Example 2 pertains to single-device ranks, as opposed to Example 1. Thus, we find the Verilog code in the '912 patent supports Petitioner's position that a rank may be only one device.

We previously explained that the prosecution history of the examination and reexamination do not elucidate the proper construction of "rank." Inst. Dec. 31–32. Nothing that has transpired during the trial changes our view of the prosecution history.

We consider claim constructions from district courts in our analyses if they are timely made of record. 37 C.F.R. § 42.100(b). Petitioner contends that the District Court for the Eastern District of Texas considering the '912 patent and its related '215 patent concluded that "rank" can include a single memory device. Paper 79, 2 (Petitioner's Updated Mandatory Notices) (citing Ex. 1117, 11–14). This is consistent with our discussion of the intrinsic record above.

Based on the foregoing, we conclude that "rank" as used in the '912 patent can include only "one memory device." Because the intrinsic record is clear, we need not resort to extrinsic evidence to determine the scope of

the term "rank." *See Seabed Geosolutions (US) Inc. v. Magseis FF LLC*, 8 F.4th 1285, 1287 (Fed. Cir. 2021) ("If the meaning of a claim term is clear from the intrinsic evidence, there is no reason to resort to extrinsic evidence."); *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1367 (Fed. Cir. 2003) ("When an analysis of *intrinsic* evidence resolves any ambiguity in a disputed claim term, it is improper to rely on extrinsic evidence to contradict the meaning so ascertained."); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (*en banc*) (noting that extrinsic evidence is "in general . . . less reliable than the patent and its prosecution history in determining how to read claim terms"). With this construction, we proceed to address the challenge grounds asserted by Petitioner.

D. Obviousness of Claim 16 Over Ellsberry (Ground 3)

We now address the parties' contentions concerning whether Ellsberry is prior art to the '912 patent under their respective priority dates and whether Ellsberry qualifies as a "printed publication"; and Petitioner's contention that Ellsberry teaches or suggests each limitation of claim 16. We conclude that claim 16 is obvious notwithstanding Patent Owner's arguments to the contrary.

1. Priority

Petitioner bears the initial burden of production on priority. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2015). Petitioner satisfies that burden by arguing that Ellsberry, having publication and filing dates before the filing date of the '912 patent, renders claim 16 of the '912 patent obvious under § 103(a). *Id.*; Pet. 63–111. The burden of production on the issue of priority then shifts to Patent Owner to show that Ellsberry is not prior art. *Dynamic Drinkware*, 800 F.3d at 1380.

Patent Owner must show that each application in a priority chain leading back to an application predating Ellsberry complies with the written description requirement of § 112 and reasonably conveys to those skilled in the art that the inventors had possession of the subject matter of claim 16 as of the earlier filing date. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571 (Fed. Cir. 1997); *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Patent Owner does not satisfy its burden of production for the reasons that follow.

The '912 patent was filed on September 7, 2007, as U.S. Application 11/862,931 ("the '931 application"), and issued November 17, 2009. Ex. 1001, codes (21), (22), 1:3–16. The '912 patent indicates that it is a continuation of U.S. Application 11/173,175, filed on July 1, 2005, which issued as U.S. Patent 7,289,386 ("the '386 patent"). *Id.* at code (63). The '386 patent claims priority to U.S. Provisional 60/588,244 ("the '244 provisional"), filed July 15, 2004. *Id.* at code (60), 1:6–11.

The '912 patent further indicates that the '386 patent is a continuation-in-part of U.S. Application 11/075,395, filed March 7, 2005, which issued as U.S. Patent 7,286,436 ("the '436 patent"). *Id.* at code (63), 1:11–13. The '436 patent claims priority to U.S. Provisional 60/550,668 ("the '668 provisional") filed March 5, 2004, and U.S. Provisional 60/575,595 ("the '595 provisional") filed May 28, 2004. *Id.* at code (60).

Petitioner contends that the '668, '595, and '244 provisionals and the '436 patent do not provide written description support under § 112 ¶ 1 for claim 16 of the '912 patent. Pet. 63–69. Accordingly, Petitioner contends that the priority date for the '912 patent is July 1, 2005. *Id.* at 20–21. Ellsberry was filed on June 1, 2005 as U.S. Application 11/142,989.

Ex. 1037, codes (21), (22). Petitioner contends that Ellsberry constitutes prior art to claim 16 of the '912 patent under §§ 102(a) and (e) and that Ellsberry renders claim 16 obvious under § 103(a). Pet. 20–21 (citing *id.* at § VI.B.1; Ex. 1003 ¶¶ 189–196).

More specifically, Petitioner contends that the '668 and '595 provisionals do not disclose the claimed "logic element" or that such a "logic element" receives "at least one row/column address signal, bank address signals, and at least one chip-select signal." *Id.* at 63 (citing Ex. 1003 ¶ 189). Patent Owner does not dispute Petitioner's contentions concerning the '668 and '595 provisionals.

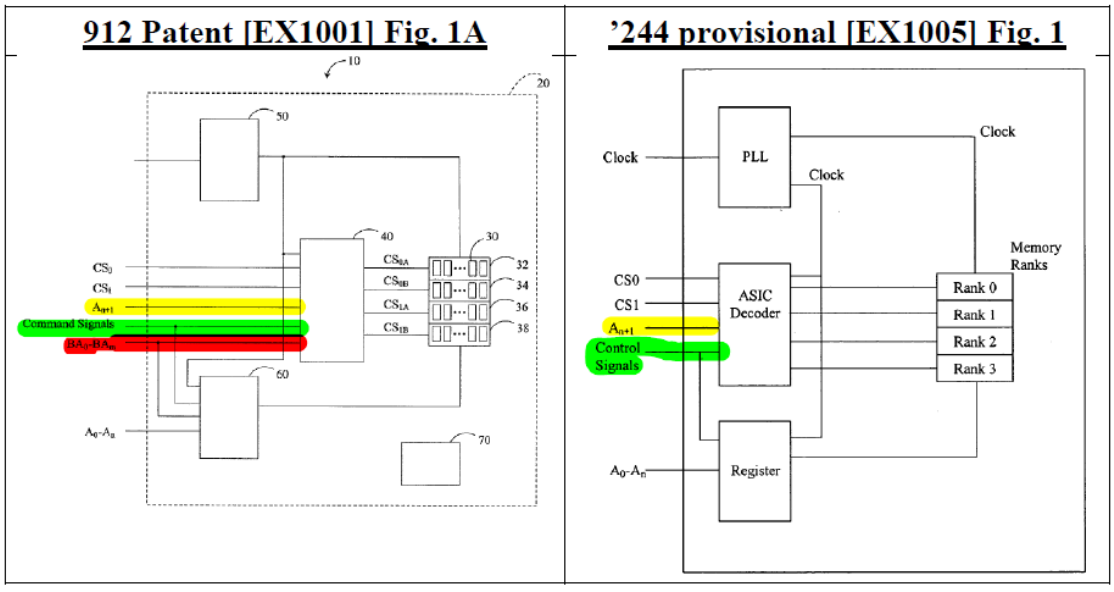
Instead, Patent Owner relies on the '244 provisional and '436 patent as providing written description support for claim 16 of the '912 patent. PO Resp. 54–75; PO Sur-Reply 21–40. Petitioner contends that the '244 provisional has no disclosure of "bank address" signals as required by claim 16. Pet. 63. Petitioner further contends that the '436 patent, which is in a separate priority chain from the '244 provisional, lacks any embodiment including "a circuit" comprising "a logic element" and "a register" as required by claim 16 and as shown in Figure 1A of the '912 patent (elements 40 and 60, respectively). *Id.* at 64 (citing Ex. 1003 ¶ 190). Petitioner, therefore, contends that Ellsberry is not prior art because it predates the earliest effective filing date of the '912 patent. *Id.* at 68–69 (citing Ex. 1003 ¶¶ 188, 196).

a) '244 Provisional

Patent Owner argues that the '244 provisional provides written description support for the "bank address" signals that Petitioner contends are missing. PO Resp. 62–70. Specifically, Patent Owner asserts that a

POSITA would have understood "control signals" to include "bank address" signals under the JEDEC DRAM standards of the day. *Id.* at 63 (citing Ex. 2062 ¶¶ 62–66). Patent Owner asserts that Petitioner's expert, Dr. Wolfe, acknowledged that personal computers would send bank address signals (*id.* at 64); that Figure 1 of the '244 provisional would be understood to be a JEDEC-style memory module because of its chip select signals (*id.* at 64–65); that the JEDEC standards required bank address signals (*id.* at 65–68); and that the '244 provisional mentions "one control signal (such as an address signal)," which would be understood as an "address signal" that would include the bank address signal "BA2" (*id.* at 69–70).

Petitioner replies that the '244 provisional does not provide support for the "bank address" signals and provides the following diagram to explain.



Pet. Reply 34–35. The diagram shows that Figure 1A of the '912 patent includes bank address signals BA_0–BA_m whereas Figure 1 of the '244 provisional does not show any bank address signals, but does show control

signals. Petitioner further asserts that Patent Owner's argument that the control signals contain the bank address signals is belied by the fact that all other address signals are set out in separate lines in the figures. *Id.* at 35 (citing PO Resp. 63–68). In addition, Petitioner contends that Patent Owner's argument that commands would include bank address signals is incorrect because those commands would go to the memory devices, and not to the logic performing rank multiplication. *Id.* (citing Ex. 2103, 109:3–110:8, 111:3–13, 112:15–113:23, 114:23–116:4). Rank multiplication is achieved by the logic element using two input chip select signals to generate one of four output chip select signals to select one of the four ranks of memory devices. *See, e.g.*, Pet. 6–7; Ex. 1003 ¶¶ 173, 190; PO Resp. 1–3; Ex. 2062 ¶¶ 31–35.

Petitioner further notes that Patent Owner argued during reexamination that rank multiplication can be performed by row or column address and not bank address signals. Pet. 7; Pet. Reply 35. For the same reason, Petitioner argues that the '244 provisional's reference to using "an address signal" is not a disclosure of using a "bank address signal" for rank multiplication. *Id.* at 35–36 (citing PO Resp. 69, 72; Ex. 1005 ¶ 10, Fig. 1 ("A_{n+1}")).

Petitioner further contends that Patent Owner asserted that "bank address" signals were known for "DDR" memory devices, but argues that this is an obviousness argument, and obviousness is insufficient to show an actual disclosure of the '244 provisional that would demonstrate that the inventors had possession of how to use "bank address signals" for rank multiplication. *Id.* at 36 (citing *Ariad*, 598 F.3d at 1352; *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017)). Petitioner further argues that the '244

provisional does not even disclose "DDR memory devices" and that Patent Owner makes another obviousness argument based on "DRAM" devices, many of which were not capable of double-data-rate (DDR) operation. *Id.* (citing Ex. 1034, 5–6). Petitioner argues that the '244 patent mentions "data" only once, but does not explain or illustrate the data strobe lines (DQS) for DDR transactions, or how to avoid BBARX collisions for DDR devices. *Id.* at 36–37 (citing Ex. 1034, 6–7 (Figs. 12, 13); Ex. 1101, 80:4–81:16).

Patent Owner replies that the written description requirement does not require the exact terms appearing in the claim to be used *in haec verba* and asserts that Petitioner's arguments fail to consider what a POSITA would have recognized as opposed to what the specification states verbatim. PO Sur-Reply 22. Patent Owner reiterates that the control signals mentioned in the '244 provisional would include bank address signals. *Id.* at 22–28. Patent Owner further asserts that DDR or DDR2 SDRAMs were the most commonly available DRAM devices at the time of the '244 provisional and that a POSITA would have understood that its teachings pertained to such devices. *Id.* at 23–28.

We agree with Petitioner that the '244 provisional does not provide written description support under § 112 ¶ 1 for claim 16 of the '912 patent. There is no mention of "bank address" signals in the '244 provisional. In order to find that "bank address" signals are present, according to Patent Owner's arguments and the evidence presented, one would have to (1) assume at least that the '244 provisional pertains to DDR memory modules (when there is no mention of DDR and there were other types of DRAM devices on the market) because Figure 1 suggests them by its use of

chip select signals and the term "rank," and because they were the most common at the time; (2) understand that DDR DRAMs use bank address signals according to the JEDEC standards; (3) recognize that bank address signals are not mentioned in the '244 provisional; (4) infer that bank address signals would be included as part of the control signals (even though the other address signals are explicitly mentioned and set out separately); and (5) infer that the bank address signals are used for rank multiplication (when row/ and column/address could have been used for this purpose). This is a chain of inferences too long and speculative to show that the '244 provisional demonstrates that the inventors had possession of the subject matter of claim 16.

b) '436 Patent

Petitioner also contends that the '436 patent fails to disclose a "circuit" comprising "a logic element" and "a register" as required by limitation [16.c] of claim 16 of the '912 patent. Pet. 64 (citing Ex. 1003 ¶ 190).

Patent Owner argues that the '436 patent teaches that "the logic element [] 640 comprises a programmable-logic device (PLD) 642" that "uses sequential and combinatorial logic procedures" to produce gated CAS signals or gated chip-select signals for each of the four ranks in Figure 11A of the '436 patent. PO Resp. 55 (citing Ex. 1009, 17:41–45, 18:3–11) (emphasis omitted). Patent Owner argues that Petitioner's expert, Dr. Wolfe, establishes that a POSITA would understand that PLD 642 includes a logic element to perform sequential and combinatorial logic, and that the sequential logic would include a register to store state values. *Id.* at

55–56 (citing Ex. 2103, 117:16–119:18; Ex. 1009, 17:41–45, 18:3–11; Ex. 2062 ¶ 78).

Patent Owner's arguments are not persuasive to demonstrate that the '436 patent provides written description support for claim 16 of the '912 patent. First, the '436 patent teaches that in certain embodiments its logic element 640 comprises a PLD 642 that uses sequential and combinatorial logic procedures. Ex. 1009, 17:41–45, 18:3–11. Under Patent Owner's arguments, a POSITA would have had to infer that "sequential procedures" requires a register when there is no mention of this in the '436 patent, and when other types of devices, such as flip-flops and memory, could hold state as well.[7] For example, Dr. Brogioli recognizes that devices other than a register could be used when he refers to a "*storage* or register" as holding state (Ex. 2062 ¶ 78 (emphasis added)), as does Dr. Wolfe when he refers to a "register or an *equivalent*" (Ex. 2103, 118:16–20 (emphasis added)).

Furthermore, even assuming Patent Owner is correct that a "sequential procedure" implies the existence of a register, that register would be, according to the '436 patent, part of logic element 640. Ex. 1009, 17:41–45, 18:3–11. In contrast, claim 16 recites that "the circuit comprises a logic

[7] Sequential Logic Circuits and the SR Flip-flop (electronics-tutorials.ws) https://www.electronics-tutorials.ws/sequential/seq_1.html (last viewed 4/12/2024) ("Unlike **Combinational Logic** circuits that change state depending upon the actual signals being applied to their inputs at that time, **Sequential Logic** circuits have some form of inherent 'Memory' built in. . . . bistable latches and flip-flops are the basic building blocks of sequential logic circuits. Sequential logic circuits can be constructed to produce either simple edge-triggered flip-flops or more complex sequential circuits such as storage registers, shift registers, memory devices or counters"). Ex. 3021.

element and a register." Ex. 1001, 3:17–18 (reexamination certificate). In other words, claim 16 recites that the "logic element" and "register" are two different things whereas the '436 patent describes the register as included in the logic element.

Moreover, Petitioner argues that Patent Owner did not show that the '436 patent provides written description support for limitation [16.e] requiring that "the command signal is transmitted to only one DDR memory device at a time." Pet. Reply 29 (citing Ex. 1101, 107:24–108:12, 113:1–114:8, 115:16–116:24, 118:6–119:10) (emphasis omitted). Patent Owner argues that this is a new argument. Paper 87, 1. Petitioner alleged, however, that the '436 patent lacked written description support and provided specific examples in the Petition. Pet. 64. In its Response, Patent Owner argued that the '436 patent supports claim 16 of the '912 patent. PO Resp. 54–62. Petitioner's argument in its Reply has nexus and was responsive to Patent Owner's argument in its Response, and was a fair extension of the previously raised Petition argument that the '436 patent lacks support for claim 16 and providing examples to explain why. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1385 (Fed. Cir. 2023) (petitioner's reply argument is not new if it has nexus and is responsive to patent owner's response argument, and is a fair extension of argument raised in petition). In any event, Patent Owner had the opportunity to respond to Petitioner's Reply arguments, and availed itself of that opportunity. PO Sur-Reply 28–40.

Patent Owner further argues that, under Petitioner's theory, the '436 patent's reference to "[o]ther numbers of memory components 610 in each of the ranks 620, 625, 630, 635 are compatible with embodiments described

herein" means that there could be only one memory device per rank, and that a command signal would thus be sent to only one device at a time, which would satisfy limitation [16.e]. PO Sur-Reply 39–40 (citing Ex. 1009, 17:11–13) (alteration in original).

Even if we accept Patent Owner's argument as correct and assume it does not constitute a new argument as Petitioner alleges (*see* Paper 86), this would not negate the other discussed deficiencies in the '436 patent's written description.

Furthermore, to antedate Ellsberry based on the '436 patent, Patent Owner must show that the '436 patent provides written description support for all of the limitations of claim 16. Patent Owner, however, only addresses in its Response how the '436 patent allegedly provides written description support for "each disputed limitation," i.e., those raised by Petitioner. PO Resp. 54–62. This is insufficient because, "to gain the benefit of the filing date of an earlier application under 35 U.S.C. § 120, each application in the chain leading back to the earlier application must comply with the written description requirement of 35 U.S.C. § 112." *Zenon Env't, Inc. v. U.S. Filter Corp.*, 506 F.3d 1370, 1378 (Fed. Cir. 2007) (quoting *Lockwood*, 107 F.3d at 1571); *see also In re Hogan*, 559 F.2d 595, 609 (CCPA 1977) ("[T]here has to be a continuous chain of copending applications each of which satisfies the requirements of § 112 with respect to the subject matter presently claimed." (quoting *In re Schneider*, 481 F.2d 1350, 1356 (CCPA 1973)) (alteration in original).

To show that claim 16 is entitled to the benefit of the March 7, 2005, filing date of the '436 patent, Patent Owner had "to show not only the existence of the earlier application [the '436 patent], but why the written

description in the earlier application supports the claim." *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008). "In the context of the allegedly anticipating [Ellsberry] prior art, that means producing sufficient evidence and argument to show that an ancestor to the ['912] patent, with a filing date prior to the [Ellsberry] date, contains a written description that supports all the limitations of claim [16]." *Id.* Patent Owner did not endeavor to do this as to all limitations of claim 16 with respect to the '436 patent, and, therefore, Patent Owner's attempt to gain the benefit of the filing of the '436 patent fails for this additional reason.

For the foregoing reasons, we determine that the '668, '595, and '244 provisionals and the '436 patent do not provide written description support under § 112 ¶ 1 for claim 16 of the '912 patent. Thus, we do not reach the parties' remaining arguments such as whether the '436 patent describes that row and/or bank address signals are used to generate output signals, or whether the '244 provisional or '436 patent address BBARX collisions. PO Resp. 56–62, Pet. Reply 29–34.

2. Printed Publication

Petitioner contends that Ellsberry is prior art to claim 16 of the '912 patent under §§ 102(a) and (e), and renders the claim obvious under § 103(a). Pet. 4, 20–21 (citing § VI.B.1; Ex. 1003 ¶¶ 189–196). Patent Owner argues that Ellsberry was not published until December 2006, after the invention date of the '912 patent, and thus is not a "printed publication" under § 311(b). PO Resp. 54. Petitioner replies that Patent Owner's argument that Ellsberry is not prior art as of its pre-AIA § 102(e) date is legally incorrect, as the Board has repeatedly held. Pet. Reply 16 (citing

Exs. 1098 and 2063 (same), 7–10; Ex. 1099, 27–29; Ex. 1100, 29; MPEP § 2217).

We agree with Petitioner on this issue, which is currently on appeal before the Court of Appeals for the Federal Circuit. *Lynk Labs, Inc. v. Samsung Electronics Co., Ltd.*, Appeal No. 23-2346, Doc. 14, page 15 (Fed. Cir. Jan. 10, 2024).

In an *inter partes* review, a petitioner "may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or ***printed publications***." 35 U.S.C. § 311(b).

Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1037, code (43) (publication date of Dec. 7, 2006); *see also* PO Resp. 54 (acknowledging publication in December 2006). Ellsberry is prior art at least under 35 U.S.C. § 102(e)(1), being "an application for patent, ***published*** under section 122(b), by another filed in the United States before the invention by the applicant for patent." *See* Ex. 1037, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) because it argues that claim 16 is unpatentable under 35 U.S.C. § 103(a) on the basis of prior art (Ellsberry), which is a printed publication.

Accordingly, we determine that Ellsberry is prior art to the '912 patent at least under pre-AIA 35 U.S.C. § 102(e)(1).

3. Ellsberry (Ex. 1037)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1037, code (54). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from

memory devices communicatively coupled to the memory bank switch." *Id.* at code (57). "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

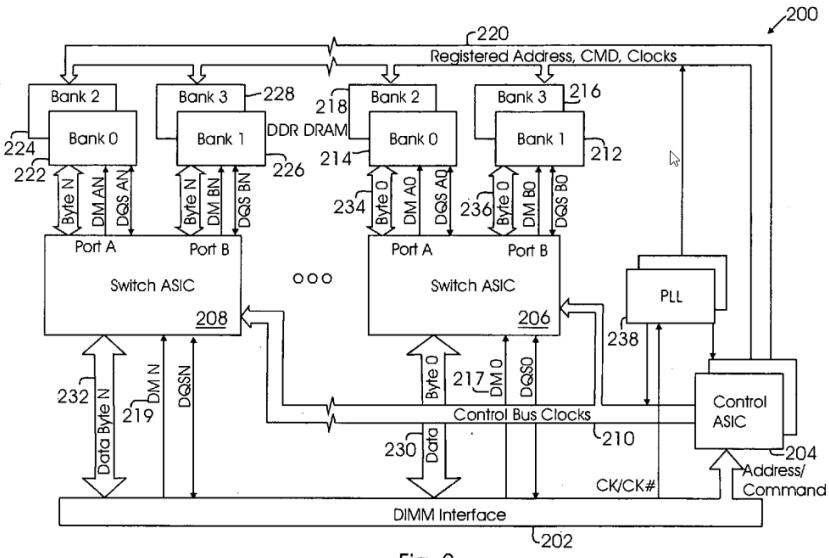


Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29.

Figure 12 of Ellsberry is shown below.

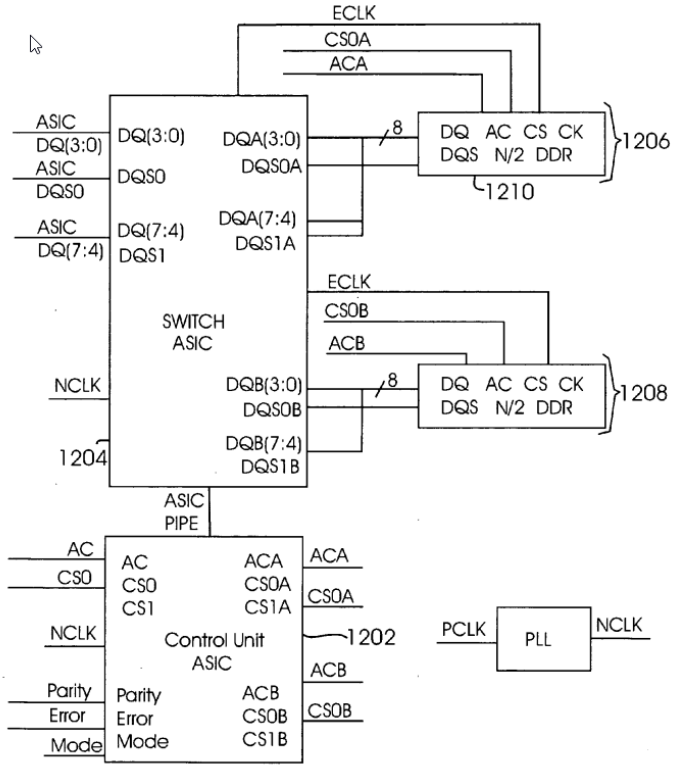


Fig. 12

Figure 12 of Ellsberry shows another configuration of the control unit and bank switch. *Id.* ¶ 52. In Figure 12, a single chip-select memory configuration includes one control unit 1202 and one bank switch 1204 which are used to control two memory banks 1206, 1208, each memory bank having one memory device 1210. *Id.* ¶ 55.

4. Correspondence of Ellsberry to Claim 16

Petitioner contends that Ellsberry teaches or suggests all limitations of claim 16. Pet. 69–111.

The preamble limitation [16.pre] of claim 16 recites "memory module connectable to a computer system." Ex. 1001, 3:9–11 (reexamination certificate). Petitioner contends that Ellsberry describes a memory module 106 with a capacity expanding device 108, connected to a computer system

100 that includes a processing unit 102 and I/O controller 104. Pet. 69 (citing Ex. 1037 ¶¶ 23, 27, Fig. 1; Ex. 1003 ¶¶ 198–199).

Patent Owner does not dispute that Ellsberry discloses the preamble limitation [16.pre].

Petitioner shows that the preamble limitation [16.pre] of claim 16 is taught by Ellsberry. It is thus unnecessary for us to determine whether the preamble is limiting.

Claim 16 further recites limitation [16.a] as "a printed circuit board." Ex. 1001, 3:12 (reexamination certificate). Petitioner contends that Ellsberry teaches a memory module with a printed circuit board. Pet. 72–73 (citing Ex. 1037 ¶ 2, Fig. 5).

Patent Owner does not dispute that Ellsberry discloses limitation [16.a].

Petitioner shows that limitation [16.a] of claim 16 is taught by Ellsberry.

Claim 16 further recites limitation [16.b] as "a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board." Ex. 1001, 3:13–16 (reexamination certificate). Petitioner contends that Ellsberry teaches DDR and DDR 2 memory devices mounted on a circuit board. Pet. 73–74 (citing Ex. 1037 ¶¶ 3, 23, 26, 46; Ex. 1038, 4, 23; Ex. 1003 ¶¶ 209–213).

Claim 16 further recites limitation [16.b.i] as "the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks." Ex. 1001, 3:14–16 (reexamination certificate). Petitioner contends that Ellsberry discloses a memory module with two memory devices arranged in two single device ranks controlled by separate

chip select signals (CS_{0A}, CS_{0B}). Pet. 74–76 (citing Ex. 1037 ¶¶ 3, 26, 30, 32, Fig. 12; Ex. 1003 ¶¶ 215, 218–221). Petitioner thus contends "a first number of DDR memory devices" is two and the "first number of ranks" is two. *Id.* Alternatively, Petitioner contends "a first number of DDR memory devices" is four and the "first number of ranks" is four. *Id.* at 76 (citing Ex. 1037, Fig. 13; Ex. 1003 ¶ 216). Petitioner's expert states that "bank" (as used in Ellsberry) and "rank" were interchangeable terms at the time. Ex. 1003 ¶ 76. Both terms are mentioned in Ellsberry. *See, e.g.*, Ex. 1037, code (57), Fig. 9.

Patent Owner contends that limitation [16.b.i] of claim 16 requires multiple-device ranks. PO Resp. 75–82. For the reasons discussed in § II.C, *supra*, and addressed further with respect to limitation [16.e], *infra*, we determine that "rank" can include only "one memory device." Thus, we disagree with Patent Owner's attempted distinction over the art.

Petitioner shows that limitations [16.b] and [16.b.i] of claim 16 are taught by Ellsberry.

Limitation [16.c] of claim 16 recites "a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register." Ex. 1001, 3:17–18 (reexamination certificate). Petitioner contends that Ellsberry teaches this limitation. Pet. 77–80 (citing Ex. 1003 ¶¶ 224–225). Specifically, Petitioner contends that Ellsberry teaches that the "circuit" is a control unit ASIC, that the "logic element" is a control block, and that the "register" corresponds to register 302. *Id.* at 77.

Petitioner contends that Ellsberry discloses limitation [16.c.i] of claim 16 reciting "the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one

row/column address signal, bank address signals, and at least one chip-select signal." *Id.* at 75–78; Ex. 1001, 3:18–22 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches a command processing system 300 with a control block possessing address/command decode logic 304, configuration decode logic 306, and bank switch state machine 308. Pet. 78–79 (citing Ex. 1037, Fig. 3). Petitioner notes that Ellsberry describes memory addresses and command information are received from DIMM interface 202, buffered in register 302, decoded in logic 304, and that a bank switch state machine 308 determines which memory bank should be activated or accessed. *Id.* at 79 (citing Ex. 1037 ¶ 39). Petitioner contends that a person of ordinary skill in the art would have understood that Ellsberry's control block includes a "logic element" and "register" receiving row/column address signal, bank address signals, and chip-select signals. *Id.* (citing Ex. 1003 ¶ 224).

Petitioner contends that Ellsberry teaches limitation [16.c.ii] of claim 16 reciting "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." Pet. 86–95 (citing Ex. 1003 ¶¶ 232–243); Ex. 1001, 3:22–28 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that the "set of input signals" corresponding to a single DDR2 memory device and the memory module uses two DDR2 memory devices to simulate a larger memory device. *Id.* at 87–88 (citing Ex. 1037, Figs. 7D, 12 [signals AC, C0]; Ex. 1003 ¶ 233). Petitioner contends that Ellsberry teaches that the "set of input signals" includes bank address, row address,

and column address signals consistent with the JEDEC standard. *Id.* at 87–95 (citing Ex. 1037, Figs. 7D, 8A).

Petitioner further contends the "second number of DDR memory devices" is one, which is less than the "first number of DDR memory devices," which is two, and that the "second number of ranks" is one which is less than the "first number of ranks," which is two. *See* Ex. 1037, Fig. 12. According to Petitioner, these relations would also be satisfied for the alternative when the "first number of DDR memory devices" is four and the "first number of ranks" is four. *See* Pet. 76 (citing Ex. 1037, Fig. 13).

Patent Owner contends that limitation [16.c.ii] of claim 16 requires multiple-device ranks. PO Resp. 75–82. As discussed above in § II.C, *supra*, and addressed further regarding limitation [16.e], *infra*, we determine that "rank" can include only one memory device. Thus, we disagree with Patent Owner's attempted distinction over the art.

Petitioner contends that Ellsberry teaches the limitation [16.c.iii] of claim 16 reciting "the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks." Pet. 95–99 (citing Ex. 1037, Figs. 12, 13; Ex. 1003 ¶¶ 244–246); Ex. 1001, 3:28–31 (reexamination certificate). Petitioner contends that Ellsberry teaches that "the circuit" corresponds to the Control Unit ASIC and that the "set of output signals" corresponds to Ellsberry's signals ACA, CS0A, ACB, CS0B that are responsive to the "set of input signals" corresponding to Ellsberry's signals AC, CS0. Pet. 95–96 (citing Ex. 1037, Fig. 12). Petitioner contends that Ellsberry teaches that the "circuit generat[es] the set of output signals in response to the set of input signals" because the

relationship between the input signals and output signals is described in Ellsberry. *Id.* at 97–99 (citing Ex. 1037 ¶¶ 37, 42, 40, Figs. 7D, 8A; Ex. 1003 ¶¶ 232–243, 246). Petitioner further contends that "the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks" corresponds to single device ranks 1206, 1208 corresponding to chip-select signals CS0A, CS0B. *Id.* at 95–96 (citing Ex. 1037, Fig. 12). In addition to this embodiment with two single-device ranks, Petitioner contends similar mappings apply to Ellsberry's embodiment with four-single device ranks. *Id.* (citing Ex. 1037, Fig. 13).

Petitioner contends that Ellsberry teaches the limitation [16.c.iv] of claim 16 reciting "wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks." Pet. 99–103 (citing Ex. 1003 ¶¶ 248–254); Ex. 1001, 3:32–37 (reexamination certificate). Petitioner contends that the "command signal" corresponds to a read or write command under the JEDEC standard. Pet. 99 (citing Ex. 1029, 6, 49). Petitioner further contends that Ellsberry selects "one" rank and transmits the command signal to the selected "one" rank. *Id.*

Furthermore, Petitioner notes that Ellsberry states "[t]he control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)."

Id. at 100 (quoting Ex. 1037 ¶ 11). Petitioner further notes that Ellsberry states that the control unit may send either the same command to both memory banks or different commands to each memory bank with a "no operation" command to the other memory bank. *Id.* at 100–01 (citing Ex. 1037 ¶ 42, Fig. 8A; Ex. 1029, 48, 49; Ex. 1003 ¶¶ 229, 233–235, 249, 250). Petitioner contends this Ellsberry disclosure is similar to Example 1 of the Verilog code in the '912 patent. *Id.* at 102 (citing Ex. 1003 ¶ 251). Petitioner contends another embodiment of Ellsberry selects a target rank based on a row address bit that is bank specific, like Example 2 of the Verilog code in the '912 patent. *Id.* (citing Ex. 1003 ¶ 252).

Patent Owner does not dispute that Ellsberry teaches limitations [16.c], [16.c.i], [16.c.iii], and [16.c.iv].

Petitioner has shown that Ellsberry teaches limitations [16.c], [16.c.i]. [16.c.ii], [16.c.iii], and [16.c.iv] of claim 16.

Claim 16 recites a limitation [16.d] as "a phase-lock loop device coupled to the printed circuit board." Petitioner contends that Ellsberry teaches limitation [16.d]. Pet. 103–06 (citing Ex. 1037 ¶ 2, Figs. 12, 13; Ex. 1003 ¶¶ 255–257). Specifically, Petitioner contends that Ellsberry teaches a "phase lock loop (PLL) 238 [(yellow)] regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 104 (citing Ex. 1037 ¶ 30, Fig. 2; Ex. 1003 ¶ 256) (alteration in original). Petitioner further contends that Ellsberry's PLL is coupled to the circuit board. *Id.* at 105 (citing Ex. 1037 ¶ 48, Fig. 5). In particular, Petitioner contends that Ellsberry teaches that external phase lock loop (PLL) 514 receives a clock signal from the edge interface 506 and provides a clock

signal to the memory module components. *Id.* (citing Ex. 1037 ¶¶ 39, 45, 48, 49, Figs. 2–4, 12; Ex. 1003 ¶ 257).

Claim 16 recites the limitation [16.d.i] as "the phase-lock loop device is operatively coupled to the plurality of DDR memory devices, the logic element, and the register." Ex. 1001, 3:39–41 (reexamination certificate). Petitioner contends that Ellsberry discloses limitation [16.d.i]. Pet. 106–09 (citing Ex. 1003 ¶¶ 259–263). Specifically, Petitioner contends Ellsberry's PLL receives a clock signal PCLK and generates a clock signal NCLK that is provided to the Control Unit ASIC and Switch ASIC. *Id.* at 106 (citing Ex. 1037 ¶ 30, Figs. 2–5, 12, 13; Ex. 1003 ¶¶ 255–257). Petitioner contends the Switch ASIC then uses the clock NCLK to derive the clock ECLK provided to the memory devices. *Id.* Petitioner thus contends Ellsberry's PLL is also operatively coupled to the plurality of DDR memory devices. *Id.* at 106–07 (citing Ex. 1037, Fig. 12; Ex. 1003 ¶ 260).

Petitioner contends Control Unit ASIC uses the clock signal NCLK from the PLL to derive its own local clocks that are provided to both the Control Block and register 302 in the Control Unit ASIC. *Id.* at 108 (citing Ex. 1037, Figs. 3, 12, 13; Ex. 1003 ¶ 261).

Petitioner contends that, to the extent Ellsberry does not sufficiently disclose a local clock of the Control Unit ASIC is provided to the register 302, a person of ordinary skill in the art would have understood that register 302 is clocked by a local clock signal as indicated by the small triangle at the bottom of the register 302. *Id.* at 108–09 (citing Ex. 1003 ¶ 262). Petitioner notes that Ellsberry states that the PLL "regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 109 (quoting Ex. 1037 ¶ 30). Thus, Petitioner contends that Ellsberry's PLL provides a

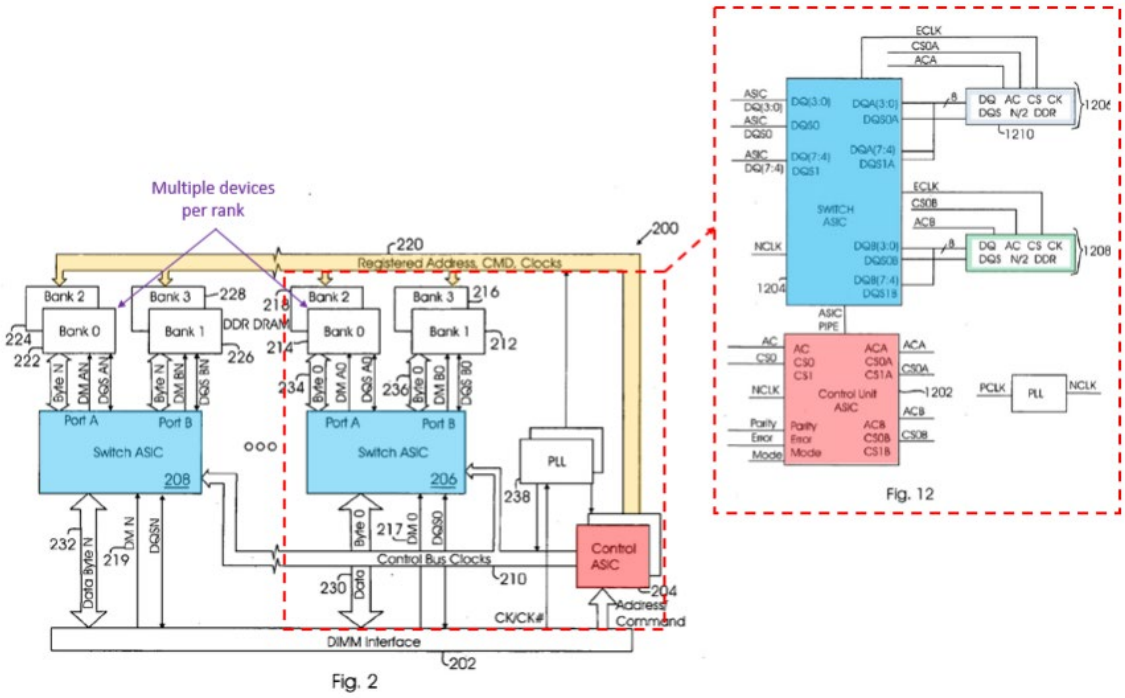
clock to the Control Unit ASIC, which can be used to operate its components, including the register 302, and that a person of ordinary skill in the art "would have understood and been motivated to use the local clock in the Control Unit ASIC to operate the register 302." *Id.* (citing Ex. 1003 ¶ 262).

Patent Owner does not dispute that Ellsberry teaches limitations [16.d] and [16.d.i].

Petitioner has shown that Ellsberry teaches limitations [16.d] and [16.d.i] of claim 16.

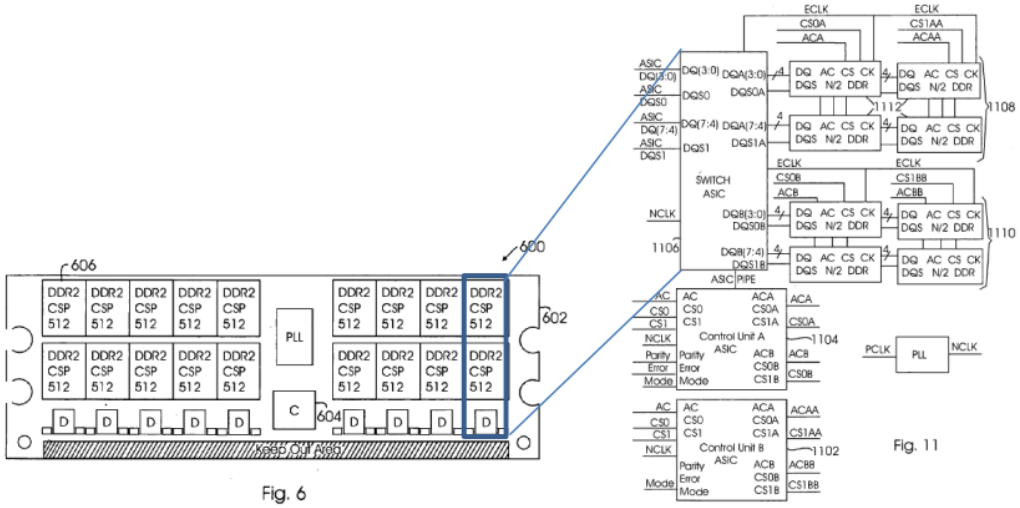
Petitioner contends that Ellsberry discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time." Pet. 109–11 (citing Ex. 1003 ¶¶ 264–265); Ex. 1001, 3:42–43 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that an Activate, Write or Read command signal is transmitted to only the selected memory device and the other memory device receives a no-operation command. Pet. 109–11 (citing Ex. 1037 ¶¶ 10, 33, 42, Figs. 8A, 12; Ex. 1003 ¶ 264).

Patent Owner argues that the Board's prior decision in IPR2023-00203 that Ellsberry's Figure 12 discloses a complete memory module was incorrect. PO Resp. 75 (citing Ex. 2063, 10–11; Ex. 2062 ¶ 239). Patent Owner argues that Ellsberry's Figures 10–13 each depict one data group of a memory module, not the entire memory module. *Id.* at 75–76 (citing Ex. 2062 ¶ 240). In support of its argument, Patent Owner provides the following figure, which is an annotated composite of Ellsberry's Figures 2 and 12.



Id. at 76 (citing Ex. 1037, Figs. 2, 12). Patent Owner contends that Ellsberry's Figure 12 shows a data group which is a part of the entire memory module shown in Ellsberry's Figure 2 which has multiple memory devices per rank. *Id.* at 76–77.

Patent Owner also argues that Ellsberry's Figures 6 and 11, shown below, support its argument that each rank includes multiple memory devices.



Id. at 77. Patent Owner asserts that Figure 6 shows multiple data groups per rank even though Figure 11, like Figure 12, shows only a single bank switch and one data group. *Id.* (citing Ex. 1037 ¶ 51; Ex. 2062 ¶¶ 242–243). Patent Owner argues that "a POSITA would understand that Figures 10–13 are used to illustrate how each data group and switch on the memory module can be implemented, and not how many data groups the memory modules are to have." *Id.* at 77–78 (citing Ex. 1038, 50–51, 57, 77, 81; Ex. 2061, 40 n.11; Ex. 1037 ¶ 52; Figs. 2, 5–6; Ex. 2062 ¶ 244).

Patent Owner further argues that Petitioner's experts, Dr. Wolfe and Dr. Subramanian, testified that they had never used or known of a memory module with DDR or newer generations of DRAMs that was 16 or fewer bits wide. *Id.* at 78 (citing Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:7). Patent Owner asserts that from a POSITA's perspective there were no known 8-bit-wide memory modules, especially JEDEC-style ones, and that 8-bit-wide memory modules would be going against the industry trend of increasing module data width. *Id.* at 79 (citing Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:7; Ex. 1034, 20–21; Ex. 2062 ¶¶ 245–246).

Patent Owner further argues that the Board questioned why Ellsberry needed to comply with JEDEC, and asserts that Ground 3 relies on implementations that follow the JEDEC standard but there is no substantial evidence that a JEDEC-compliant memory module would have a single device per rank. *Id.* at 79–80 (citing Ex. 2063, 12; Pet. 93; Ex. 1037 ¶¶ 50, 57; Ex. 1029, 1–3; Pet. 69–111; Ex. 1032, 4.20.4-5; Ex. 2062 ¶ 247; Ex. 2103, 46:3–15; Ex. 2112, 1; Ex. 1090, 86:19–87:17).

Patent Owner further criticizes Petitioner's contention that it would have been obvious to make a module with only a single data group because it would have been simpler to make, would require fewer parts, and would present fewer error sources. *Id.* at 81 (citing Pet. 76; *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016)). Patent Owner argues that there is no evidence that a POSITA had ever thought of constructing an 8-bit wide DDR memory module. *Id.* at 81–82 (citing Ex. 2062 ¶ 251; Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:13). Patent Owner further asserts this does not make any technical or economic sense, and "[i]f simplicity is desired, Ellsberry would just couple a 1Gbx8 (or 512Mbx8) device directly with the CPU, as the cost saved by removing PCB, PCB routing, costly switch ASIC and control ASIC would more than offset any potential price difference between a single 1Gbx8/512Mbx8 and two 512Mbx8/256Mbx8 devices." *Id.* at 82 (citing Ex. 2062 ¶ 252). Patent Owner concludes that Petitioner is using the claim as a roadmap to piece together the modifications, and is engaging in hindsight. *Id.*

Petitioner argues that Ellsberry does not require multiple switches. Pet. Reply 38 (citing PO Resp. 75–78; Pet. 74–77; Ex. 2103, 157:1–161:3, 164:6–15, 177:13–178:3; Ex. 1037 ¶ 28). Petitioner further contends that

Ellsberry describes Figure 12 as a memory module and not just part of a module, and makes clear that a memory module just requires one or more memory devices. *Id.* (citing Ex. 1037 ¶¶ 21, 23, 52). Petitioner further states that Ellsberry specifically claims a "memory module" with "one or more memory bank switches." *Id.* (citing Ex. 1037, claims 6, 8).

In addition, Petitioner argues that claim 16 does not exclude memory modules that are 8- or 16-bits wide. *Id.* at 39 (citing *id.* at 5; PO Resp. 78–82). Petitioner contends that the JEDEC SPD standards for memory modules specifically permitted those widths. *Id.* (citing *id.* at 14–15). Moreover, Petitioner asserts that Perego-422 specifically taught those widths. *Id.* (citing *id.* at 18, 21–22, where W_A=W_{DP}). Furthermore, Petitioner states that the Board explained that memory modules such as Ellsberry's Figure 12 could still "expand the capacity" of the memory module with multiple ranks. *Id.* (citing Exs. 1098 and 2063 (same), 12).

In Sur-Reply, Patent Owner asserts that JEDEC specifications do not permit memory modules below 32-bits wide. PO Sur-Reply 40–42 (citing Ex. 1006, 8; Ex. 1107, 8). Patent Owner further asserts that Perego-422 and Ellsberry are "completely different architectures." *Id.* at 42 (citing Ex. 1035; Ex. 1037). Patent Owner contends that while Perego-422 can program WA for different access cycles, Ellsberry's data access width is fixed. *Id.* Patent Owner contends there is a lack of any known examples of x8 or x16 DDR1 or DDRs SDRAM modules and that a POSITA would not have found it obvious to construct such a memory module. *Id.* (citing Pet. 81–86).

The parties' disputes concerning limitation [16.e] can be resolved by inspection of Ellsberry. Ellsberry states

> FIGS. 10, 11, 12 and 13 illustrate different configurations of *memory modules* (e.g., DIMMs) that can be built using *combinations of the control unit and bank switch* according to various embodiments of the invention.

Ex. 1037 ¶ 10. We understand this to mean that Figures 10–13 are memory modules notwithstanding that they could also be used as parts of a larger memory module according to Figure 2's configuration. That they are combinations of the control unit and bank switch (singular) means there could be only one bank switch in the memory module.

Ellsberry further states

> [t]he capacity-expanding feature of the invention is accomplished by a combination of a control unit 204 and ***one*** or more memory bank switches 206 & 208.

Id. ¶ 28. This confirms that a memory module may include only one memory bank switch, as shown in Figures 10–13.

Ellsberry's Figure 12 shows a memory module with

> one control unit 1202 and one bank switch 1204 [that] are used to control two memory banks 1206 & 1208, each memory bank having one memory device 1210.

Id. ¶ 55. Petitioner is correct that Ellsberry discloses transmitting a command (Activate, Write or Read) to only the selected one of the two memory devices in Figure 12, and a no-operation (NOP) command to the other memory device. Pet. 109–11 (citing Ex. 1037 ¶¶ 10, 33, 42, Figs. 8A, 12; Ex. 1003 ¶¶ 264–265).

Accordingly, we determine that Ellsberry discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time."

Thus, we do not agree with Patent Owner's arguments that Ellsberry's Figures 10–13 do not constitute respective memory modules, but are only parts of the memory module shown in Figure 2. As to Patent Owner's arguments concerning bit width, claim 16 does not require any particular bit width, so Patent Owner is arguing a feature that is not commensurate in scope with the claim. *In re Self*, 671 F.2d 1344, 1348 (CCPA 1982). Nor does claim 16 recite that the memory module is compliant with a JEDEC standard. Patent Owner also does not explain why a POSITA could not have drawn on teachings in JEDEC standards without fully complying with them as needed for a particular application.

Furthermore, Petitioner directs us to evidence that JEDEC standards permitted 8-bit and 16-bit wide modules. Pet. Reply 14–15 (citing Ex. 1107, 7–8, 13; Ex. 1106, 7–8, 13; Ex. 1101, 141:11–19, 144:10–147:25, 149:10–18, 151:3–153:22); *see* Ex. 1107, 8 (disclosing that "[b]yte 6 is used to designate the module's data width" and including a table indicating values from 0–255). Patent Owner cites this disclosure and asserts that "JEDEC specifications do not permit memory modules below 32-bit wide." PO Sur-Reply 40–42 (reproducing disclosure from Ex. 1107, 8 and Ex. 1106, 8). The cited portions, however, show that the data width can be defined below 32 bits given that a byte can represent 255 values as in Exhibit 1107. *See also* Ex. 1106, 8 (disclosing a "16 bit width identifier").

Moreover, we do not agree with Patent Owner's argument that claim 16 requires sending a command to a single device that is in a multi-device rank. A rank may have only one device for reasons explained in § II.C.

We determine that Petitioner has shown by a preponderance of the evidence that Ellsberry teaches or suggests each limitation of claim 16.

5. Secondary Considerations

Patent Owner does not present objective evidence of non-obviousness other than to respond to Petitioner's assertion of evidence of "simultaneous invention." PO Resp. 82–83. As discussed, Ellsberry teaches all of the limitations of claim 16, and there is no objective evidence of non-obviousness in the record.

6. Conclusion

Petitioner has shown by a preponderance of the evidence that Ellsberry teaches or suggests each limitation of claim 16 of the '912 patent. Accordingly, Petitioner has shown by a preponderance of the evidence that claim 16 of the '912 patent is unpatentable as obvious over Ellsberry.

E. Obviousness of Claim 16 Over Perego-422 (Ground 1)

Our determination that claim 16 is obvious over Ellsberry (Ground 3) is dispositive. Therefore, we need not reach Petitioner's contention that claim 16 is obvious over Perego-422.

F. Obviousness of Claim 16 Over Perego-422 and Amidi (Ground 2)

Our determination that claim 16 is obvious over Ellsberry (Ground 3) is dispositive. Therefore, we need not reach Petitioner's contention that claim 16 is obvious over the combination of Perego-422 and Amidi.

G. Supplemental Information

Patent Owner sought to submit supplemental information in the form of testimony from a Micron representative concerning the meaning of the term "rank." Paper 72. As we determined that the intrinsic evidence is clear that a "rank" may include only one memory device, we do not and need not

resort to extrinsic evidence on this topic. Therefore, we dismiss Patent Owner's motion to introduce this extrinsic evidence.

H. Motion to Exclude

Petitioner sought to exclude Exhibits 1090, 2056, 2058, 2059, 2104, 2107, 2108, 2112, 2113, 2117 and portions of Exhibit 1101. Paper 89. Because we do not rely on any of these Exhibits in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claim 16 of the '912 patent is unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claim 16 of the '912 patent has been shown to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Submit Supplemental Information is dismissed;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[8]

[8] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this

Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
16	103(a)	Perego-422		
16	103(a)	Perego-422, Amidi		
16	103(a)	Ellsberry	16	
Overall Outcome			16	

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Paper 103
Date: July 10, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Before DERRICK BRENT,[2] *Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the United States Patent and Trademark Office*.

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a Petition and Motion for Joinder in IPR2023-00203 and were joined as parties to this proceeding. *See* Paper 58.

[2] Katherine K. Vidal, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office, took no part in this decision. The Director's authority is delegated to Derrick Brent, Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the United States Patent and Trademark Office, by operation of

ORDER

The Office received a request for Director Review of the Final Written Decision in the above-captioned case. *See* Paper 97; Ex. 3100. Director Vidal is recused from this matter, and the request was referred to me.

Upon consideration of the request, it is:

ORDERED that the request for Director Review is denied; and

FURTHER ORDERED that the Patent Trial and Appeal Board's Final Written Decision in this case is the final decision of the agency.

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the Director's Memorandum § II.c. *See* Director's Memorandum, Procedures for Recusal to Avoid Conflicts of Interest and Delegations of Authority (Apr. 20, 2022) (Recusal Procedure Memo), available at www.uspto.gov/sites/default/files/documents/Director-Memorandum-on-Recusal-Procedures.pdf.

IPR2022-00615
Patent 7,619,912 C1

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US007619912B2

(12) **United States Patent**
Bhakta et al.

(10) **Patent No.: US 7,619,912 B2**
(45) **Date of Patent: Nov. 17, 2009**

(54) **MEMORY MODULE DECODER**

(75) Inventors: **Jayesh R. Bhakta**, Cerritos, CA (US); **Jeffrey C. Solomon**, Irvine, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 307 days.

(21) Appl. No.: **11/862,931**

(22) Filed: **Sep. 27, 2007**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, and a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004.

(51) **Int. Cl.**
G11C 15/02 (2006.01)

(52) **U.S. Cl.** **365/51**; 365/230.06; 365/233.1; 365/233.13; 711/105; 711/115

(58) **Field of Classification Search** 365/51, 365/230.06, 233.1, 233.13; 711/105, 115
See application file for complete search history.

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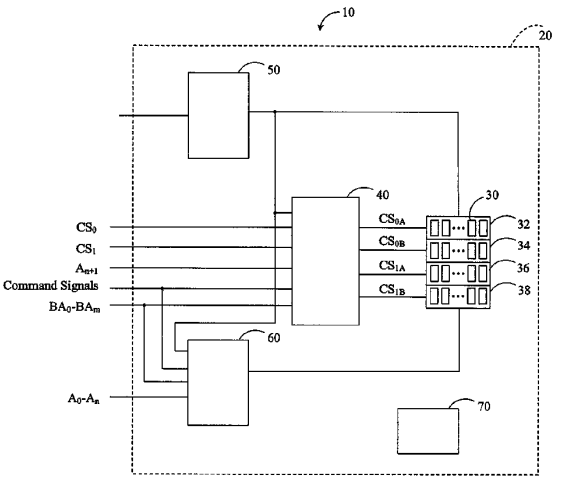
(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

51 Claims, 18 Drawing Sheets



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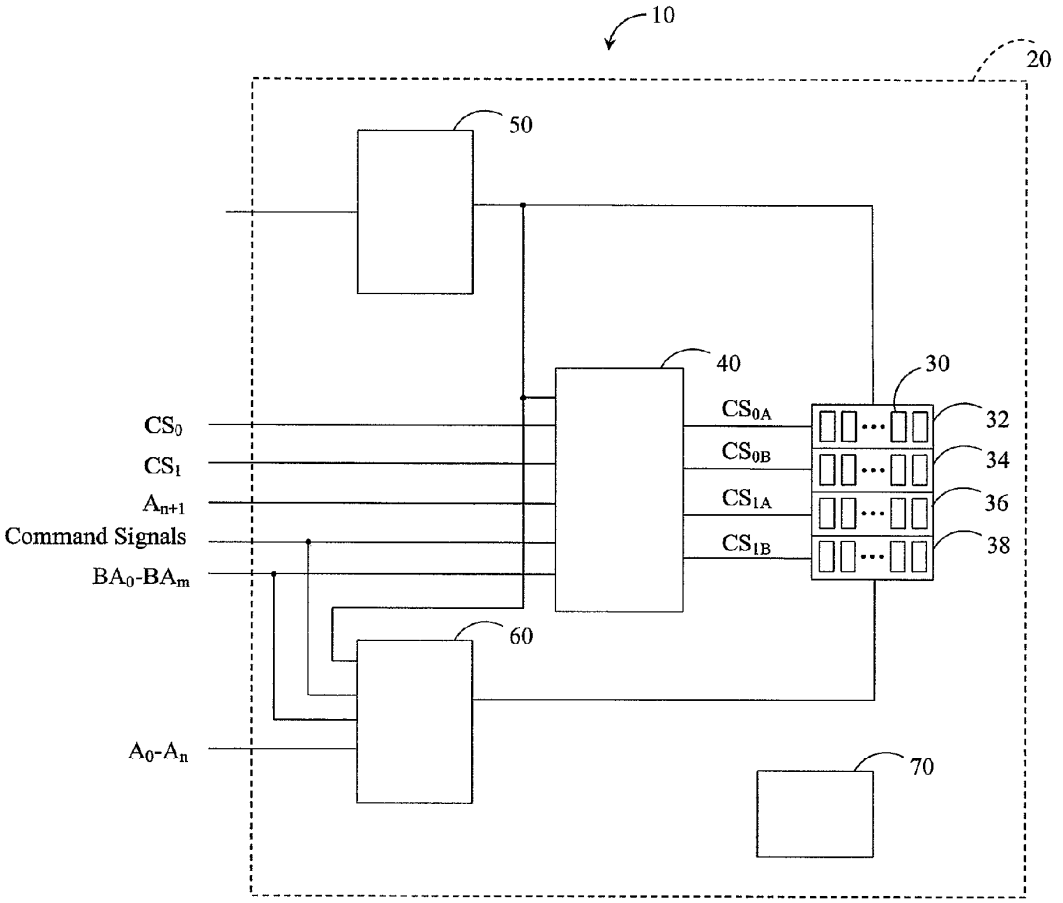
"64 & 72 Pin Zip/Simm Sram Module", JEDEC, Standard No. 21-C, www.jedec.com/download/search/4_04_01.pdf, Jun. 1997 pp. 4.4.1-1.
"PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification" JEDEC, Standard No. 21-C, Revision 1-3, Jan. 2002, pp. 4.20.4-1.

* cited by examiner

Figure 1A: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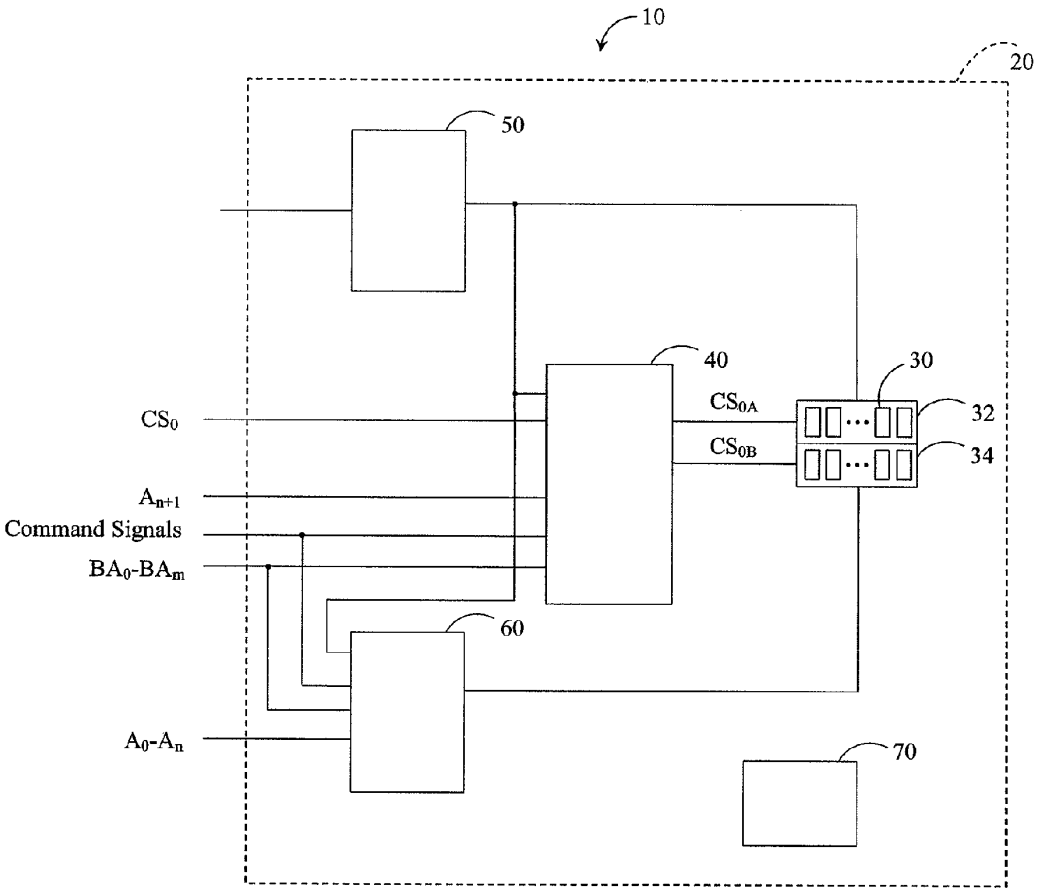
20
50
40
30
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32
34
36
38
60
A_0-A_n
70

Figure 1B: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20
50
40
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CS_0
CS_{0A}
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Command Signals
BA_0-BA_m
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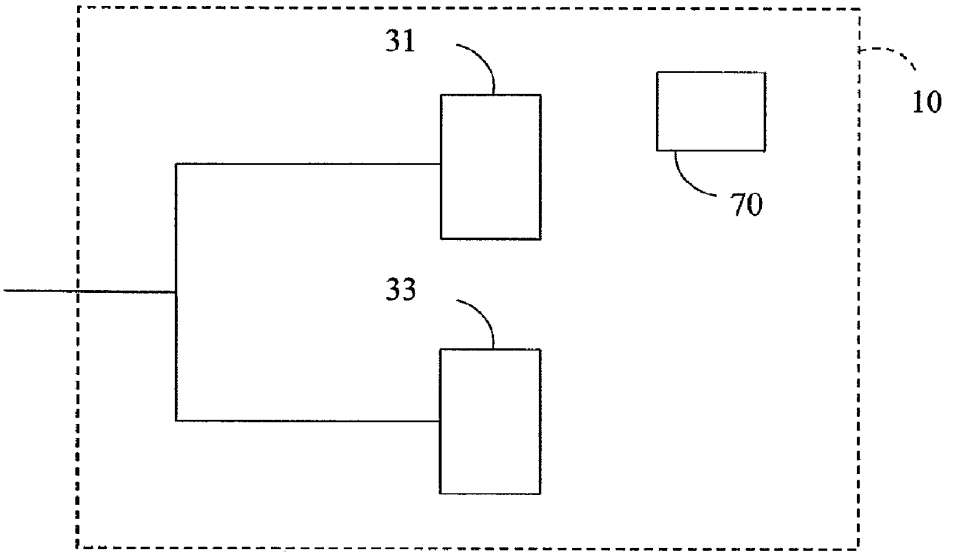
A_0-A_n
70

Figure 1C:



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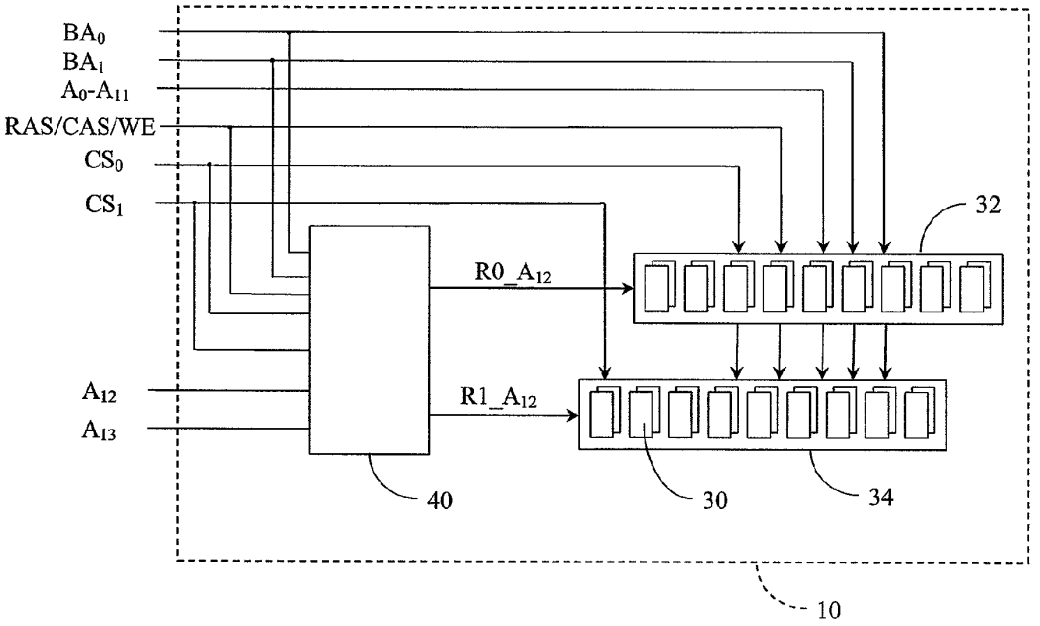

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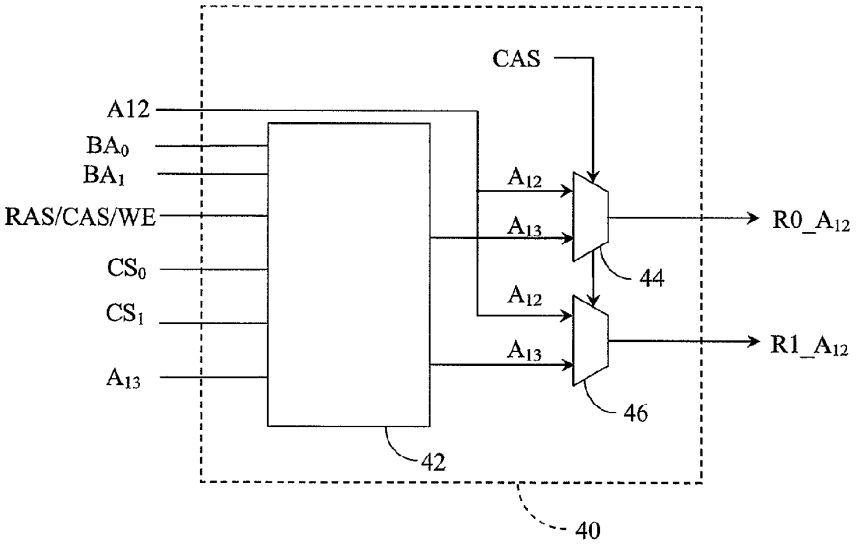

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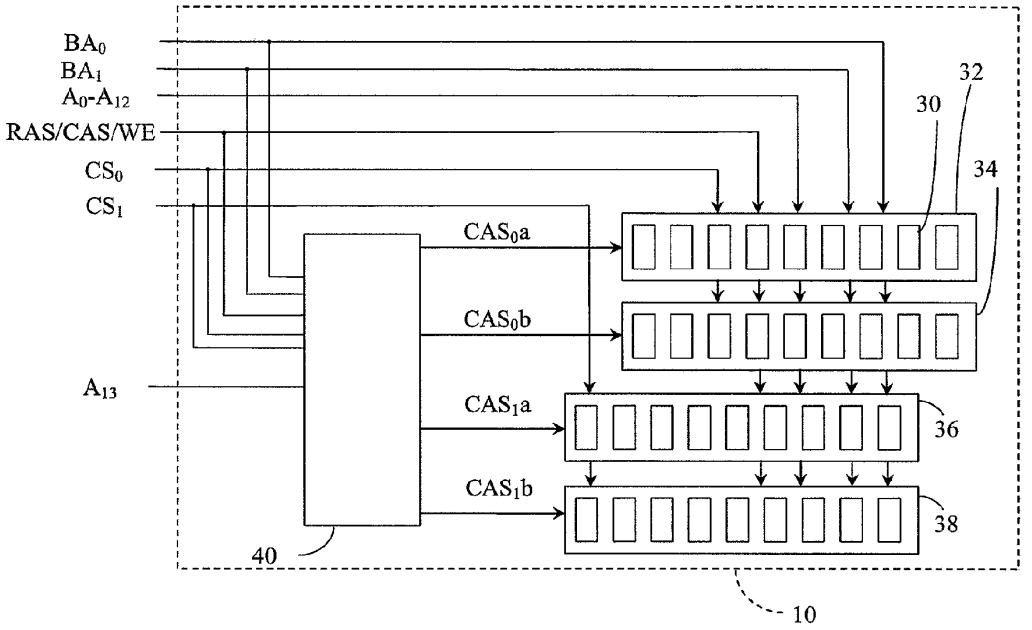

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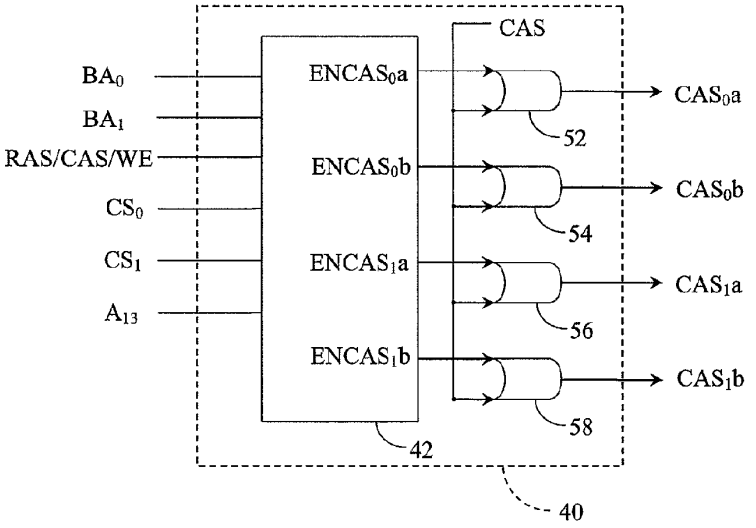

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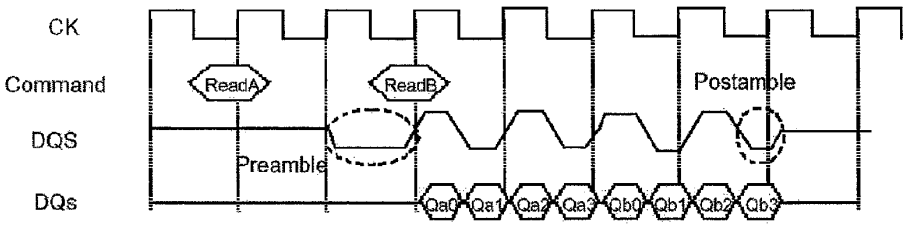

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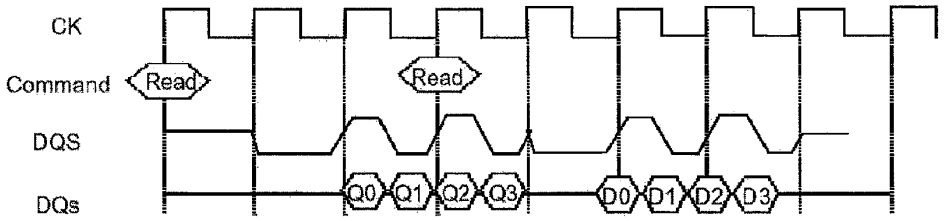

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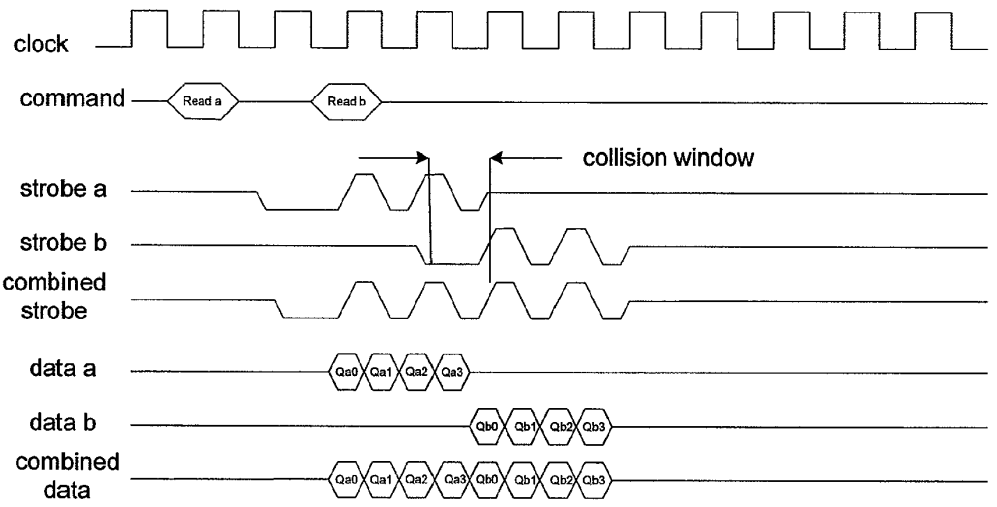
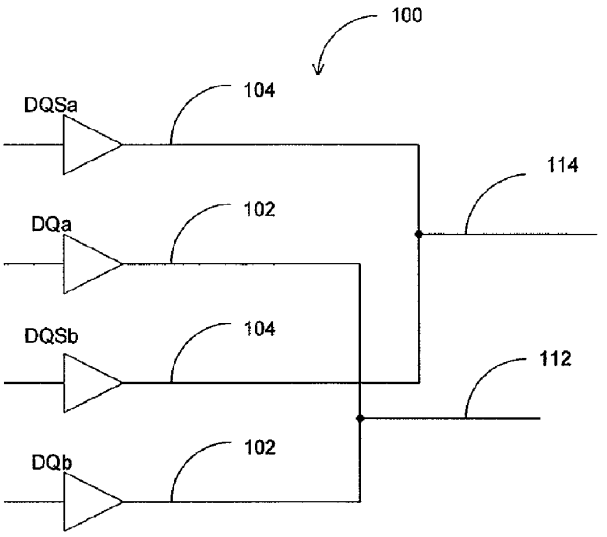

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

Figure 6A:



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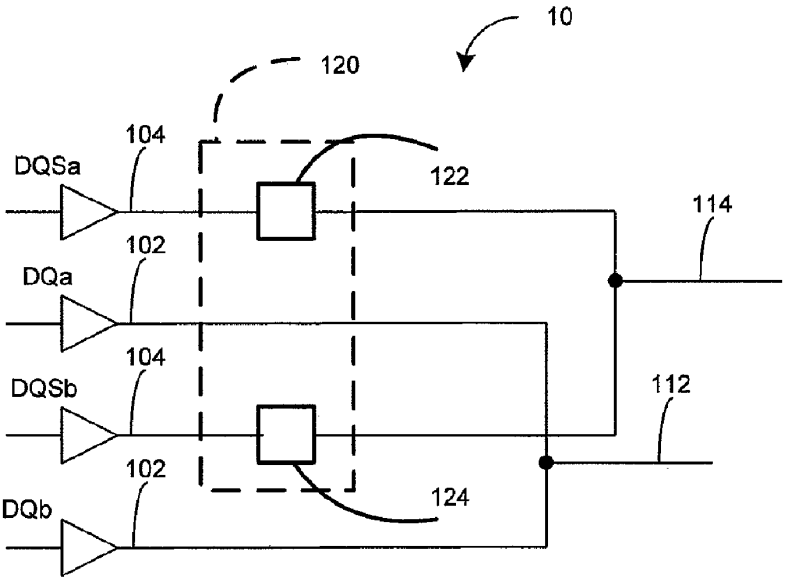

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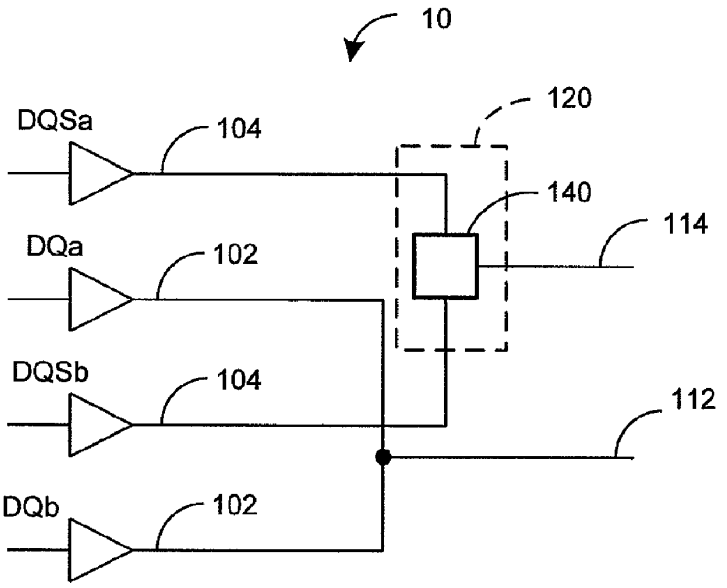

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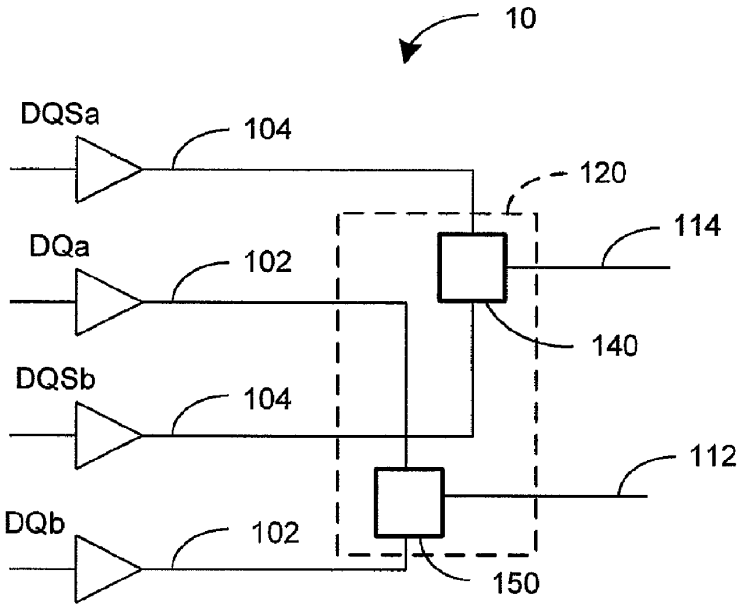

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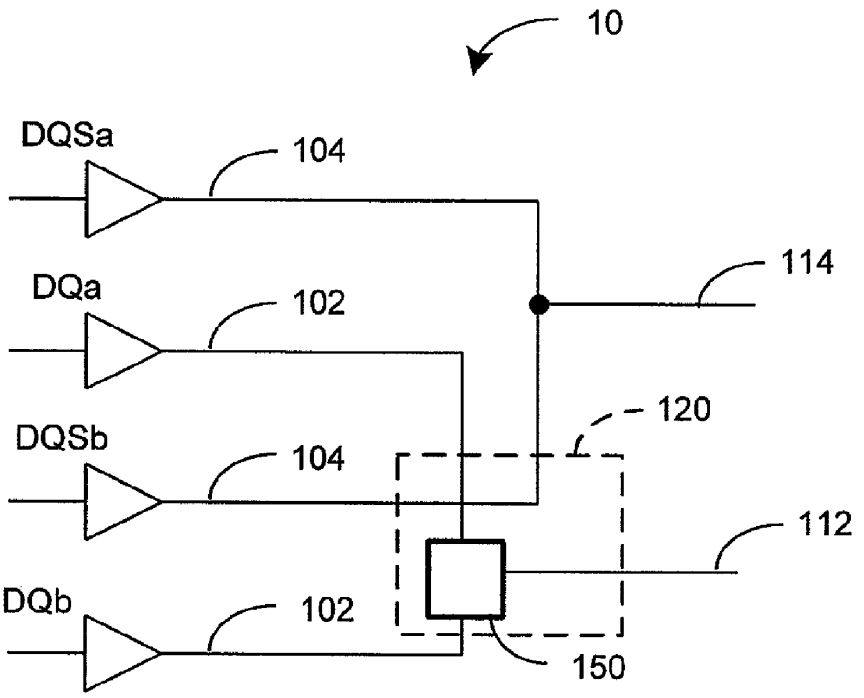

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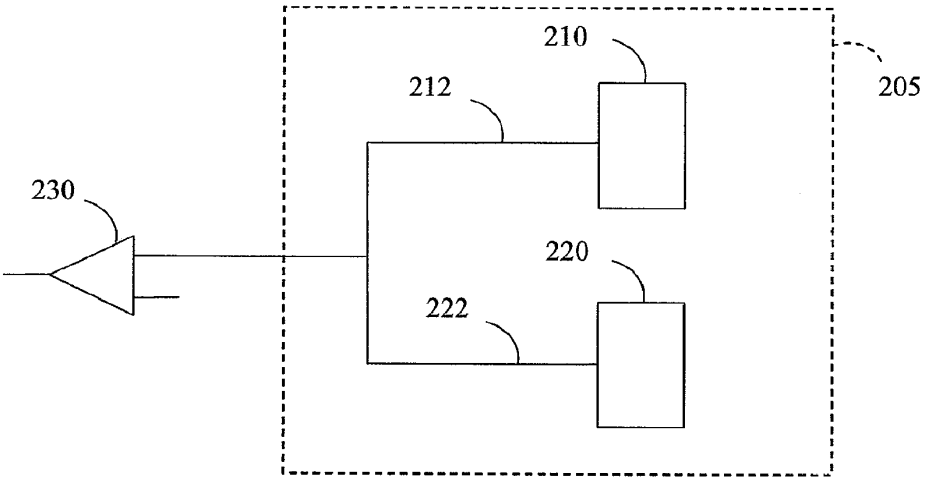

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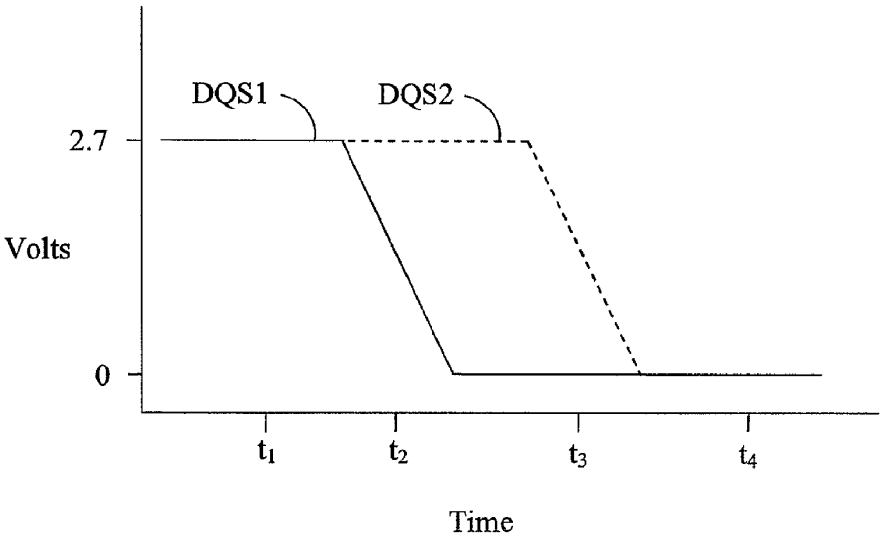

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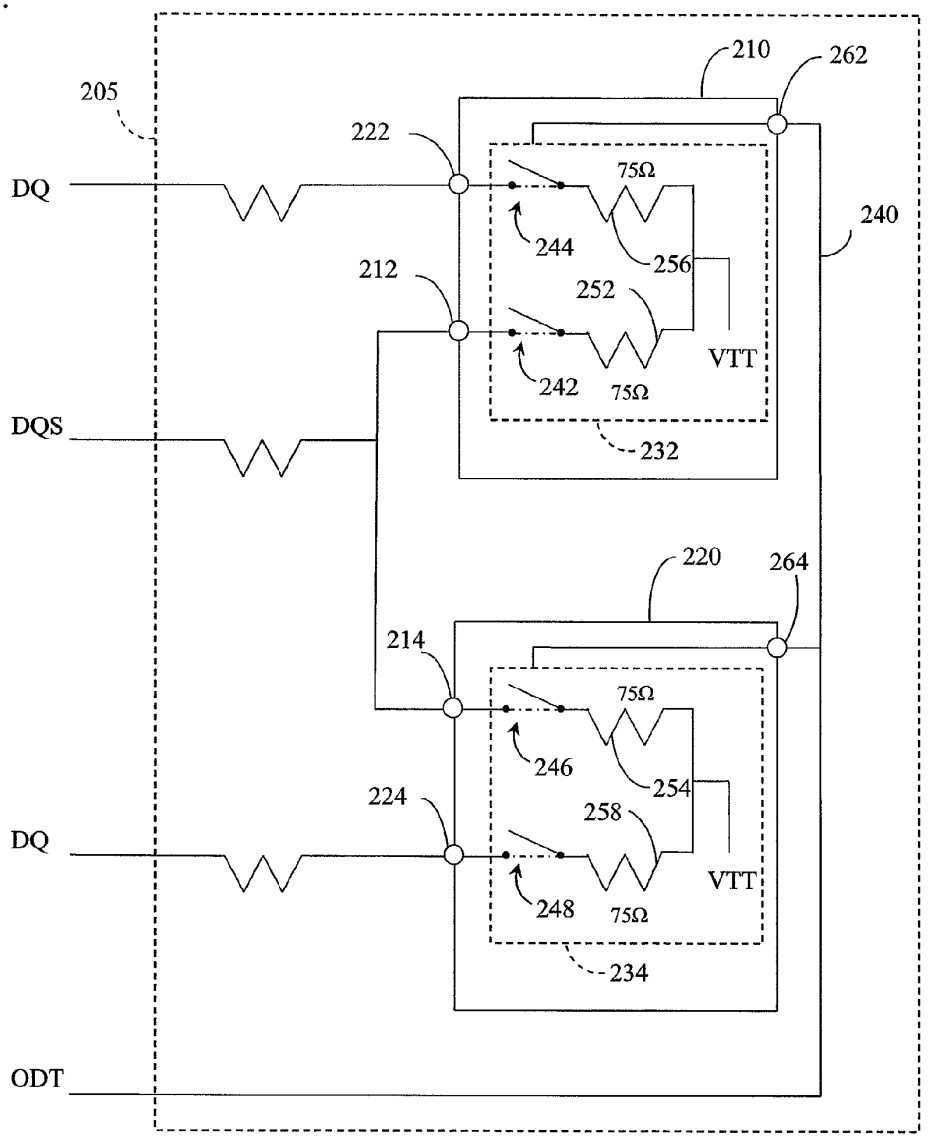
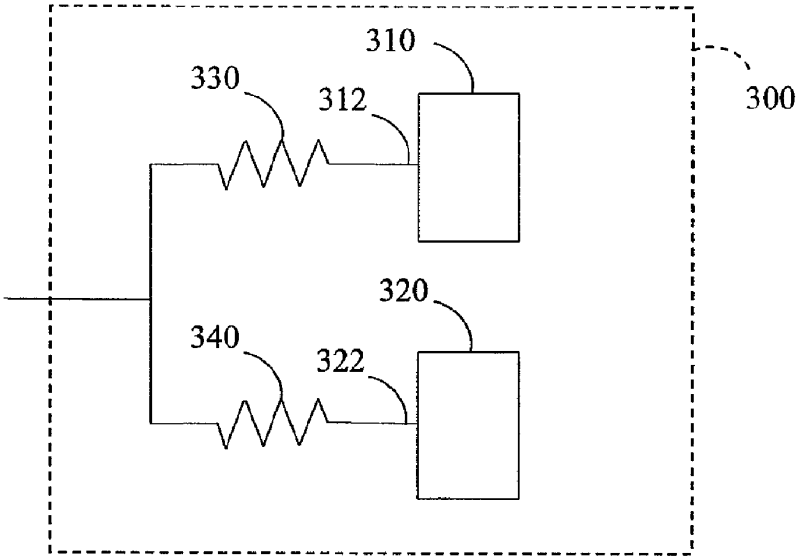

205
210
262
222
DQ
75Ω
240
244
256
212
252
VTT
242
75Ω
DQS
232
220
264
214
75Ω
246
254
224
258
DQ
VTT
248
75Ω
234
ODT

Figure 10:



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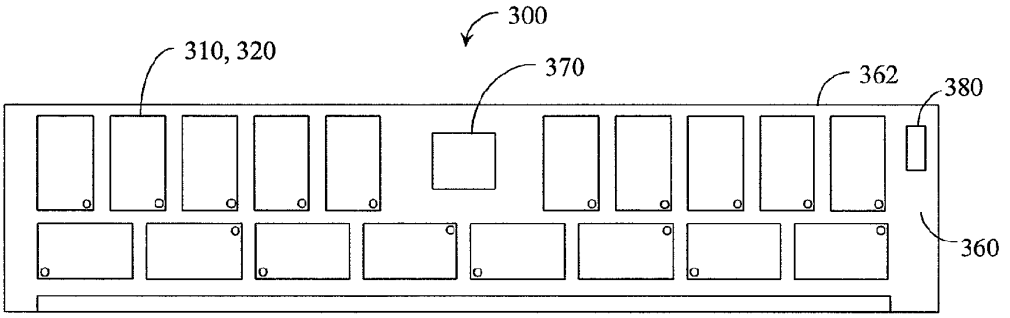

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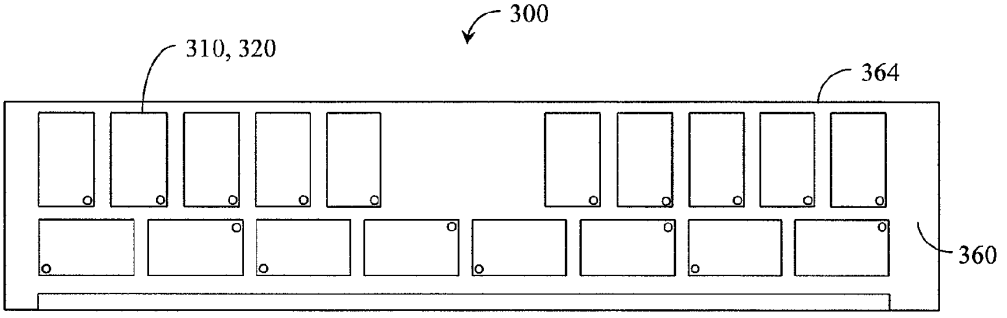

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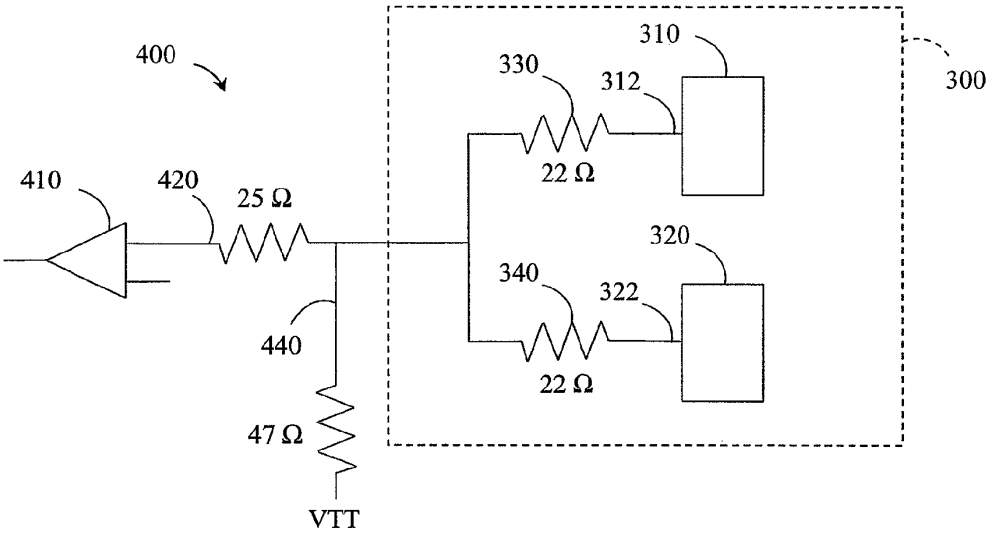

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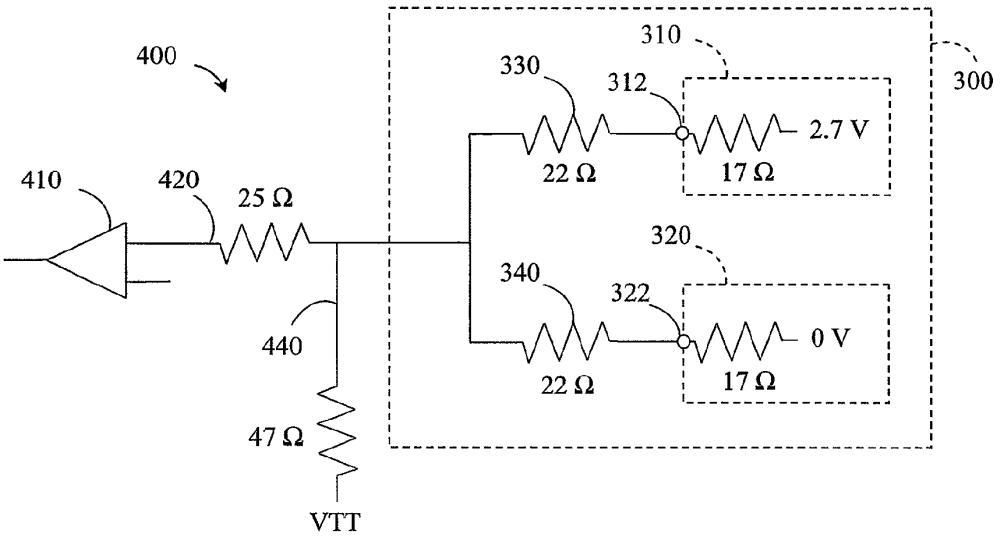

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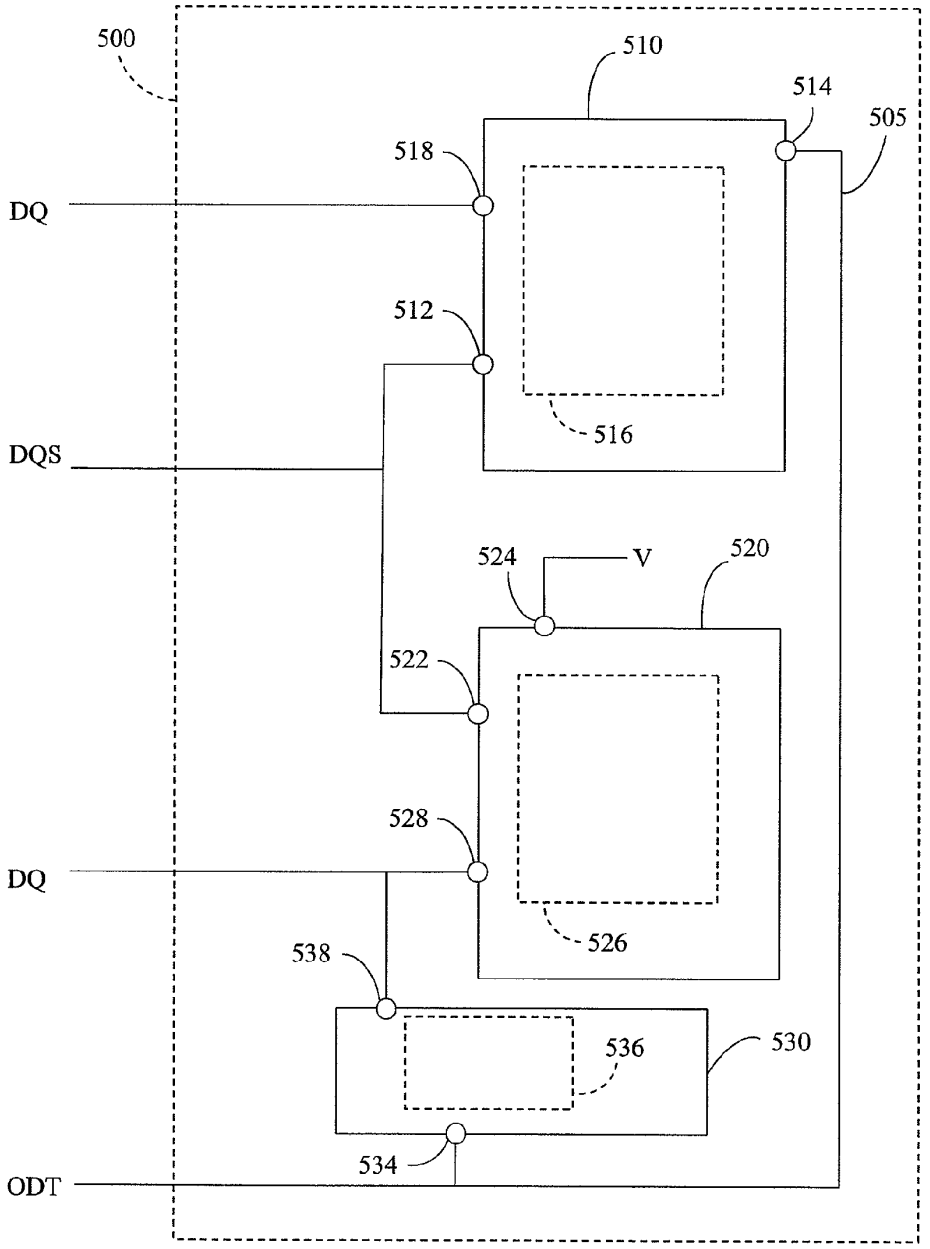
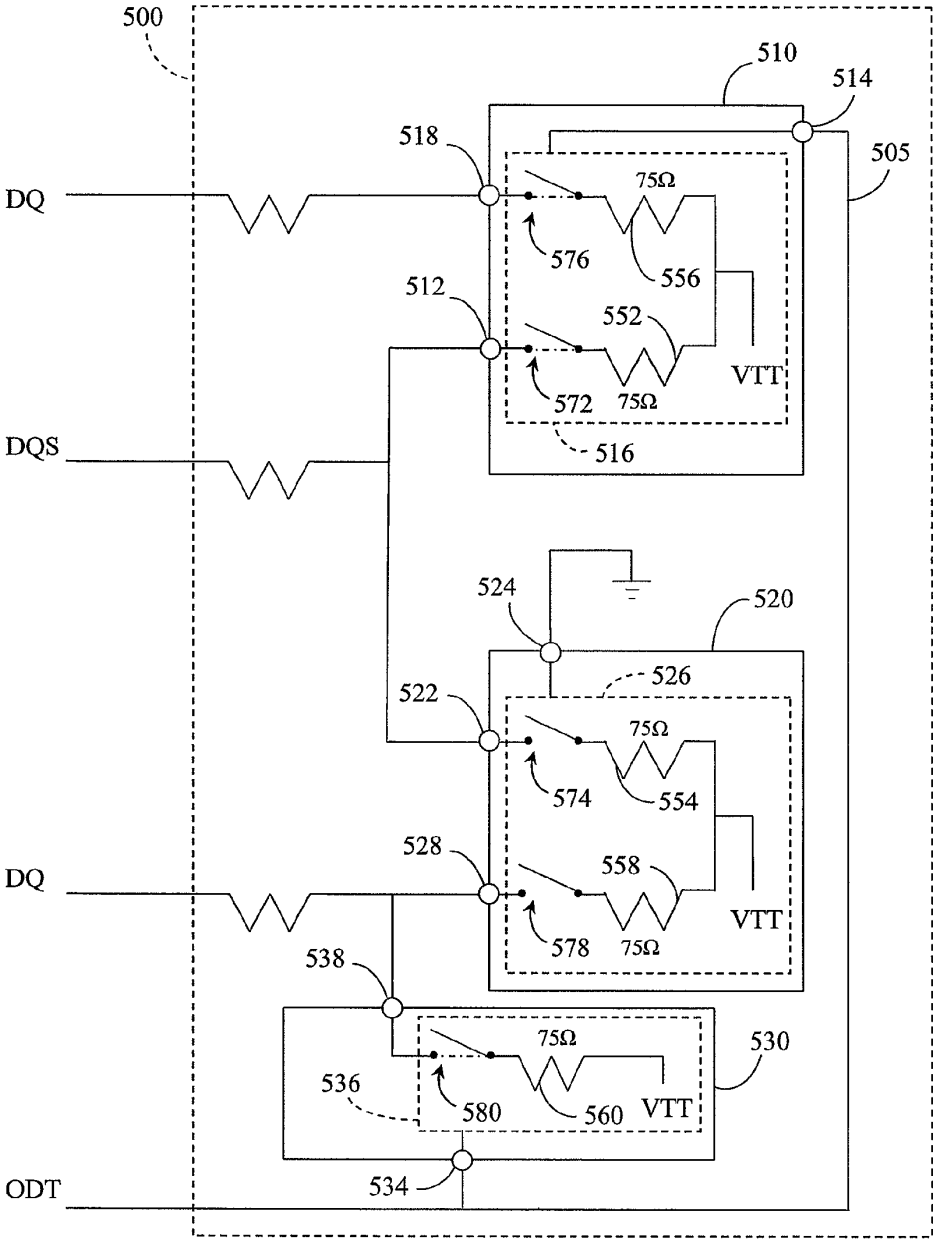

500
510
514
505
518
DQ
512
516
DQS
524
V
520
522
528
DQ
526
538
536
530
534
ODT

Figure 14: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DQ
75Ω
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556
512
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VTT
572
75Ω
DQS
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524
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522
75Ω
574
554
528
558
DQ
VTT
578
75Ω
538
75Ω
530
536
580
560
VTT
534
ODT

MEMORY MODULE DECODER

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation of U.S. patent application Ser. No. 11/173,175, filed Jul. 1, 2005, now U.S. Pat. No. 7,289,386 incorporated in its entirety by reference herein, which claims the benefit of U.S. Provisional Application No. 60/588,244, filed Jul. 15, 2004, incorporated in its entirety by reference herein, and which is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005 now U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Application No. 60/550,668, filed Mar. 5, 2004 and U.S. Provisional Application No. 60/575,595, filed May 28, 2004.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 230 or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 230 or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

The commercially-available 512-MB (64 M×8-byte) memory modules and the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

SUMMARY OF THE INVENTION

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

In certain embodiments, a method utilizes a memory module in a computer system. The method comprises coupling the memory module to the computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The method further comprises inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The method further comprises generating a second set of control signals in

response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The memory module comprises means for coupling the memory module to the computer system. The memory module further comprises means for inputting a first set of control signals to the memory module. The first set of control signals corresponds to a second number of ranks smaller than the first number of ranks. The memory module further comprises means for generating a second set of control signals in response to the first set of control signals. The second set of control signals corresponds to the first number of ranks.

In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises an isolation device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The isolation device selectively alternates between electrically coupling the first data signal line to the common data signal line and electrically coupling the second data signal line to the common data signal line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A schematically illustrates an exemplary memory module with four ranks of memory devices compatible with certain embodiments described herein.

FIG. **1**B schematically illustrates an exemplary memory module with two ranks of memory devices compatible with certain embodiments described herein.

FIG. **1**C schematically illustrates another exemplary memory module in accordance with certain embodiments described herein.

FIG. **2**A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

FIG. **2**B schematically illustrates an exemplary logic element compatible with embodiments described herein.

FIG. **3**A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

FIG. **3**B schematically illustrates an exemplary logic element compatible with embodiments described herein.

FIG. **4**A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

FIG. **4**B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

FIG. **5** shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the preamble time interval of the data strobe of memory device "b."

FIG. **6**A schematically illustrates a circuit diagram of a conventional memory module showing the interconnections between the DQ data signal lines of two memory devices and their DQS data strobe signal lines.

FIG. **6**B schematically illustrates a circuit diagram of an exemplary memory module comprising an isolation device in accordance with certain embodiments described herein.

FIG. **6**C schematically illustrates an isolation device comprising a logic element which multiplexes the DQS data strobe signal lines from one another.

FIG. **6**D schematically illustrates an isolation device which multiplexes the DQS data strobe signal lines from one another and which multiplexes the DQ data signal lines from one another.

FIG. **6**E schematically illustrates an isolation device which comprises the logic element on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

FIG. **7** schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

FIG. **8** is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

FIG. **9** schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

FIG. **10** schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

FIGS. **11**A and **11**B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

FIGS. **12**A and **12**B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

FIG. **13** schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

FIG. **14** schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. **13**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices.

Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer

higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

FIG. **1**A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a computer system (not shown). The memory module **10** comprises a printed circuit board **20** and a plurality of memory devices **30** coupled to the printed circuit board **20**. The plurality of memory devices **30** has a first number of memory devices. The memory module **10** further comprises a logic element **40** coupled to the printed circuit board **20**. The logic element **40** receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element **40** generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

In certain embodiments, as schematically illustrated in FIG. **1**A, the memory module **10** further comprises a phase-lock loop device **50** coupled to the printed circuit board **20** and a register **60** coupled to the printed circuit board **20**. In certain embodiments, the phase-lock loop device **50** and the register **60** are each mounted on the printed circuit board **20**. In response to signals received from the computer system, the phase-lock loop device **50** transmits clock signals to the plurality of memory devices **30**, the logic element **40**, and the register **60**. The register **60** receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **60** comprises a plurality of register devices. While the phase-lock loop device **50**, the register **60**, and the logic element **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **50**, the register **60**, and the logic element **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **50** and a register **60** compatible with embodiments described herein.

In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **20**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), mini-DIMMs, and micro-DIMMs.

In certain embodiments, the printed circuit board **20** is mountable in a module slot of the computer system. The printed circuit board **20** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in four ranks, as schematically illustrated by FIG. **1**A. In other embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. **1**B. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

In certain embodiments, the logic element **40** comprises a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the logic element **40** is a custom device. Sources of logic elements **40** compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element **40** comprises various discrete electrical elements, while in certain other embodiments, the logic element **40** comprises one or more integrated circuits. Persons skilled in the art can select an appropriate logic element **40** in accordance with certain embodiments described herein.

As schematically illustrated by FIGS. **1**A and **1**B, in certain embodiments, the logic element **40** receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element **40** generates a set of output control signals which includes address signals and command signals.

In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input control signals corresponds to a second

number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. **1**A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. **1**B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize.

In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. **1**A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. **1**B.

In the exemplary embodiment schematically illustrated by FIG. **1**A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **60**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The logic element **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the logic element **40** and the register **60** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.

2. A_{n+1} is an active high signal.

3. 'x' is a Don't Care condition.

4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

In Logic State 1: CS_0 is active low, A_{n+1}, is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

In Logic State 4: CS_1 is active low, A_{n+1}, is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

In Logic State 5: CS_1 is active low, A_{n+1}, is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

In Logic State 6: CS_1 is active low, A_{n+1}, is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

Memory modules typically include a serial-presence detect (SPD) device **70** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **70** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

- Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].
- Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].
- Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].
- Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].
- Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

- Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].
- Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].
- Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].
- Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].
- Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

In certain embodiments, the SPD device **70** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **70** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **70** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **70** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **70** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device.

FIG. **1**C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **70** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of

memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

In certain such embodiments, the SPD device **70** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **70** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen 512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **70** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input control signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **70**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **70** reports to the computer system that the memory module **10** only has one rank. The logic element **40** then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**. Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **70** reports to the computer system that the memory module **10** only has one rank. The logic element **40** then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**. Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

Memory Density Multiplication

In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory.

In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The logic element **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "× 4" configuration	11	11	12	12
Number of column address bits for "× 8" configuration	10	10	11	11
Number of column address bits for "× 16" configuration	9	9	10	10

As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	10	4	1 KB
512 Mb	14	10	4	1 KB
1 Gb	14	10	8	1 KB
2 Gb	15	10	8	1 KB
4 Gb	to be determined	to be determined	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

Because the standard memory configuration of 4-Gb DDR2 SDRAM modules is not yet determined by the appropriate standards-setting organization, Tables 3B and 4 have "to be determined" in the appropriate table entries.

In certain embodiments, the logic translation equations are programmed in the logic element **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the logic element **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 1. The exemplary code of Example 1 corresponds to a logic element **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

EXAMPLE 1

```
always @(posedge clk__in)
  begin
        rs0N__R <= rs0__in__N;    // cs0
        rasN__R <= ras__in__N;
        casN__R <= cas__in__N;
        weN__R <= we__in__N;
  end
// Gated Chip Selects
assign          pcs0a__1 = (~rs0__in__N & ~ras__in__N & ~cas__in__N)                    // ref,md reg set
                | (~rs0__in__N & ras__in__N & cas__in__N)                               // ref exit, pwr dn
                | (~rs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & a10__in)       // pchg all
                | (~rs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & ~a10__in & ~ba2__in)// pchg single bnk
                | (~rs0__in__N & ~ras__in__N & cas__in__N & we__in__N      & ~ba2__in)  // activate
                | (~rs0__in__N & ras__in__N & ~cas__in__N              & ~ba2__in)      // xfr
                ;
assign          pcs0b__1 = (~rs0__in__N & ~ras__in__N & ~cas__in__N)                    // ref,md reg set
                | (~rs0__in__N & ras__in__N & cas__in__N)                               // ref exit, pwr dn
                | (~rs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & a10__in)       // pchg all
                | (~rs0__in__N & ~ras__in__N & cas__in__N & ~we__in__N & ~a10__in & ba2__in)// pchg single bnk
                | (~rs0__in__N & ~ras__in__N & cas__in__N & we__in__N      & ba2__in)   // activate
                | (~rs0__in__N & ras__in__N & ~cas__in__N              & ba2__in) // xfr
                ;
//-------------------------------------
  always @(posedge clk__in)
    begin
        a4__r <= a4__in ;
        a5__r <= a5__in ;
        a6__r <= a6__in ;
        a10__r <= a10__in ;
        ba0__r <= ba0__in ;
        ba1__r <= ba1__in ;
        ba2__r <= ba2__in ;
        q__mrs__cmd__cyc1 <= q__mrs__cmd ;
    end
////////////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////////////
assign q__mrs__cmd__r = (!rasN__R & !casN__R & !weN__R)
                & !rs0N__R
              & (!ba0__r & !ba1__r)
                ;               // md reg set cmd
  always @(posedge clk__in)
    if (~reset__N)              // lmr
        cl3 <= 1'b1 ;
    else if (q__mrs__cmd__cyc1)       // load mode reg cmd
    begin
```

-continued

```
            cl3 <= (~a6__r & a5__r & a4__r ) ;
  end
 always @(posedge clk__in)
  if (~reset__N)              // reset
            cl2 <= 1'b0 ;
  else if (q__mrs__cmd__cyc1)       // load mode reg cmd
  begin
            cl2 <= (~a6__r & a5__r & ~a4__r ) ;
  end
 always @(posedge clk__in)
  if (~reset__N)              // reset
            cl4 <= 1'b0 ;
  else if (q__mrs__cmd__cyc1)       // load mode reg cmd
  begin
            cl4 <= (a6__r & ~a5__r & ~a4__r ) ;
  end
 always @(posedge clk__in)
  if (~reset__N)                cl5 <= 1'b0 ;
  else if (q__mrs__cmd__cyc1)       // load mode reg cmd
  begin
            cl5 <= (a6__r & ~a5__r & a4__r ) ;
  end
assign                          pre__cyc2__enfet = (wr__cmd__cyc1 & acs__cyc1 & cl3)        // wr brst cl3 preamble
                                        ;
assign                          pre__cyc3__enfet = (rd__cmd__cyc2 & cl3)                    // rd brst cl3 preamble
                                        | (wr__cmd__cyc2 & cl3)                             // wr brst cl3 1st pair
                                        | (wr__cmd__cyc2 & cl4)                             // wr brst cl4 preamble
                                        ;
assign                          pre__cyc4__enfet = (wr__cmd__cyc3 & cl3)                    // wr brst cl3 2nd pair
                                        | (wr__cmd__cyc3 & cl4)                             // wr brst cl4 1st pair
                                        | (rd__cmd__cyc3 & cl3)                             // rd brst cl3 1st pair
                                        | (rd__cmd__cyc3 & cl4)                             // rd brst cl4 preamble
                                        ;
assign                          pre__cyc5__enfet = (rd__cmd__cyc4 & cl3)                    // rd brst cl3 2nd pair
                                        | (wr__cmd__cyc4 & cl4)                             // wr brst cl4 2nd pair
                                        | (rd__cmd__cyc4 & cl4)                             // rd brst cl4 1st pair
                                        ;
// dq
assign                          pre__dq__cyc = pre__cyc2__enfet
                                   | pre__cyc3__enfet
                                   | pre__cyc4__enfet
                                   | pre__cyc5__enfet
                                   ;
assign                          pre__dq__ncyc = enfet__cyc2
                                   | enfet__cyc3
                                   | enfet__cyc4
                                   | enfet__cyc5
                                   ;
// dqs
assign                          pre__dqsa__cyc = (pre__cyc2__enfet & ~ba2__r)
                                   | (pre__cyc3__enfet & ~ba2__cyc2)
                                   | (pre__cyc4__enfet & ~ba2__cyc3)
                                   | (pre__cyc5__enfet & ~ba2__cyc4)
                                   ;
assign                          pre__dqsb__cyc = (pre__cyc2__enfet & ba2__r)
                                   | (pre__cyc3__enfet & ba2__cyc2)
                                   | (pre__cyc4__enfet & ba2__cyc3)
                                   | (pre__cyc5__enfet & ba2__cyc4)
                                   ;
assign                          pre__dqsa__ncyc = (enfet__cyc2 & ~ba2__cyc2)
                                   | (enfet__cyc3 & ~ba2__cyc3)
                                   | (enfet__cyc4 & ~ba2__cyc4)
                                   | (enfet__cyc5 & ~ba2__cyc5)
                                   ;
assign                          pre__dqsb__ncyc = (enfet__cyc2 & ba2__cyc2)
                                   | (enfet__cyc3 & ba2__cyc3)
                                   | (enfet__cyc4 & ba2__cyc4)
                                   | (enfet__cyc5 & ba2__cyc5)
                                   ;
always @(posedge clk__in)
  begin
            acs__cyc2 <= acs__cyc1 ;        // cs active
            ba2__cyc2 <= ba2__r ;
            ba2__cyc3 <= ba2__cyc2 ;
            ba2__cyc4 <= ba2__cyc3 ;
            ba2__cyc5 <= ba2__cyc4 ;
            rd__cmd__cyc2 <= rd__cmd__cyc1 & acs__cyc1;
            rd__cmd__cyc3 <= rd__cmd__cyc2 ;
            rd__cmd__cyc4 <= rd__cmd__cyc3 ;
```

-continued

```
            rd_cmd_cyc5 <= rd_cmd_cyc4 ;
            rd_cmd_cyc6 <= rd_cmd_cyc5 ;
            rd_cmd_cyc7 <= rd_cmd_cyc6 ;
            wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
            wr_cmd_cyc3 <= wr_cmd_cyc2 ;
            wr_cmd_cyc4 <= wr_cmd_cyc3 ;
            wr_cmd_cyc5 <= wr_cmd_cyc4 ;
  end
 always @(negedge clk_in)
  begin
            dq_ncyc <= dq_cyc;
            dqs_ncyc_a <= dqs_cyc_a;
            dqs_ncyc_b <= dqs_cyc_b;
  end
// DQ FET enables
assign              enq_fet1 = dq_cyc | dq_ncyc                ;
assign              enq_fet2 = dq_cyc | dq_ncyc ;
assign              enq_fet3 = dq_cyc | dq_ncyc                ;
assign                 enq_fet4 = dq_cyc | dq_ncyc ;
assign                 enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign                 ens_fet1a = dqs_cyc_a | dqs_ncyc_a ;
assign                 ens_fet2a = dqs_cyc_a | dqs_ncyc_a ;
assign                 ens_fet3a = dqs_cyc_a | dqs_ncyc_a ;
assign                 ens_fet1b = dqs_cyc_b | dqs_ncyc_b ;
assign                 ens_fet2b = dqs_cyc_b | dqs_ncyc_b ;
assign                 ens_fet3b = dqs_cyc_b | dqs_ncyc_b ;
```

Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a logic element **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

EXAMPLE 2

```
// latched a13 flags cs0, banks 0-3
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
  begin
          1_a13_00 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)   // activate
  begin
          1_a13_01 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)   // activate
  begin
          1_a13_10 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)    // activate
  begin
          1_a13_11 <= a13_r ;
  end
// gated cas
assign cas_i = ~(casN_R);
assign cas0_o = ( ~rasN_R & cas_i)
          | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
          | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
          | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
          | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
          ;
assign cas1_o = ( ~rasN_R & cas_i)
          | ( rasN_R & 1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
```

-continued

```
          | ( rasN__R & 1__a13__01 & ~bnk1__R & bnk0__R & cas__i)
          | ( rasN__R & 1__a13__10 & bnk1__R & ~bnk0__R & cas__i)
          | ( rasN__R & 1__a13__11 & bnk1__R & bnk0__R & cas__i)
          ;
assign    pcas__0__N = ~cas0__o;
assign    pcas__1__N = ~cas1__o;
assign    rd0__o__R1 = rasN__R & cas0__o & weN__R & ~rs0N__R; // rnk0 rd cmd cyc
assign    rd1__o__R1 = rasN__R & cas1__o & weN__R & ~rs0N__R; // rnk1 rd cmd cyc
assign    wr0__o__R1 = rasN__R & cas0__o & ~weN__R & ~rs0N__R; // rnk0 wr cmd cyc
assign    wr1__o__R1 = rasN__R & cas1__o & ~weN__R & ~rs0N__R ; // rnk1 wr cmd cyc
 always @(posedge clk__in)
  begin
          rd0__o__R2 <= rd0__o__R1 ;
          rd0__o__R3 <= rd0__o__R2;
          rd0__o__R4 <= rd0__o__R3;
          rd0__o__R5 <= rd0__o__R4;
          rd1__o__R2 <= rd1__o__R1 ;
          rd1__o__R3 <= rd1__o__R2;
          rd1__o__R4 <= rd1__o__R3;
          rd1__o__R5 <= rd1__o__R4;
          wr0__o__R2 <= wr0__o__R1 ;
          wr0__o__R3 <= wr0__o__R2;
          wr0__o__R4 <= wr0__o__R3;
          wr1__o__R2 <= wr1__o__R1 ;
          wr1__o__R3 <= wr1__o__R2;
          wr1__o__R4 <= wr1__o__R3;
  end
 always @(posedge clk__in)
  begin
  if (
     (rd0__o__R2 & ~rd1__o__R4)                                  // pre-am rd if no ped on rnk 1
   | rd0__o__R3                                                  // 1st cyc of rd brst
   | rd0__o__R4                                                  // 2nd cyc of rd brst
   | (rd0__o__R5 & ~rd1__o__R2 & ~rd1__o__R3)                    // post-rd cyc if no ped on rnk 1
   | (wr0__o__R1)                                                // pre-am wr
   | wr0__o__R2 | wr0__o__R3                                     // wr brst 1st & 2nd cyc
   | (wr0__o__R4)                                                // post-wr cyc (chgef9)
   | wr1__o__R1 | wr1__o__R2 | wr1__o__R3 | wr1__o__R4 // rank 1 (chgef9)
    )
                    en__fet__a <= 1'b1;                          // enable fet
  else
                    en__fet__a <= 1'b0;                          // disable fet
  end
 always @(posedge clk__in)
          begin
          if (
                (rd1__o__R2 & ~rd0__o__R4)
              | rd1__o__R3
              | rd1__o__R4
              | (rd1__o__R5 & ~rd0__o__R2 & ~rd0__o__R3)
            | (wr1__o__R1)                                       // (chgef8)
            | wr1__o__R2 | wr1__o__R3
       | (wr1__o__R4)                                            // post-wr cyc (chgef9)
       | wr0__o__R1 | wr0__o__R2 | wr0__o__R3 | wr0__o__R4       // rank 0 (chgef9)
            )
                    en__fet__b <= 1'b1;                          //
          else
                    en__fet__b <= 1'b0;
          end
```

FIG. **2**A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32** and a second rank **34**. In certain embodiments, the memory devices **30** of the first rank **32** are configured in pairs, and the memory devices **30** of the second rank **34** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **34** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a logic element **40** which receives a first set of address and control signals from a memory controller (not shown) of the computer system. The first set of address and control signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The logic element **40** translates the first set of address and control signals into a second set of address and control signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32** and the second rank **34**.

The first rank **32** of FIG. **2**A has 18 memory devices **30** and the second rank **34** of FIG. **2**A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32**, **34** are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **2**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **2**A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. **2**A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and control signals including the extra row address (A_{13}) to the memory module **10**. The logic element **40** receives the address and control signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

FIG. **2**B schematically illustrates an exemplary logic element **40** compatible with embodiments described herein. The logic element **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. **2**B, the logic element **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **34** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

In the exemplary logic element **40** of FIG. **2**B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **34** as the A_{12} address. The first rank **32** and the second rank **34** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the logic element **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

FIG. **3**A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32**, a second rank **34**, a third rank **36**, and a fourth rank **38**. The memory module **10** further comprises a logic element **40** which receives a first set of address and control signals from a memory controller (not shown). The first set of address and control signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The logic element **40** translates the first set of address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32**, the second rank **34**, the third rank **36**, and the fourth rank **38**.

Each rank **32**, **34**, **36**, **38** of FIG. **3**A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32**, **34**, **36**, **38** are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **3**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **3**A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and control signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. **3**A. FIG. **3**B schematically illustrates an exemplary logic element **40** compatible with embodiments described herein. In certain embodiments, the logic element **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32**, **34**, **36**, **38** of memory devices **30**.

In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements,

while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

In the embodiment schematically illustrated by FIG. **3**B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32**, **34**, **36**, **38** is active.

In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32**, **34**, **36**, **38**. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32**, **34**, **36**, **38**.

Back-to-Back Adjacent Read Commands

Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. **4**A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. **4**B for successive read accesses from different memory devices.

In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

In certain embodiments described herein in which the number of ranks of the memory module is doubled or quadrupled, the logic element **40** generates a set of output control signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller of the computer system. As shown in FIG. **5**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

FIG. **6**A schematically illustrates a circuit diagram of a conventional memory module **100** showing the interconnections between the DQ data signal lines **102** of the memory devices "a" and "b" (not shown) and their DQS data strobe signal lines **104**. In certain embodiments, the electrical signal lines are etched on the printed circuit board. As shown in FIG. **6**A, each of the memory devices has their DQ data signal lines **102** electrically coupled to a common DQ line **112** and the DQS data strobe signal lines **104** electrically coupled to a common DQS line **114**.

In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104** of the memory devices from one another during the transition from the first read data burst of one rank of memory devices to the second read data burst of another rank of memory devices. FIG. **6**B schematically illustrates a circuit diagram of an exemplary memory module **10** comprising an isolation device **120** in accordance with certain embodiments described herein. As shown in FIG. **6**B, each of the memory devices **30** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104** electrically coupled to the common DQS line **114** through the isolation element **120**. The isolation device **120** of certain embodiments multiplexes the DQS data strobe signal lines **104** of the two ranks of memory devices **30** from one another to avoid a BBARX collision.

In certain embodiments, as schematically illustrated by FIG. **6**B, the isolation device **120** comprises a first switch **122** electrically coupled to a first data strobe signal line (e.g., DQSa) of a first memory device (not shown) and a second switch **124** electrically coupled to a second data strobe signal line (e.g., DQSb) of a second memory device (not shown). Exemplary switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. In certain embodiments, the time for switching the first switch **122** and the second switch **124** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first memory device and before the first DQS data strobe of the read data burst of the second memory device). During the read data burst for a first memory device, the first switch **122** is enabled. After the last DQS data strobe of the first memory device and before the first DQS data strobe of the second memory device, the first switch **122** is disabled and the second switch **124** is enabled.

In certain embodiments, as schematically illustrated by FIG. **6**C, the isolation device **120** comprises a logic element **140** which multiplexes the DQS data strobe signal lines **104** from one another. Exemplary logic elements compatible with embodiments described herein include, but are not limited to multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex. The logic element **140** receives a first DQS data strobe signal from the first memory device and a second

DQS data strobe signal from a second memory device and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**. Persons skilled in the art can select other types of isolation devices **120** compatible with embodiments described herein.

In certain embodiments, as schematically illustrated by FIG. **6**D, the isolation device **120** also multiplexes the DQ data signal lines **102** of the two memory devices from one another. For example, in certain embodiments, the isolation device **120** comprises a pair of switches on the DQ data signal lines **102**, similar to the switches **122**, **124** on the DQS data strobe signal lines **104** schematically illustrated by FIG. **6**B. In certain other embodiments, the isolation device **120** comprises a logic element **150**, as schematically illustrated by FIG. **6**D. In certain embodiments, the same types of switches and/or logic elements are used for the DQ data signal lines **102** as for the DQS data strobe signal lines **104**. The logic element **150** receives a first DQ data signal from the first memory device and a second DQ data signal from the second memory device and selectively switches one of the first and second DQ data signals to the common DQ data signal line **112**. Persons skilled in the art can select other types of isolation devices **120** compatible with embodiments described herein.

In certain embodiments, the isolation device **120** advantageously adds propagation delays to the DQ data signals which match the DQS strobe signals being multiplexed by the isolation device **120**. In certain embodiments, the isolation device **120** advantageously presents a reduced impedance load to the computer system by selectively switching between the two ranks of memory devices to which it is coupled. This feature of the isolation device **120** is used in certain embodiments in which there is no memory density multiplication of the memory module (e.g., for a computer system with four chip-select signals), but where the impedance load of the memory module may otherwise limit the number of ranks or the number of memory devices per memory module. As schematically illustrated by FIG. **6**E, the isolation device **120** of certain such embodiments comprises the logic element **150** on the DQ data signal lines but not a corresponding logic element on the DQS data strobe signal lines.

In certain embodiments, the control and timing of the isolation device **120** is performed by an isolation-control logic element (e.g., application-specific integrated circuit, custom programmable logic device, field-programmable gate array, etc.) which is resident on the memory module **10**. In certain embodiments, the isolation-control logic element is the same logic element **40** as schematically illustrated in FIGS. **1**A and **1**B, is part of the isolation device **120** (e.g., logic element **140** or logic element **150** as schematically illustrated by FIG. **6**D), or is a separate component. The isolation-control logic element of certain embodiments controls the isolation device **120** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate components of the isolation device **120** are switched to enable and disable the DQS data strobe signal lines **104** to mitigate BBARX collisions. In certain other embodiments, the isolation-control logic element monitors the commands received by the memory module from the computer system and selectively enables and disables the DQ data signal lines **102** to reduce the load impedance of the memory module **10** on the computer system. In still other embodiments, this logic element performs both of these functions together.

Tied Data Strobe Signal Pins

For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

FIGS. **7** and **8** schematically illustrate a problem which may arise from tying together two output signal pins. FIG. **7** schematically illustrates an exemplary memory module **205** in which a first DQS pin **212** of a first memory device **210** is electrically connected to a second DQS pin **222** of a second memory device **220**. The two DQS pins **212**, **222** are both electrically connected to a memory controller **230**.

FIG. **8** is an exemplary timing diagram of the voltages applied to the two DQS pins **212**, **222** due to non-simultaneous switching. As illustrated by FIG. **8**, at time t_1, both the first DQS pin **212** and the second DQS pin **222** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **212** and the second DQS pin **222** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **212** is low while the second DQS pin **222** is high. Under such conditions, a current will flow between the two DQS pins **212**, **222**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **212**, **222** can be substantial, resulting in heating of the memory devices **210**, **220**, and contributing to the degradation of reliability and eventual failure of these memory devices.

A second problem may also arise from tying together two output signal pins. FIG. **9** schematically illustrates another exemplary memory module **205** in which a first DQS pin **212** of a first memory device **210** is electrically connected to a second DQS pin **214** of a second memory device **220**. The two DQS pins **212**, **214** of FIG. **9** are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **222** of the first memory device **210** and the corresponding DQ pin **224** of the second memory device **220** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **210**, **220** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. **9** only shows one DQ pin for each memory device **210**, **220**.

Each of the memory devices **210**, **220** of FIG. **9** utilizes a respective on-die termination or "ODT" circuit **232**, **234** which has termination resistors (e.g., 75 ohms) internal to the memory devices **210**, **220** to provide signal termination. Each memory device **210**, **220** has a corresponding ODT signal pin **262**, **264** which is electrically connected to the memory controller via an ODT bus **240**. The ODT signal pin **262** of the first memory device **210** receives a signal from the ODT bus **240** and provides the signal to the ODT circuit **232** of the first memory device **210**. The ODT circuit **232** responds to the signal by selectively enabling or disabling the internal termination resistors **252**, **256** of the first memory device **210**. This behavior is shown schematically in FIG. **9** by the switches **242**, **244** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **264** of the second memory device **220** receives a signal from the ODT bus **240** and provides the signal to the ODT circuit **234** of the second memory device **220**. The ODT circuit **234** responds to the signal by selectively enabling or disabling the internal termination resistors **254**, **258** of the second memory device **220**. This behavior is shown schematically in FIG. **9** by the switches **246**, **248** which are either closed (dash-dot line) or opened (solid line). The switches **242**, **244**, **246**, **248** of FIG. **9** are schematic representations of the operation of the ODT circuits **232**, **234**, and do not signify that the ODT circuits **232**, **234** necessarily include mechanical switches.

Examples of memory devices **210**, **220** which include such ODT circuits **232**, **234** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **262** of the first memory device **210** is pulled high, the termination resistors **252**, **256** of the first memory device **210** are enabled. When the ODT signal pin **262** of the first memory device **210** is pulled low (e.g., grounded), the termination resistors **252**, **256** of the first memory device **210** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

In certain configurations, as schematically illustrated by FIG. **9**, the DQS pins **212**, **214** of each memory device **210**, **220** are selectively connected to a voltage VTT through a corresponding termination resistor **252**, **254** internal to the corresponding memory device **210**, **220**. Similarly, in certain configurations, as schematically illustrated by FIG. **9**, the DQ pins **222**, **224** are selectively connected to a voltage VTT through a corresponding termination resistor **256**, **258** internal to the corresponding memory device **210**, **220**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **222**, **224** and/or the DQS pins **212**, **214** are selectively connected to ground through the corresponding termination resistors **252**, **254**, **256**, **258**. The resistances of the internal termination resistors **252**, **254**, **256**, **258** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. **9**, each internal termination resistor **252**, **254**, **256**, **258** has a resistance of approximately 75 ohms.

When connecting the first memory device **210** and the second memory device **220** together to form a double word width, both the first memory device **210** and the second memory device **220** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **210** and the second memory device **220** by tying the DQS pins **212**, **214** together, as shown in FIG. **9**, results in a reduced effective termination resistance for the DQS pins **212**, **214**. For example, for the exemplary configuration of FIG. **9**, the effective termination resistance for the DQS pins **212**, **214** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **252**, **254** of the two memory devices **210**, **220** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

FIG. **10** schematically illustrates an exemplary memory module **300** in accordance with certain embodiments described herein. The memory module **300** comprises a first memory device **310** having a first data strobe (DQS) pin **312** and a second memory device **320** having a second data strobe (DQS) pin **322**. The memory module **300** further comprises a first resistor **330** electrically coupled to the first DQS pin **312**. The memory module **300** further comprises a second resistor **340** electrically coupled to the second DQS pin **322** and to the first resistor **330**. The first DQS pin **312** is electrically coupled to the second DQS pin **322** through the first resistor **330** and through the second resistor **340**.

In certain embodiments, the memory module **300** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. **11**A and **11**B schematically illustrate a first side **362** and a second side **364**, respectively, of such a memory module **300** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **360**. In certain embodiments, the memory module **300** further comprises a phase-lock-loop (PLL) clock driver **370**, an EEPROM for serial-presence detect (SPD) data **380**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **300** allow precise control of data transfer between the memory module **300** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **300** are suitable for a variety of high-performance system applications.

In certain embodiments, the memory module **300** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **310** and a second memory device **320**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **300** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **310** of each pair has the first DQS pin **312** electrically coupled to the second DQS pin **322** of the second memory device **320** of the pair. In addition, the first DQS pin **312** and the second DQS pin **322** are concurrently active when the first memory device **310** and the second memory device **320** are concurrently enabled.

In certain embodiments, the first resistor **330** and the second resistor **340** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **312** and the second DQS pin **322** while allowing signals to propagate between the memory controller and the DQS pins **312**, **322**. In certain embodiments, each of the first resistor **330** and the second resistor **340** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **330** and the second resistor **340** has a resistance of approxi-

mately 22 ohms. Other resistance values for the first resistor **330** and the second resistor **340** are also compatible with embodiments described herein. In certain embodiments, the first resistor **330** comprises a single resistor, while in other embodiments, the first resistor **330** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **340** comprises a single resistor, while in other embodiments, the second resistor **340** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

FIGS. **12**A and **12**B schematically illustrate an exemplary embodiment of a memory module **300** in which the first resistor **330** and the second resistor **340** are used to reduce the current flow between the first DQS pin **312** and the second DQS pin **322**. As schematically illustrated by FIG. **12**A, the memory module **300** is part of a computer system **400** having a memory controller **410**. The first resistor **330** has a resistance of approximately 22 ohms and the second resistor **340** has a resistance of approximately 22 ohms. The first resistor **330** and the second resistor **340** are electrically coupled in parallel to the memory controller **410** through a signal line **420** having a resistance of approximately 25 ohms. The first resistor **330** and the second resistor **340** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. **12**A and **12**B) by a signal line **440** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

FIG. **12**B schematically illustrates exemplary current-limiting resistors **330**, **340** in conjunction with the impedances of the memory devices **310**, **320**. During an exemplary portion of a data read operation, the memory controller **410** is in a high-impedance condition, the first memory device **310** drives the first DQS pin **312** high (e.g., 2.7 volts), and the second memory device **320** drives the second DQS pin **322** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. **8**, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

In certain embodiments, as schematically illustrated by FIG. **12**B, the DQS driver of the first memory device **310** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **320** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **310** and the first resistor **330** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **320** and the second resistor **340** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. **12**B is approximately zero.

The voltage at the second DQS pin **322** in FIG. **12**B is given by V_{DQS2}=//2.7*R_4/(R_1+R_2+R_3+R_4)=0.59 volts and the current flowing through the second DQS pin **322** is given by I_{DQS2}=0.59/R_4=34 milliamps. The power dissipation in the DQS driver of the second memory device **320** is thus P_{DQS2}=34 mA*0.59 V=20 milliwatts. In contrast, without the first resistor **330** and the second resistor **340**, only the 17-ohm impedances of the two memory devices **310**, **320** would limit the current flow between the two DQS pins **312**, **322**, and the power dissipation in the DQS driver of the second memory device **320** would be approximately 107 milliwatts. Therefore, the first resistor **330** and the second resistor **340** of FIGS. **12**A and **12**B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **330** and the second resistor **340** are advantageously selected to account for such overshoot/undershoot of voltages.

For certain such embodiments in which the voltage at the second DQS pin **322** is V_{DQS2}=0.59 volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

FIG. **13** schematically illustrates another exemplary memory module **500** compatible with certain embodiments described herein. The memory module **500** comprises a termination bus **505**. The memory module **500** further comprises a first memory device **510** having a first data strobe pin **512**, a first termination signal pin **514** electrically coupled to the termination bus **505**, a first termination circuit **516**, and at least one data pin **518**. The first termination circuit **516** selectively electrically terminating the first data strobe pin **512** and the first data pin **518** in response to a first signal received by the first termination signal pin **514** from the termination bus **505**. The memory module **500** further comprises a second memory device **520** having a second data strobe pin **522** electrically coupled to the first data strobe pin **512**, a second termination signal pin **524**, a second termination circuit **526**, and at least one data pin **528**. The second termination signal pin **524** is electrically coupled to a voltage, wherein the second termination circuit **526** is responsive to the voltage by not terminating the second data strobe pin **522** or the second data pin **528**. The memory module **500** further comprises at least one termination assembly **530** having a third termination signal pin **534**, a third termination circuit **536**, and at least one termination pin **538** electrically coupled to the data pin **528** of the second memory device **520**. The third termination signal pin **534** is electrically coupled to the termination bus **505**. The third termination circuit **536** selectively electrically terminates the data pin **528** of the second memory device **520** through the termination pin **538** in response to a second signal received by the third termination signal pin **534** from the termination bus **505**.

FIG. **14** schematically illustrates a particular embodiment of the memory module **500** schematically illustrated by FIG. **13**. The memory module **500** comprises an on-die termination (ODT) bus **505**. The memory module **500** comprises a first memory device **510** having a first data strobe (DQS) pin **512**, a first ODT signal pin **514** electrically coupled to the ODT bus **505**, a first ODT circuit **516**, and at least one data (DQ) pin **518**. The first ODT circuit **516** selectively electrically terminates the first DQS pin **512** and the DQ pin **518** of the first memory device **510** in response to an ODT signal received by the first ODT signal pin **514** from the ODT bus **505**. This behavior of the first ODT circuit **516** is schematically illustrated in FIG. **14** by the switches **572**, **576** which are selectively closed (dash-dot line) or opened (solid line).

The memory module **500** further comprises a second memory device **520** having a second DQS pin **522** electrically

coupled to the first DQS pin **512**, a second ODT signal pin **524**, a second ODT circuit **526**, and at least one DQ pin **528**. The first DQS pin **512** and the second DQS pin **522** are concurrently active when the first memory device **510** and the second memory device **520** are concurrently enabled. The second ODT signal pin **524** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **526** is responsive to the voltage by not terminating the second DQS pin **522** or the second DQ pin **524**. This behavior of the second ODT circuit **526** is schematically illustrated in FIG. **14** by the switches **574**, **578** which are opened.

The memory module **500** further comprises at least one termination assembly **530** having a third ODT signal pin **534** electrically coupled to the ODT bus **505**, a third ODT circuit **536**, and at least one termination pin **538** electrically coupled to the DQ pin **528** of the second memory device **520**. The third ODT circuit **536** selectively electrically terminates the DQ pin **528** of the second memory device **520** through the termination pin **538** in response to an ODT signal received by the third ODT signal pin **534** from the ODT bus **505**. This behavior of the third ODT circuit **536** is schematically illustrated in FIG. **14** by the switch **580** which is either closed (dash-dot line) or opened (solid line).

In certain embodiments, the termination assembly **530** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **500**. In certain other embodiments, the termination assembly **530** comprises an integrated circuit mounted on the printed-circuit board of the memory module **500**. Persons skilled in the art can provide a termination assembly **530** in accordance with embodiments described herein.

Certain embodiments of the memory module **500** schematically illustrated by FIG. **14** advantageously avoid the problem schematically illustrated by FIG. **7** of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. **9**, FIGS. **13** and **14** only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **516**, the second ODT circuit **526**, and the third ODT circuit **536** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **516**, the second ODT circuit **526**, and the third ODT circuit **536** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **572**, **574**, **576**, **578**, **580** of FIG. **14** are schematic representations of the enabling and disabling operation of the ODT circuits **516**, **526**, **536** and do not signify that the ODT circuits **516**, **526**, **536** necessarily include mechanical switches.

The first ODT signal pin **514** of the first memory device **510** receives an ODT signal from the ODT bus **505**. In response to this ODT signal, the first ODT circuit **516** selectively enables or disables the termination resistance for both the first DQS pin **512** and the DQ pin **518** of the first memory device **510**. The second ODT signal pin **524** of the second memory device **520** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **554**, **558** on the second DQS pin **522** and the second DQ pin **528**, respectively, of the second memory device **520** (schematically shown by open switches **574**, **578** in FIG. **14**). The second DQS pin **522** is electrically coupled to the first DQS pin **512**, so the termination resistance for both the first DQS pin **512** and the second DQS pin **522** is provided by the termination resistor **552** internal to the first memory device **510**.

The termination resistor **556** of the DQ pin **518** of the first memory device **510** is enabled or disabled by the ODT signal received by the first ODT signal pin **514** of the first memory device **510** from the ODT bus **505**. The termination resistance of the DQ pin **528** of the second memory device **520** is enabled or disabled by the ODT signal received by the third ODT signal pin **534** of the termination assembly **530** which is external to the second memory device **520**. Thus, in certain embodiments, the first ODT signal pin **514** and the third ODT signal pin **534** receive the same ODT signal from the ODT bus **505**, and the termination resistances for both the first memory device **510** and the second memory device **520** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **500** schematically illustrated by FIG. **14** provides external or off-chip termination of the second memory device **520**.

Certain embodiments of the memory module **500** schematically illustrated by FIG. **14** advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **500**.

Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic

element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

2. The memory module of claim **1**, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

3. The memory module of claim **1**, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4. The memory module of claim **3**, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5. The memory module of claim **1**, wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column address signals to the plurality of DDR memory devices during a subsequent column access procedure.

6. The memory module of claim **1**, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

7. The memory module of claim **1**, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8. The memory module of claim **1**, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9. The memory module of claim **1**, wherein the register comprises a plurality of register devices.

10. The memory module of claim **1**, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11. The memory module of claim **10**, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12. The memory module of claim **1**, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

13. The memory module of claim **12**, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14. The memory module of claim **1**, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

16. The memory module of claim **15**, wherein the command signal is transmitted to only one DDR memory device at a time.

17. The memory module of claim **16**, wherein the command signal comprises a read command signal.

18. The memory module of claim **15**, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19. The memory module of claim **18**, wherein the command signal comprises a refresh command signal.

20. The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21. The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

22. The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

23. The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure and to transmit the stored input signal as an output signal of the set of output signals during a subsequent column access procedure.

24. The memory module of claim 15, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

25. The memory module of claim 15, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

26. The memory module of claim 25, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

27. The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register.

29. The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

30. The memory module of claim 29, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

31. The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

32. The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

33. The memory module of claim 28, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

34. The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35. The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36. The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37. The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38. The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the

plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank.

40. The memory module of claim **39**, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

41. The memory module of claim **39**, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

42. The memory module of claim **39**, wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices.

43. The memory module of claim **42**, wherein the logic element receives the second number of chip-select signals.

44. The memory module of claim **43**, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

45. The memory module of claim **39**, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

46. The memory module of claim **39**, wherein the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank.

47. The memory module of claim **39**, wherein the DDR memory devices of the second rank are spaced from the DDR memory devices of the first rank in a direction along the first side.

48. The memory module of claim **39**, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of the printed circuit board.

49. The memory module of claim **39**, wherein the plurality of input signals corresponds to a first memory density, and the plurality of output signals corresponds to a second memory density, the second memory density greater than the first memory density.

50. The memory module of claim **39**, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.

51. The memory module of claim **39**, wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,619,912 B2
APPLICATION NO. : 11/862931
DATED : November 17, 2009
INVENTOR(S) : Bhakta et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, at page 3 (item 56), column 1, line 29, under Other Publications, please delete "Komaros" and insert -- Kornaros --.

Title Page, at page 3 (item 56), column 1, line 49, under Other Publications, please delete "IPCOM00008164D," and insert -- IPCOM000008164D, --.

Title Page, at page 3 (item 56), column 2, line 18, please delete ""Continuou" and insert -- "Continuous --.

At sheet 4 of 18 (Figure 2B), line 2, please delete "A12" and insert -- A_{12} --.

At column 1, line 55, please delete "230" and insert -- 2^{30} --.

At column 1, line 58, please delete "230" and insert -- 2^{30} --.

At column 17, line 27, please delete "ens fet3b = dqs cyc b | dqs ncyc b ;" and insert -- ens_fet3b = dqs_cyc_b | dqs_ncyc_b; --.

At column 29, line 59, please delete ""//2.7*R_4" and insert -- 2.7*R_4 --.

Signed and Sealed this

Tenth Day of August, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

US007619912C1

(12) **INTER PARTES REEXAMINATION CERTIFICATE** (1643rd)
United States Patent
Bhakta et al.

(10) **Number: US 7,619,912 C1**
(45) **Certificate Issued: Feb. 8, 2021**

(54) **MEMORY MODULE DECODER**

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(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)

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Reexamination Certificate for:
Patent No.: **7,619,912**
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Related U.S. Application Data

(63) Continuation of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, and a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004.

(51) **Int. Cl.**

G11C 15/02	(2006.01)
G11C 7/10	(2006.01)
H05K 1/14	(2006.01)
G11C 8/12	(2006.01)
G06F 12/02	(2006.01)
G11C 5/04	(2006.01)
G11C 5/06	(2006.01)
H05K 1/18	(2006.01)

(52) **U.S. Cl.**
CPC ***G11C 8/12*** (2013.01); ***G06F 12/0207*** (2013.01); ***G06F 12/0215*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 7/1048*** (2013.01); ***H05K 1/181*** (2013.01); *G11C 2207/105* (2013.01); *H05K 2201/10159* (2013.01); *H05K 2203/1572* (2013.01); *Y02P 70/50* (2015.11)

(58) **Field of Classification Search**
None
See application file for complete search history.

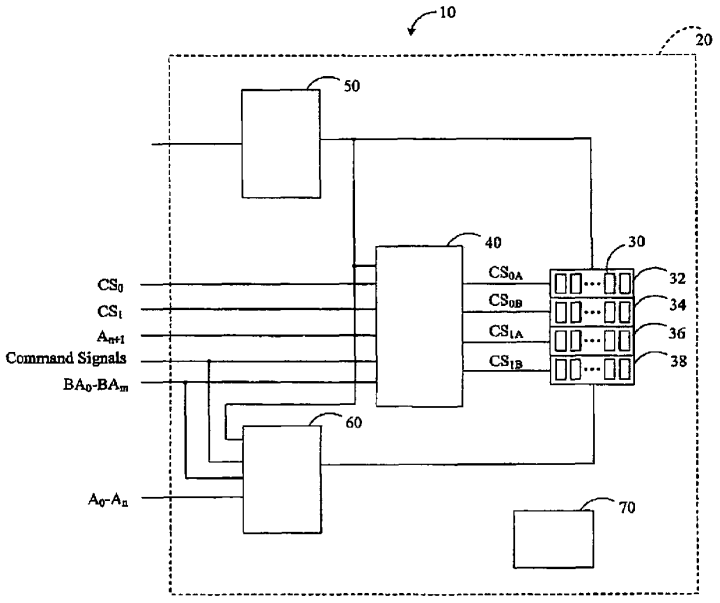
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceedings for Reexamination Control Numbers 95/001,339, 95/000,578 and 95/000,579, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — B. James Peikari

(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.



INTER PARTES REEXAMINATION CERTIFICATE

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **2**, **5**, **7**, **9**, **21**, **23**, **25**, **26**, **30**, **33**, **42**, **44** and **51** are cancelled.

Claims **1**, **15**, **16**, **28**, **39** and **43** are determined to be patentable as amended.

Claims **3**, **4**, **6**, **8**, **10-14**, **17-20**, **22**, **24**, **27**, **29**, **31**, **32**, **34-38**, **40**, **41** and **45-50**, dependent on an amended claim, are determined to be patentable.

New claims **52-91** are added and determined to be patentable.

1. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

15. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are

separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals and (iii) the at least one chip-select signal of the set of input signals and (iv) the PLL clock signal.

16. **[**The memory module of claim **15]** *A memory module connectable to a computer system, the memory module comprising:*

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

28. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal.

39. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives *at least one row address signal,* the bank address signals, *at least one chip-select signal,* and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one

rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals, and (iii) transmits the buffered bank address signals and the buffered row address signals to the at least one DDR memory device of the selected at least one rank, and wherein the plurality of the row address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the plurality of input signals and (iv) the PLL clock signal.

43. The memory module of claim **[42]** *39*, wherein the logic element receives the second number of chip-select signals.

52. The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

53. The memory module of claim 52, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

54. The memory module of claim 53, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

55. The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

56. The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

57. The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density.

58. The memory module of claim 1, wherein the register comprises a plurality of register devices.

59. The memory module of claim 1, wherein the chip-select signals generated by the logic element are a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

60. The memory module of claim 59, wherein the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

61. The memory module of claim 60, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

62. The memory module of claim 60, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

63. The memory module of claim 1, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

64. The memory module of claim 15, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per

DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

65. The memory module of claim 64, wherein the one or more attributes comprise the number or ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

66. The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

67. The memory module of claim 66, wherein the command signal comprises a read command signal.

68. The memory module of claim 15, wherein the logic element receives the command signal from the computer system and the register receives the command signal from the computer system.

69. The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices.

70. The memory module of claim 69, wherein the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank and the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has.

71. The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

72. The memory module of claim 28, wherein the register receives the input command signal of the set of input control signals.

73. The memory module of claim 39, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from one or more attributes of the plurality of DDR memory devices.

74. The memory module of claim 73, wherein the one or more attributes comprises the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

75. The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

76. The memory module of claim 43, wherein both the register and the logic element receive at least one command signal of the plurality of input signals.

77. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller thank the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buff-

ered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

78. The memory module of claim 77, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

79. The memory module of claim 78, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

80. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board:

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks:

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks,

wherein the bank address signals of the set of input control signals are received by the logic element,

wherein a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device.

81. The memory module of claim 80, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

82. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the

computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

83. The memory module of claim 82, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

84. The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

85. The memory module of claim 82, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

86. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals.

87. The memory module of claim 86, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

88. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

89. The memory module of claim 88, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

90. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives at least one row address signal, the bank address signals, the second number of chip-select signals, and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein, in responsive to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals, and (iii) transmits the buffered bank address signals and the buffered plurality of row address signals to the at least one DDR memory device of the selected at least one rank, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of the row address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals.

91. The memory module of claim 90, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

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FORM 19. Certificate of Compliance with Type-Volume Limitations **Form 19**
July 2020

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2024-2304

Short Case Caption: Netlist, Inc. v. Samsung Electronics Co., Ltd.

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