No. 2024-2304

IN THE
UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

NETLIST, INC.,
Appellant,

v.

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC,
Appellees.

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in Nos. IPR2022-00615, IPR2023-00203

APPELLEES' RESPONSE BRIEF

May 30, 2025

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PATENT CLAIM LANGUAGE AT ISSUE

U.S. Patent No. 7,619,912

Original Claims 15 & 16 (Appx97)	Challenged Claim 16 (Appx103)
15. A memory module connectable to a computer system, the memory module comprising:	**16.** [16.pre] A memory module connectable to a computer system, the memory module comprising:
a printed circuit board;	[16.a] a printed circuit board;
a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,	[16.b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,
the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;	[16.b.i] the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,	[16.c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,
the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,	[16.c.i] the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,
the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,	[16.c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,

Original Claims 15 & 16 (Appx97)	Challenged Claim 16 (Appx103)
the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,	[16.c.iii] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,
wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and	[16.c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
a phase-lock loop device coupled to the printed circuit board,	[16.d] a phase-lock loop device coupled to the printed circuit board,
the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.	[16.d.i] the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
16. The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.	[16.e] wherein the command signal is transmitted to only one DDR memory device at a time.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 2024-2304

Short Case Caption Netlist, Inc. v. Samsung Electronics Co., Ltd.

Filing Party/Entity Samsung Electronics Co., Ltd.

Instructions:

1. Complete each section of the form and select none or N/A if appropriate.
2. Please enter only one item per box; attach additional pages as needed, and check the box to indicate such pages are attached.
3. In answering Sections 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance.
4. Please do not duplicate entries within Section 5.
5. Counsel must file an amended Certificate of Interest within seven days after any information on this form changes. Fed. Cir. R. 47.4(c).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 09/25/2024

Signature: /s/ Michael Hawes

Name: Michael Hawes

1. Represented Entities. Fed. Cir. R. 47.4(a)(1).	**2. Real Party in Interest.** Fed. Cir. R. 47.4(a)(2).	**3. Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3).
Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities. ☐ None/Not Applicable	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities. ☑ None/Not Applicable
Samsung Electronics Co., Ltd.	Samsung Semiconductor, Inc.	

☐ Additional pages attached

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

☐ None/Not Applicable ☐ Additional pages attached

Brianna Potter Baker Botts L.L.P.	Ferenc Pazmandi Baker Botts L.L.P.	Eric Faragi Baker Botts L.L.P.

5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

☑ Yes (file separate notice; see below) ☐ No ☐ N/A (amicus/movant)

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). **Please do not duplicate information.** This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

☑ None/Not Applicable ☐ Additional pages attached

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 24-2304

Short Case Caption Netlist, Inc. v. Samsung Electronics Co., Ltd.

Filing Party/Entity Micron Technology, Inc., Micron Semiconductor Products, Inc., Micron Technology Texas, LLC

Instructions:

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I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 09/25/2024

Signature: /s/ E. Joshua Rosenkranz

Name: E. Joshua Rosenkranz

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Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities. ☑ None/Not Applicable	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities. ☐ None/Not Applicable
Micron Technology, Inc.		None
Micron Semiconductor Products, Inc.		Micron Technology, Inc.
Micron Technology Texas, LLC		Micron Technology, Inc.

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☐ None/Not Applicable ☐ Additional pages attached

Winston & Strawn LLP	Matthew Hopkins	Ryuk Park

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☑ None/Not Applicable ☐ Additional pages attached

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

Regulations

STATEMENT OF RELATED CASES

No appeal in or from the same action was previously before this or any other appellate court. Below are cases known to counsel to be pending in any tribunal that will directly affect or be directly affected by this Court's decision in the pending appeal:

1. *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 25-1286 (Fed. Cir.) (appeal of IPR2023-00455 and IPR2023-01142 (PTAB))
2. *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 25-1296 (Fed. Cir.) (appeal of IPR2023-00454 and IPR2023-01141 (PTAB))
3. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2:22-cv-00293 (E.D. Tex.)
4. *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00294 (E.D. Tex.)
5. *Netlist, Inc. v. Google LLC*, No. 3:09-cv-05718 (N.D. Cal.)
6. *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No 1:21-cv-01453 (D. Del.)
7. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993 (C.D. Cal.)

On January 21, 2025, this Court ordered that this appeal and the following related appeals be treated as companion cases and assigned to the same merits panel: Nos. 25-1286 and 25-1296 (above). *See* ECF No. 22.

STATEMENT OF THE ISSUES

1. Whether the Board correctly construed "*rank*" in claim 16 to cover one or more memory devices, rejecting Netlist's "two or more" proposal, where

- claim 16 does not specify the number of memory devices in a rank, and the Board identified several one-device-per-rank embodiments;
- claim 16 only uses "*plurality of*" to introduce a different limitation; and
- the previous reexamination did not construe "*rank*" and merely distinguished prior art teaching "a plurality of memory devices in a rank."

2. Whether the Board had substantial evidence to determine that Ellsberry teaches single-device ranks.

3. Whether the Board had substantial evidence to determine that neither of the applications Netlist identified as the basis for earlier priority had written description support for claim 16.

INTRODUCTION

The Board's determination that claim 16 of the '912 patent is unpatentable for obviousness was the product of a thorough analysis, which cannot be dismissed as Petitioner's lucky draw. The Board carefully considered the patent, the prior art,

and the earlier reexamination proceeding to reach a reasoned, fully explained decision entirely consistent with prior rulings.

The sole legal issue Netlist raises is a challenge to the Board's construction of "*rank*" as encompassing ***one*** or more memory devices. Netlist insists a "*rank*" must have ***two*** or more memory devices. But the claim language broadly recites, without restriction, a first or second "*number of DDR memory devices*" in a rank. The written description is similarly unconstrained and actually discloses single-device ranks. By contrast, the use of "*plurality of*" for another limitation of claim 16 shows that Netlist claimed a "plurality" when it wanted to do so. The decision not to do so for devices in a rank strongly supports the Board's construction.

Netlist's principal contention is that it disclaimed single-device ranks from claim 16 during reexamination because, Netlist says, the Board adopted that narrower construction and Netlist acquiesced. But the Board correctly determined that it never construed "*rank*" during reexamination; it merely found that the Amidi prior-art reference—which discloses multiple memory devices in a rank—did not disclose all limitations in claim 16. The Board's acknowledgement of Amidi's multiple-device ranks during reexamination is consistent with the Board's construction here allowing ranks to have one or more memory devices. The reexamination does not support Netlist.

Separate from its claim construction challenge, Netlist seeks reassessment of amply supported facts. First, as to whether Ellsberry teaches claim 16 by disclosing single-device ranks, Netlist comes nowhere close to overcoming substantial-evidence review, given that Ellsberry expressly discusses and illustrates a memory module containing single-device ranks. It is irrelevant that a previous Board decision concerning a different patent found that Ellsberry also discloses a different embodiment with multi-device ranks. Second, Netlist asserts that the Court must adopt Netlist's view of how the written description of its earlier applications should be supplemented by various "understandings" to achieve an earlier priority date for the '912 patent. However, the Board's decision rejecting an earlier priority date reasonably found that claim 16's limitations were not described in the earlier applications. For example, the earlier '436 patent application and '244 provisional conspicuously omit the claimed "*register*" and "*bank address signals*," respectively, in stark contrast to their express disclosure in the later '912 patent application. There is no basis to reweigh those factual findings on appeal.

Netlist chalks up its loss to a game of chance, but in fact, the Board's decision rests on solid reasoning and evidence. This Court should affirm.

STATEMENT OF THE CASE

I. There was a known motivation to replace one high-density memory device with multiple (cheaper) low-density memory devices, resulting in similar patent applications by Amidi, Ellsberry, and Netlist

The similarity between Netlist's '912 patent and the prior art is no coincidence. In the early 2000s, before the '912 patent was filed, there was a remarkable pricing disparity in the market for memory devices: "[H]igher-density DRAM devices (e.g., 1-Gb DRAM devices) are ***much more*** than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices)." Appx82 (4:59-62).[1] This created an obvious "economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices." Appx83 (5:3-5).

Many people recognized this motivation to replace one expensive memory device with two cheaper memory devices, including inventors named Amidi and Ellsberry, which explains the close similarity between the prior art and Netlist's later '912 patent. Appx13229-30. Amidi applied for a patent on January 5, 2004, before Netlist. Appx11867. Amidi recognized, before Netlist, that "[b]ecause memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices." Appx11878 ¶ [0008]. Ellsberry also recognized, before Netlist filed the

[1] All emphasis added unless otherwise noted.

application for the ’912 patent, the benefit of “making two smaller-capacity memory devices emulate a single higher-capacity memory device.” Appx11884 (Abstract).

II. The “chip-select” (CS) signal is used to select a “rank” of one or more memory chips

Both Amidi and Ellsberry taught that when replacing one high-density memory device with two low-density memory devices, the two low-density memory devices should receive ***different*** chip-select signals (often abbreviated “CS”). *See, e.g.*, Appx11870 (“cs0” and “cs2”); Appx11901 (“CS0A” and “CS0B”).

The chip-select signal is related to the concept of a “rank,” and is sometimes called a “rank-select signal[],” as recognized by the ’912 patent. Appx81 (2:37-39) (“rank-select signals, also called chip-select signals”); *see also* Appx11193 (“CS . . . Chip Select . . . provides for external ***Rank*** selection”). But the chip-select signal is also “part of the command code,” Appx11193, meaning that any memory chip performing a “Read” or “Write” command needs to receive a chip-select (CS) signal (in combination with several other signals called RAS, CAS, WE, and CKE):

Table 10 — Command truth table.

Function	CKE		CS	RAS	CAS	WE	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Device Deselect	H	X	H	X	X	X	X	X	X	X	1

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Appx21148 (annotating Appx11236). As shown above, if the chip-select (CS) signal is Low (L), then a read or write command is performed by that memory device, but if the chip-select (CS) signal is High (H), then that memory device is "Deselect[ed]" and does not perform a read or write command.

In summary, if a given chip-select signal (also called rank-select signal) is connected to only one memory device, then only that device will be selected to perform a read or write command when the signal is Low. That is an example of a "rank" with just one memory device. If a given chip-select signal is connected to ***two*** memory devices, then both of those devices will be selected to perform the command when the signal is Low. That is an example of a "rank" with two memory devices. And so on. Thus, as explained by the Jacob textbook cited repeatedly by Netlist in its brief, "a *rank* of memory is a '*bank*' of ***one or more*** DRAM devices

that operate in lockstep in response to a given command. . . . [S]ometimes as few as ***one*** device per rank." Appx11702-03.

III. Ellsberry used the term "bank" to describe a "rank"

Ellsberry used the term "bank" to describe a "rank," consistent with the common usage of "bank" at the time. *See, e.g.*, Appx11908 ¶ [0055] ("two memory banks 1206 & 1208"). But "bank" was also sometimes used in the industry to refer to other things (such as internal parts of a memory chip) that are not a "rank." *See, e.g.*, Appx13076-78 ¶ 76. So, as explained by the Jacob textbook, the industry started using the term "rank" to "lessen the confusion associated with overloading" the term "bank." Appx11702. That is why the Jacob textbook states that "a *rank* of memory is a '***bank***' of ***one or more*** DRAM devices that operate in lockstep in response to a given command." *Id.* The Jacob textbook provides the following illustration, where the term "bank" in the upper right is crossed out and replaced with the term "rank" to identify the memory devices connected to a given chip-select signal:

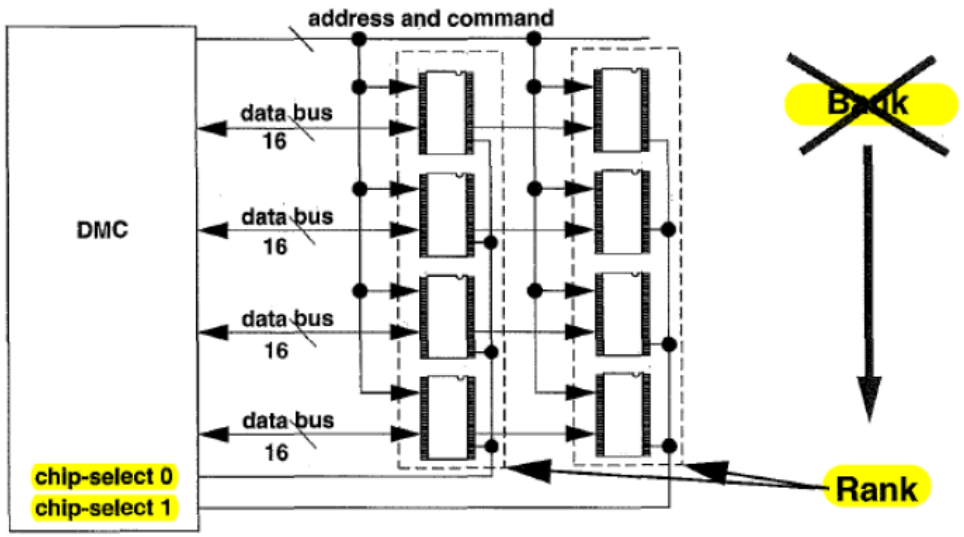


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

Appx11702 (yellow highlighting added). Professor Jacob also published a paper in 2002 that used the term "rank" rather than "bank." Appx11810-12, Appx11817.

This shift in terminology eventually made its way to JEDEC, the industry consortium. For example, the JEDEC standard for DDR SDRAM memory devices first published in 2000 used the term "bank." *See* Appx11271, Appx20270 ("Chip Select . . . provides for external ***bank*** selection"). But with the release of the second generation of that standard in 2003, JEDEC adopted the term "rank" to mean the same thing, consistent with Professor Jacob's explanation above. *See* Appx11193 ("Chip Select . . . provides for external ***Rank*** selection").

It is undisputed that Ellsberry discloses "ranks" (called "banks" by Ellsberry). Appx38-39; Appx11908 ¶ [0055]. In particular, Figure 12 of Ellsberry, shown below, illustrates a rank (1206, identified by the chip-select signal CS0A) with just

one memory device (light blue), and a second rank (1208, identified by the chip-select signals CS0B) with just ***one*** memory device (green):

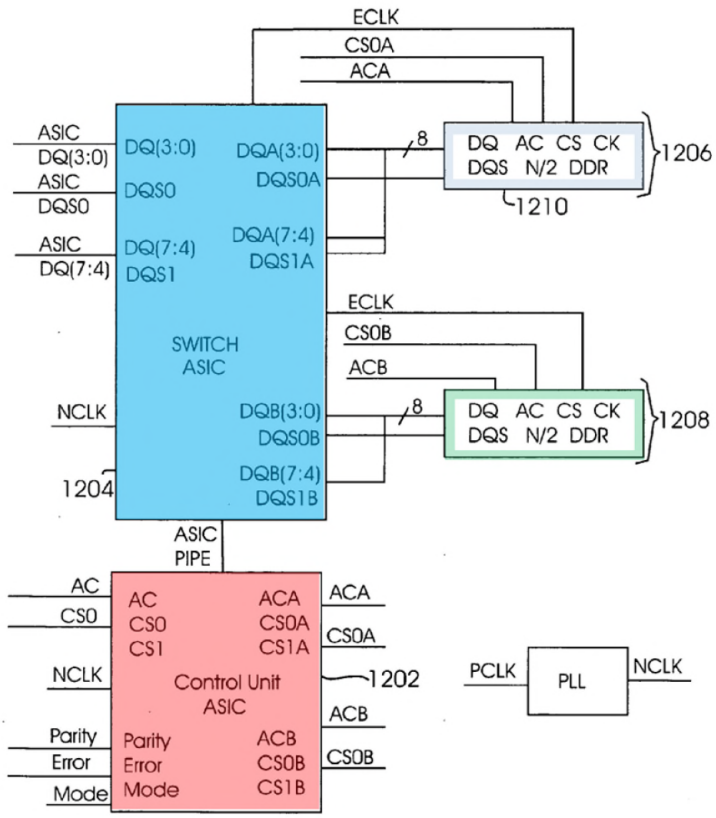


Fig. 12

Appx199 (annotating Appx11901); Appx11908 ¶ [0055]; *see also* Appx13181-85 ¶¶ 214-21. Netlist does not dispute that Ellsberry discloses "ranks," but Netlist contends that there would be ***additional*** memory devices (not shown above) in each "rank" of Ellsberry. *See, e.g.*, Br.51-52. The Board disagreed with Netlist. Appx45-51.

IV. Amidi and Ellsberry taught "rank multiplication" to double the number of chip-select signals on the module, so that two (cheaper) low-density memory devices could replace one (expensive) high-density memory device

As discussed above, both Amidi and Ellsberry taught replacing one (expensive) high-density memory device with two (cheaper) low-density memory devices. They also taught putting logic on the memory module to replace one chip-select signal from the host computer with two chip-select signals on the module—a technique referred to as "rank multiplication" given the relationship between a chip-select signal and a rank. Appx20022-23 (55:9-56:10).

For example, Figure 12 of Ellsberry, reprinted above, shows one chip-select signal (CS0) from the host computer going into the left side of the red "Control Unit," and two chip-select signals (CS0A and CS0B) coming out of the right side and going to the two ranks of memory devices on the upper right (shown outlined in light blue and green). As explained by Ellsberry, "[t]his effectively expands the number of addressable [r]anks per memory module without the need for additional chip select lines on the main memory bus. For example, the invention expands the addressable memory [r]anks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device," while still being "compatible with existing system architectures and transparent to the rest of the system." Appx11905 ¶¶ [0026-27]; *see also* Appx20244; Appx20247; Appx13196-201 ¶¶ 232-36; Appx13203-07 ¶¶ 240-42.

Similarly, Amidi teaches that a "standard" memory module only receives "two chip select signals" from the host computer, Appx11878 ¶¶ [0010-11], but Amidi teaches putting logic on the memory module to double the number of chip-select signals to "four chip select signals (cs0, cs1, cs2, and cs3)," Appx11880 ¶ [0036], corresponding to four ranks of memory devices, Appx11879-80 ¶¶ [0034-35]; Appx11870.

Although Ellsberry and Amidi share many similarities, one difference is that Ellsberry discloses an example of a single-device rank, as discussed above, while Amidi only discloses examples of "ranks" with ***multiple*** memory devices in each rank. *See, e.g.*, Appx11870 (chip-select signal "cs0" connected to ***both*** memory devices "U1" and "U9" in "First Rank"); Appx11879 ¶ [0034] ("first rank 304 of memory devices 306 (U1 through U9)").

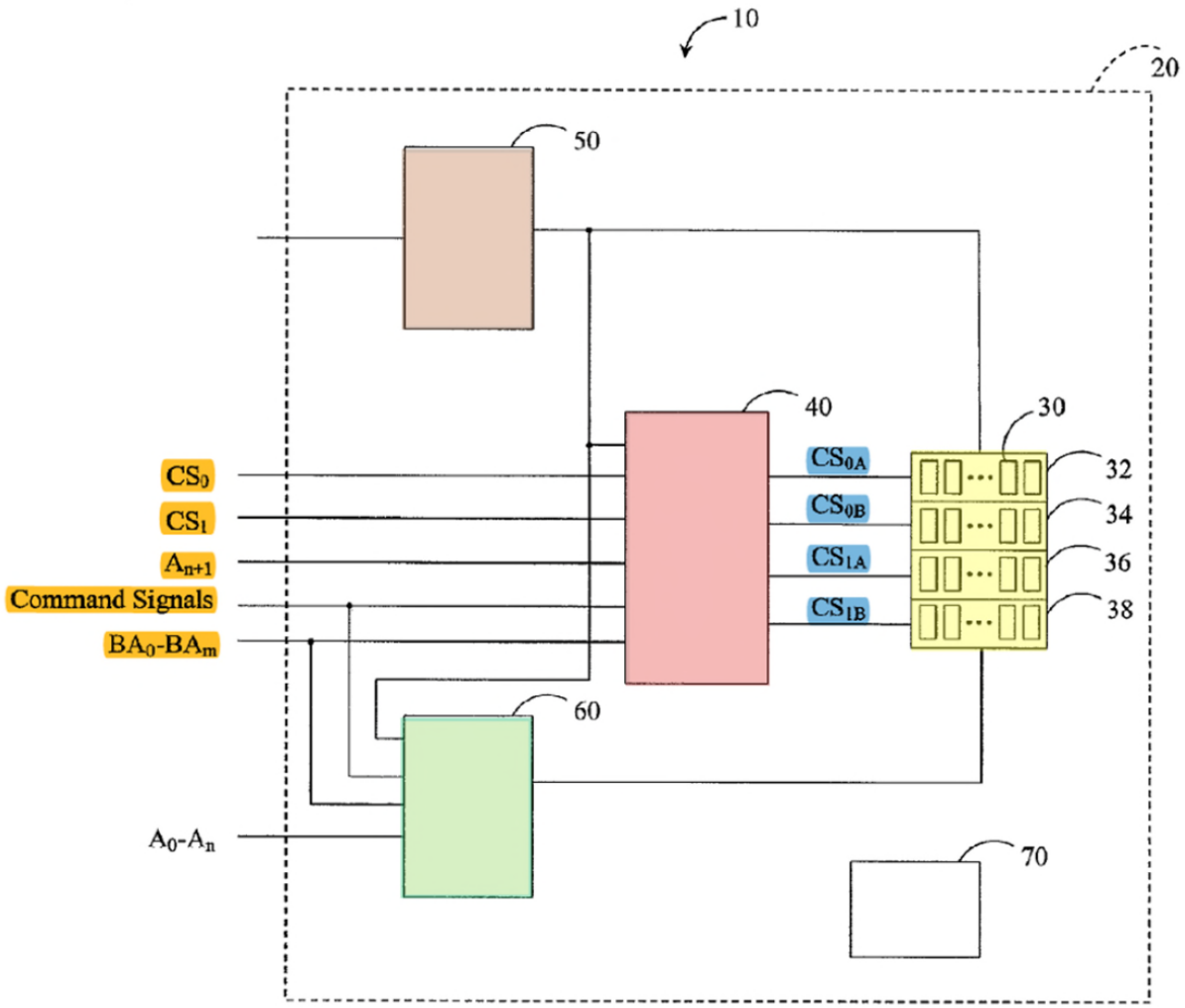
V. Netlist's '912 patent, filed after Amidi and Ellsberry, also disclosed "rank multiplication"

On July 1, 2005—one month after Ellsberry's application and over a year after Amidi's application—Netlist filed an application ultimately leading to the '912 patent. Appx60.

Like Amidi and Ellsberry, the '912 patent teaches replacing one high-density memory device with two cheaper low-density memory devices, Appx83 (5:1-5), and replacing one chip-select signal from the host computer with two chip-select signals on the memory module—which Netlist calls "rank multiplication," Br.10-11.

Figure 1A of the ’912 patent, shown below, is remarkably similar to Amidi, because it teaches a logic element 40 (red) that receives two chip-select signals from the left (CS_0 and CS_1 in orange)—designed to control ***two*** ranks of memory devices—and outputs four chip-select signals on the right (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} in blue)—which control ***four*** ranks (32, 34, 36, 38), with each rank including multiple memory devices (30, yellow):

Figure 1A:



Appx136 (annotating Appx63); Appx84 (7:35-54); Appx7-8. In Figure 1A above, the green box (60) is a "register," and the brown box (50) is a "phase-lock loop" (PLL) device. Appx83 (5:22-25).

Figure 1A above is an embodiment corresponding to original claim 15 of the '912 patent, which as discussed below was rejected during reexamination in light of Amidi in combination with JEDEC standards. However, Figure 1A above does ***not*** disclose claim 16—which originally depended from claim 15 and survived reexamination—because Figure 1A does not disclose the last limitation [16.e] requiring that "the command signal is transmitted to ***only one*** DDR memory device at a time." Appx103 (3:42-43). Instead Figure 1A shows the register 60 (green) transmitting the same command and address signals to ***all*** of the memory devices 30, and shows the logic element 40 (red) transmitting each chip select signal (e.g., CS_{0A}, blue) to ***all*** of the memory devices 30 in a given rank (e.g., rank 32, yellow). Appx20139-40 (172:15-173:23). The only disclosed embodiment in the '912 patent that transmits the command signal "to ***only one*** DDR memory device at a time," as required by claim 16, is an embodiment with just ***one*** memory device in each rank (similar to Figure 12 of Ellsberry). *See* Appx21153; Appx15-18 (discussing Appx84 (8:48-60)); Appx1016, Appx1021 ([16.e]).

VI. Reexamination of the ’912 patent by third parties

After the ’912 patent issued in November 2009, Netlist quickly asserted it (but not claim 16) against third parties, including Google. Appx12809 (1:3-23). Those lawsuits resulted in an *inter partes* reexamination of the ’912 patent, Appx12811 (3:3-20), including (as relevant to this appeal) claims 15 and 16, Appx10487. Micron and Samsung, the Appellees here, were not involved in that litigation or the resulting reexamination.

In the reexamination, Netlist admitted that “Amidi is probably the closest reference to the claims of the ’912 patent,” Appx4011, but Ellsberry was never substantively considered, apparently due to the mistaken belief that Ellsberry was not prior art because it was “filed after the [’912 patent] application’s earliest effective filing date,” Appx2210; Appx470, Appx486-88. As a result, the focus of the reexamination was on Amidi (alone and in combination with other references).

During reexamination, original claim 15 (from which claim 16 originally depended, Appx97) was found obvious over Amidi in view of certain JEDEC standards. Appx5410-14. That rejection resulted in extensive amendments to claim 15 (among other claims). Appx102-03 (2:52-3:8).

However, dependent claim 16—with limitation [16.e] requiring “the command signal is transmitted to ***only one*** DDR memory device at a time”—was ***not*** found obvious over Amidi. The Board made factual findings during the

reexamination, shown below, that Amidi (like Figure 1A of the '912 patent discussed above) discloses ***multiple*** memory devices in each rank, meaning any read or write command would be sent to ***all*** those memory devices at a time, rather than "only one . . . at a time" as required by claim 16. The Board's full discussion includes important text omitted by Netlist (Br.16-17, 21, 32, 34, 37-38):

> Requester 1 argues that Amidi teaches the limitation of "the command signal is transmitted to only one DDR memory device at a time." . . . .
>
> We agree that Amidi teaches using a command signal to read or write . . . . Yet, as the Examiner indicates:
>
> > Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. . . . . The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank.*
>
> RAN 29 [Appx7494] (emphasis added).
>
> That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A-6B (stating "Signals to Memory Devices" at the far right)

Appx10560-61 (emphasis by the Board); Appx11874-75 (Amidi's Figs. 6A and 6B stating "Signals to Memory Device**s**"); Appx11882 (Amidi ¶ 62).

This Court summarily affirmed, *see Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. June 15, 2020), and the reexamination certificate issued in 2021 with claim 16 rewritten in independent form (with no other changes) by adding rejected base claim 15's limitations. Appx101, Appx103 (3:9-43); *see also* Appx6353 (ii); Appx15120 (18:2-8), Appx15130 (28:4-6).

VII. Present IPR proceedings initiated by Samsung and Micron

Netlist did not suggest that Samsung might be infringing the '912 patent until after the reexaminations concluded in 2021, which motivated Samsung to challenge claim 16[2] in the present IPR for the first time. *See* Appx243-45 (citing Appx12918-19 ¶ 14; Appx12925 ¶ 40; Appx12812 (4:5-11); Appx12817-18 (9:14-10:26)).

Samsung filed an IPR petition challenging claim 16 on three grounds: (1) obviousness over Perego (Appx11831); (2) obviousness over the combination of Perego and Amidi; and (3) obviousness over Ellsberry. Appx132; Appx10-11. The Board later joined Micron[3] to the proceedings. Appx21389-92; Appx884.

Netlist contended that Samsung (but not Micron) should be time-barred from seeking *inter partes* review because of its relationship with Google, whom Netlist

[2] All other previously asserted claims of the '912 patent were amended during reexamination and subject to intervening rights, Appx15146 (44:5-10), leaving only claim 16 the subject of the current litigation, Appx15156 (10:4-10), Appx15159 (13:5-15), Appx15163 (17:18-20); Appx15807.

[3] "Micron" refers to Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Appx1 n.1.

had sued for infringement in 2009 as discussed above. Appx473. The Board, after permitting discovery on the issue, rejected Netlist's argument. Appx2-3.

In the Petition, Petitioner proposed that the term "*rank*" should be construed to mean "an independent set of ***one or more*** memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module." Appx140-42; Appx13075-79 ¶¶ 73-77; Appx411-13. Petitioner later proposed the same construction for "*rank*" in a different IPR involving the related '215 patent. In two institution decisions involving the '912 patent, and a third institution decision involving the related '215 patent, the Board preliminarily construed "*rank*" to include ***one*** or more memory devices, agreeing with Petitioner's proposal and rejecting Netlist's proposal requiring ***two*** or more memory devices. Appx490-95 (Oct. 19, 2022); Appx874-76 (June 7, 2023); Appx19941-45 (Aug. 1, 2023). In related litigation, the district court also rejected Netlist's arguments and construed "*rank*" in the '912 and '215 patents to include "one or more" memory devices. Appx20949-52, Appx20973 (Nov. 21, 2023).

In its final written decision, the Board determined that claim 16 of the '912 was unpatentable over Ellsberry, without reaching Grounds 1 and 2 involving Perego, as discussed below. Appx55.

A. Level of ordinary skill in the art

With respect to the level of skill in the art, the Board found in the final written decision (and Netlist does not challenge on appeal) that a POSITA "would have been familiar with various standards of the day, including JEDEC industry standards." Appx12-13. Contrary to Netlist's arguments on appeal that JEDEC ***required*** DDR memory modules to be 64- or 72-bits wide, Br.7-9, 39, the Board found that "JEDEC standards permitted 8-bit and 16-bit wide modules" consistent with Figure 12 of Ellsberry showing an 8-bit-wide memory module with a single x8 (i.e., 8-bit-wide) DDR memory device in each rank. Appx51.

The JEDEC standard cited by the Board, called the "SPD" standard for DRAM modules, Appx20382, is discussed by the '912 patent, Appx85 (9:23-10:55), and consistent with that standard, the '912 patent expressly permits modules ***less*** than 64-bits wide (contrary to Netlist's argument on appeal, Br.7-9, 39): "[M]emory modules . . . having widths of . . . 32 bits . . . as well as other widths . . . are compatible with embodiments described herein." Appx83 (5:60-64). "In addition, memory devices . . . having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein." Appx83 (6:16-19). For example, JEDEC had standardized a 32-bit-wide module with a single x32 (i.e., 32-bit-wide) DDR memory device—a rank with only one memory device. Appx21151 (annotating Appx20427, Appx20433).

B. The Board properly construed "*rank*" to include one or more memory devices

Both parties agreed before the Board that the "dispositive issue for claim construction" is whether the claimed "*rank*" may include only one memory device or whether it must include at least two memory devices. Appx14.

The Board concluded that "the claim term 'rank' may include only one memory device." Appx14-24. The Board determined that the claim language on its face "does not preclude the possibility that a rank could have a single memory device." Appx14-15. Claim 55's additional requirement that each rank comprises a "plurality" of memory devices, when contrasted with claim 16, "implies that each of the ranks [in claims without that requirement] could include a single memory device." Appx15. The Board also determined that the '912 patent discloses embodiments with single-device ranks. Appx15-23. The Board rejected Netlist's arguments that claim 16 is limited to a memory module "compliant with a JEDEC standard" and in any event made factual findings that JEDEC permitted single-device ranks (e.g., one 8-bit memory device on an 8-bit-wide module). Appx51.

Contrary to Netlist's arguments, the Board did not "disregard" the reexamination history discussed above. Br.27, 31-32. The Board specifically considered and rejected Netlist's reexamination-based arguments. *See* Appx23 (referring to the Institution Decision); Appx493-94 (Institution Decision at 31-32). The Board explained that the reexamination did ***not*** state "that claim 16 requires a

plurality of memory devices in a rank." Appx494. Instead, "[t]he Examiner's point was merely that the Requester did not provide a reasonable explanation why one would transmit a command signal to only one DDR memory device at a time when Amidi teaches there are a plurality of memory devices in a rank." *Id.* The Board's conclusion was consistent with its previous conclusion during reexamination. *See supra* p.15 (quoting Appx10561) ("That is, Figures 6A and 6B of Amidi show various command signals . . . being transmitted to more than one memory device.").

The Board also took into account the construction of "*rank*" in district court, *see* 37 C.F.R. § 42.100(b), and concluded that the district court's construction "that 'rank' can include a single memory device . . . is consistent with our discussion of the intrinsic record above." Appx23 (citing Appx20949-52).

C. The Board found Ellsberry discloses a single-device rank, rendering claim 16 obvious

The Board found that Ellsberry discloses all limitations of claim 16. Appx37-51. The Board rejected Netlist's argument that Figure 12 of Ellsberry—which expressly shows ***one*** memory device per rank—actually discloses "***multiple*** memory devices per rank." Appx46. "Petitioner is correct that Ellsberry discloses transmitting a command (Activate, Write or Read) to only the selected one of the two memory devices in Figure 12 . . . ." Appx50; *see also* Appx21206.

D. The Board found no written-description support for claim 16 in the earlier ’436 patent or ’244 provisional (filed before Ellsberry)

The Board rejected Netlist’s arguments that Ellsberry (filed June 1, 2005) is not prior art to claim 16 of the ’912 patent. Appx24-34. Netlist had argued that claim 16 was entitled to the earlier filing date of either the ’244 provisional application filed July 15, 2004 (Appx2335-45), or the ’436 patent filed March 7, 2005 (Appx2482-509) which incorporates the ’668 provisional filed March 5, 2004 (Appx2346-90). The Board found that the ’244 provisional does not provide written description for the claimed “*bank address signals*” and does not disclose using bank address signals for rank multiplication, which, as the Board pointed out, can be done with row or column address signals instead. Appx26-30. The Board found that the ’436 patent does not provide written description for the claimed “*register*.” Appx30-34. The Board also found that Netlist failed to identify support in the ’436 patent for ***all*** limitations of claim 16. Appx33-34.

SUMMARY OF ARGUMENT

The Board properly assessed the claim language, specification, and prosecution history, as well as extrinsic evidence concerning JEDEC standards, to conclude that claim 16's "*rank*" encompasses one or more memory devices. Claim construction starts with the language of the claim, which Netlist's appeal seeks to avoid. Despite the applicants specifying a "*plurality*" in other parts of claim 16, they chose not to impose that limitation on the number of devices in a "*rank*." On its face, the language choices made in claim 16 support the Board's construction. Additionally, the contrast between claims 16 and 55 undermines Netlist's attempt to add a limitation. Claim 55 expressly requires that a "*rank*" consists of multiple memory devices. Netlist would render that language mere surplusage contrary to this Court's teachings.

Turning to the written description, the Board identified multiple disclosures of single-device ranks further supporting its conclusion. Netlist's focus on other examples of multi-device ranks is perfectly consistent with a "one or more" construction and fails to offer any support for importing a "plurality" limitation.

Netlist attempts to overcome all that intrinsic evidence based solely on a discussion in the reexamination—which Netlist mischaracterizes on the critical point. The Board correctly assessed the full language from which Netlist extracts its quotations and properly concluded that the reexamination's treatment of the Amidi

reference did not construe the claim to require multiple-device ranks. Instead, the examiner and Netlist distinguished Amidi on grounds perfectly consistent with the Board's "one or more" construction. Netlist plainly fails to identify any clear and unmistakable disclaimer.

Netlist also seeks support in the extrinsic evidence, arguing that compliance with JEDEC standards requires importing its desired limitation. However, the Board receives deference to its findings that the JEDEC standards permit single-device ranks. Netlist fails to challenge those findings, which immediately bars its argument on appeal. In any event, claim 16 does not require compliance with JEDEC standards and the '912 patent as a whole teaches embodiments outside those standards.

The Board's analysis properly applied this Court's approach to claim construction and should be affirmed.

Turning to Netlist's challenges to the Board's factual findings, Ellsberry's express disclosures provide substantial evidence supporting the finding that Ellsberry teaches an embodiment with a memory module having single-device ranks satisfying the proper construction of claim 16. Rather than addressing the express disclosure of Ellsberry's Figure 12, Netlist offers its own complicated interpretation that requires merging different figures together in a particular way to require multi-device ranks. But that is not a reasonable reading of Ellsberry, and, in any event,

would not meet the standard of review for the relief Netlist seeks. Netlist also argues about statements regarding Ellsberry in previous IPRs. However, the language Netlist highlights concerns different embodiments and is simply irrelevant to the appealed finding.

Netlist also seeks to reweigh the evidence showing a lack of written description for claim 16 in the '244 provisional application and in the application that resulted in the earlier '436 patent. For the '436 patent, the Board was not required to adopt Netlist's position that a POSITA would infer an unidentified "*register*" when the '436 patent does not disclose it. Netlist also failed to meet its burden of production with respect to showing written description for each and every limitation of claim 16, which it cannot remedy on appeal.

For the '244 provisional, the Board had substantial evidence to find inadequate written description support for the unmentioned "*bank address signals*." Netlist again seeks to import disclosure, this time from JEDEC standards for particular DDR devices, but the Board could reasonably reject that approach. No language in the '244 provisional mentions DDR devices or JEDEC. Netlist's argument that undisclosed "industry standards" must be combined with its provisional application is both legally wrong and factually inadequate. The Board should be affirmed.

ARGUMENT

I. Standard of Review

This Court reviews legal conclusions de novo and factual findings for substantial evidence. *Almirall, LLC v. Amneal Pharms. LLC*, 28 F.4th 265, 271-72 (Fed. Cir. 2022). Substantial evidence means "such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000) (quoting *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229-30 (1938)). "[T]he possibility of drawing two inconsistent conclusions from the evidence does not prevent an administrative agency's finding from being supported by substantial evidence." *Consolo v. Fed. Mar. Comm'n*, 383 U.S. 607, 620 (1966).

"Whether a claimed invention is unpatentable as obvious under § 103 is a question of law based on underlying findings of fact." *In re Gartside*, 203 F.3d at 1316. Those underlying facts include the "scope and content of the prior art, differences between the prior art and the claims at issue, the level of ordinary skill in the pertinent art, and any objective indicia of non-obviousness." *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007); *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)). A finding as to the scope and content of the prior art is reviewed for substantial evidence, which considers whether "the Board reasonably found that a skilled artisan

would have understood that [disclosure]." *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1340 (Fed. Cir. 2020).

For claim construction, this Court "review[s] the Board's constructions based on intrinsic evidence de novo and its factual findings based on extrinsic evidence for substantial evidence." *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1376 (Fed. Cir. 2019) (quoting *HTC Corp. v. Cellular Commc'ns Equip., LLC*, 877 F.3d 1361, 1367 (Fed. Cir. 2017)).

For determinations of whether an earlier priority application provides written description for a claim, "[s]ufficiency of written description is a question of fact, reviewed for substantial evidence." *Parus Holdings, Inc. v. Google LLC*, 70 F.4th 1365, 1373 (Fed. Cir. 2023) (quoting *Gen. Hosp. Corp. v. Sienna Biopharms., Inc.*, 888 F.3d 1368, 1371 (Fed. Cir. 2018)).

II. The Board correctly recognized that a "*rank*" may have only one memory device

Following well-established claim construction law under *Phillips*, the Board "determine[d] that the intrinsic evidence of the '912 patent shows that the claim term 'rank' may include only one memory device." Appx13-14. The Board's conclusion adheres to the plain claim language, preserves embodiments in the specification practicing claim 16, and is consistent with the prosecution history as discussed below in detail.

The first sign that something is amiss with Netlist's claim-construction arguments is that they are upside down. Netlist elsewhere concedes (Br.60) that "the specification"—the claims plus the written description—is "the single best guide to the meaning of a disputed term" and "[u]sually . . . dispositive." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). Yet Netlist leads (Br.33-34, 36-38, 41-45) with a lengthy disclaimer argument based on the "prosecution history," which "often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1317. Only as an afterthought does Netlist briefly make a few arguments aimed at the "claim language" (Br.38-40, 46-47) and the "specification" (Br.40-41, 48-50).

Moreover, Netlist's bluster about the prosecution history is misplaced—there was no construction of "*rank*" during reexamination. The statements that Netlist cites merely found that Amidi's ranks included a plurality of memory devices. *See* Appx493-94 (citing Appx6374-76, Appx6413). As the Board correctly put it, referring to the case "***when*** there is a plurality of memory devices in a rank" is not a claim construction—it is a reference to the specific teachings of Amidi. Appx493-94.

A. The claim language itself shows that a "*rank*" may include only a single memory device

"Claim construction begins with the words of the claim, which 'must be read in view of the specification, of which they are a part.'" *Wi-LAN, Inc. v. Apple Inc.*,

811 F.3d 455, 462 (Fed. Cir. 2016) (quoting *Phillips*, 415 F.3d at 1315). The Board correctly recognized that the claims indicate that a "*rank*" may include just a single device. Appx14-15.

Claim 16 recites a memory module comprising "*a plurality of double-data-rate (DDR) memory devices … having a first number of DDR memory devices arranged in a first number of ranks*." Appx103 (3:13-16). The claimed memory module also includes a "*logic element … receiving a set of input signals … to control a second number of DDR memory devices arranged in a second number of ranks*." *Id*. (3:18-24). The only restriction on these "*number[s]*" is that the "*second number*" of devices and ranks must each be less than the corresponding "*first number*" of devices and ranks. *Id.* (3:25-28). Thus, the "*second number*" can be one, Appx214-15, as expressly claimed elsewhere in the '912 patent, Appx98 (Claim 35, "*wherein the first number of ranks is two and the second number of ranks is one*").

Claim 16 distinguishes between "*a plurality of*" on one hand and "*a first number of*" or "*a second number of*" on the other. The Board's construction is consistent with a claim "in which care is taken to use 'a plurality of' when more than the singular is meant." *Sound View Innovations, LLC v. Hulu, LLC*, 33 F.4th 1326, 1333 (Fed. Cir. 2022). Accordingly, the language of claim 16, which does not use "*plurality of*" to describe the number of devices in a rank, "does not preclude the possibility that a rank could have a single memory device." Appx14-15.

Claim 16 also stands in contrast to claim 55, which expressly states that "***each rank*** of the first number of ranks comprises ***a plurality of the DDR DRAM*** chip packages." Appx104 (5:56-58). The Board properly refused to erase that difference in language. Appx15. When certain claims "contain additional limitations that limit those claims" and contrast with claims lacking those limitations, a proper construction aligns with that difference in scope. *Callicrate v. Wadsworth Mfg., Inc.*, 427 F.3d 1361, 1371-72 (Fed. Cir. 2005) (comparing claims to reject limit on "preformed endless loop" as requiring a mechanical connection device).

Focusing solely on claim differentiation, Netlist wrongly suggests that claim 55 can be disregarded because other differences exist between claim 55 and claim 16. Br.46 (citing *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004)). But claim differentiation is not the only way in which other claims can inform the meaning of a term. As explained in *Phillips*, "the usage of a term [("rank")] in one claim [(claim 55)] can often illuminate the meaning of ***the same term in other claims*** [(claim 16)]." 415 F.3d at 1314. Nor do similarities between claim 1 and claim 55 suggest that claim 55's reference to a plurality of chip packages is just "repeating requirements claim 1 imposes already." *Contra* Br.47. Such an interpretation would render "*plurality*" in claim 55 superfluous, which is "highly disfavored." *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021)

(quoting *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017)).

Netlist points to a JEDEC standard for DDR to support its construction, but Netlist is incorrect that "the claims reference JEDEC's 'DDR' standard." Br.39-40, 46. The term "*DDR*" in claim 16 is just an abbreviation for "*double-data-rate (DDR) memory devices*," Appx103 (3:13), which includes DDR devices beyond those in the particular JEDEC standard cited by Netlist, *see, e.g.*, Appx20427-36 (DDR SGRAM); Appx20838-61 (DDR SRAM). And the "JESD79D" JEDEC standard cited by Netlist, which the patent "incorporates by reference," Br.40 (citing Appx86 (12:40-41), does not even use the term "rank" and instead uses the older term "bank," consistent with the definition in the Jacob textbook that a "a *rank* of memory is a '*bank*' of ***one or more*** DRAM devices," *see supra* pp.7-9 (citing Appx11702; Appx20270 ("Chip Select . . . provides for external ***bank*** selection")). Netlist's own expert refused to limit claim 16 to any particular JEDEC standard. Appx20191-92 (224:12-225:17). Accordingly, the Board reasonably determined that "claim 16 [does not] recite that the memory module is compliant with a JEDEC standard." Appx51. In any event, as discussed below, the JEDEC standards permitted single-device ranks with DDR memory. *See infra* pp.41-44.

The Board's construction of "*rank*" is also confirmed by the usage of "*rank*" in related U.S. Patent No. 9,858,215. The '215 patent is in the same family as the

'912 patent, with both patents descended from U.S. Patent No. 7,289,386 filed July 1, 2005. Appx60, Appx15352. The term "*rank*" as used in claim 1 of the related '215 patent expressly encompasses ranks having only one memory device: "the plurality of memory integrated circuits including ***at least one*** first memory integrated circuit ***in the first rank*** and ***at least one*** second memory integrated circuit ***in the second rank***." Appx15403 (37:32-38). This claim language in the related '215 patent is contrary to Netlist's assertion that a "*rank*" always requires ***two*** or more memory devices. As this Court has held, "we presume, unless otherwise compelled, that the same claim term in the same patent or related patents carries the same construed meaning." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003). Only the Board's construction of "one or more" is consistent with the varying uses of "*rank*" in Netlist's patents.

B. The specification confirms that a "*rank*" includes embodiments with only a single memory device

The Board correctly determined that the "specification of the '912 patent similarly describes its memory module without restriction on the specific number of memory devices that can be included in each rank." Appx15 (citing Appx82-84 (3:3-14, 6:64-7:18)). For example, the Board "f[ou]nd no statement … in the '912 patent that a rank must include multiple memory devices, and cannot include a single memory device." Appx18. The specification discloses that memory devices "of a memory module are generally arranged as ranks or rows of memory, each rank of

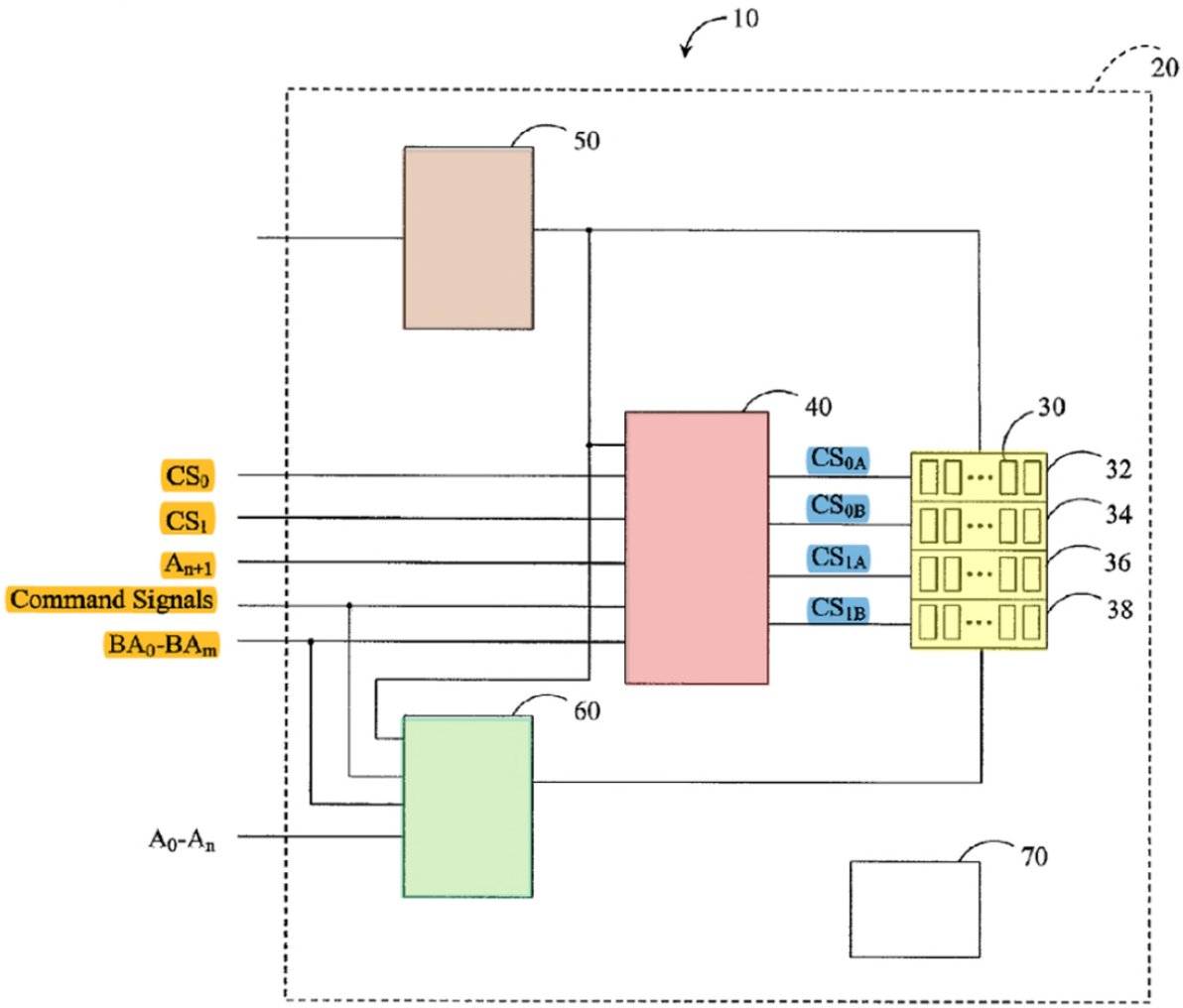
memory generally having a bit width," "the ranks of a memory module are selected or activated by … rank-select signals, also called chip-select signals," and "[m]ost … systems support one-rank and two-rank memory modules." Appx81 (2:16-18, 2:35-40). But the specification never requires multiple memory devices in a rank.

On the contrary, the specification teaches that single-device ranks are permissible, by disclosing that the width of a single memory device can be the ***same*** as the width of the memory module (e.g., 32 bits). Appx83 (5:60-64, 6:16-19). Netlist never proposed a construction excluding any particular bit-widths from the scope of claim 16, *see*, *e.g.*, Appx20194-96 (227:19-229:20), and the Board concluded that "claim 16 does not require any particular bit width," Appx51. The 32-bit example from the specification of a single-device rank satisfies Netlist's argument that "the bit-width of the memory ***chips*** in a rank must ***add up*** to the bit-width of the ***memory module***." Br.39; *see also* Appx13075 ¶ 74 ("'rank' . . . read[s] or write[s] the full bit-width of the memory module"). And Petitioner introduced evidence that such an example of a single-device rank was commercially available with DDR memory. Appx21151 (annotating Appx20427, Appx20433).

On appeal, Netlist argues that Figure 1A, annotated below, includes multiple memory devices (30, yellow) per rank (e.g., 32). Br.48-49 (pointing to Figure 1A); *see also* Br.40-41 (pointing to examples of 64-bit and 72-bit memory modules). But the Board correctly recognized that such figures are described as "exemplary," rather

than limiting. Appx18. And the Board's conclusion that a "*rank*" can include one ***or more*** memory devices is consistent with examples like Figure 1A below showing the "or more" part of the claim construction where there is more than one memory device (30) per rank (e.g., 32).

Figure 1A:



Appx136 (annotating Appx63); Appx84 (7:35-54).

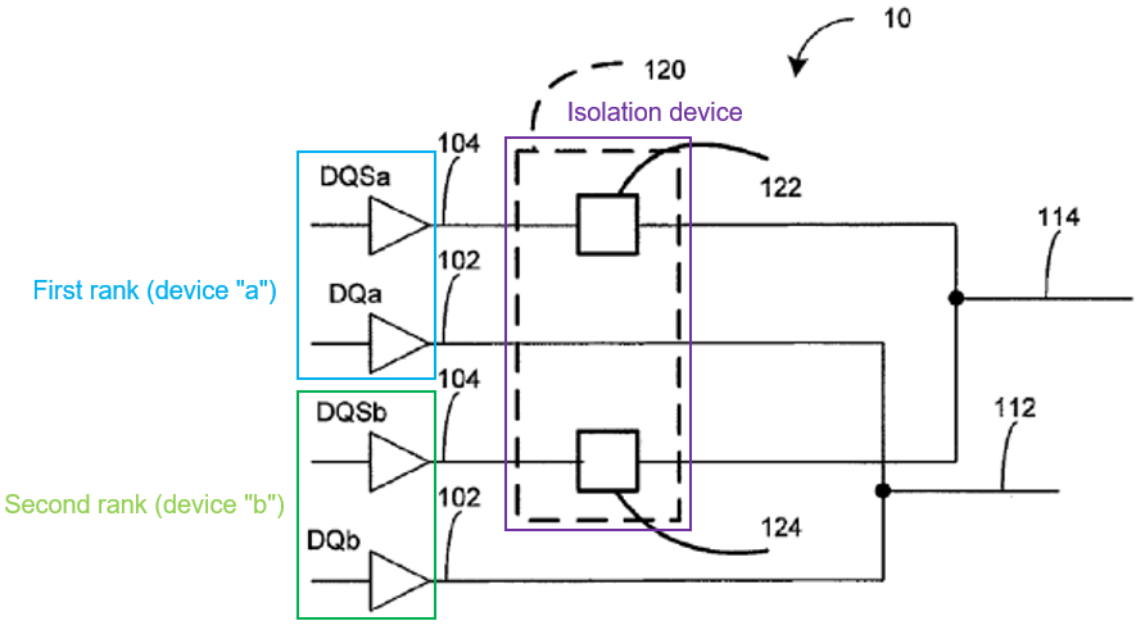
But the '912 patent also discloses single-device ranks, as recognized by the Board. Appx18-19, 23. For example, the Board analyzed in detail the '912 patent's

Table 1 and the corresponding description in the specification. Appx15-18 (analyzing Appx84-85 (7:55-9:21)). There, the specification states that "[i]n certain embodiments, the command signal is passed through ***to the selected rank only*** … [and i]n such embodiments, the command signal (e.g. read) is sent to ***only one memory device*** or the other memory device so that data is supplied from one memory device at a time." Appx84 (8:48-60). In this example, when the command signal is sent to only one rank, it is sent to only one memory device—an example of a single-device rank. The '912 patent further explains that, when "the command signal is passed through ***to both*** associated ***ranks*** …, the command signal (e.g., refresh) is sent ***to both memory devices***," *id*., making clear that the two memories are arranged in two ranks, meaning "each rank must have only one memory device," Appx18. Accordingly, the Board's conclusion that "this passage means that a rank may have only one memory device" is fully supported by the '912 patent. Appx18.

On appeal, Netlist argues that "Table 1 refers to the embodiment in Figure 1A," which has multiple memories in a rank. Br.48-49. But the statements the Board relied on, discussed directly above, concern various "embodiments" without any reference to Figure 1A. Appx84 (8:47-60) ("In certain embodiments"; "In such embodiments"); Appx18.

The Board also carried out a detailed analysis of the "Back-Back Adjacent Read Commands" (BBARX) section of the '912 patent and determined that it also

discloses a single-device rank. Appx18-23 (citing Appx92-93 (23:26-25:67)). This section teaches that "[t]he isolation device 120 of certain embodiments multiplexes the DQS data strobe signal lines 104 of the two ranks of memory devices 30 from one another to avoid a BBARX collision." Appx92 (24:35-38). This is shown below in Figure 6B, which the Board concluded shows "memory devices 'a' and 'b' of different ranks," Appx18-19, with no suggestion that either rank contains other undisclosed memory devices:



Appx70 (annotations added); *see* Appx92 (24:39-58). "This section thus supports that a rank may have only one memory device." Appx19.

Netlist does not dispute that "Figure 6B depicts … memory devices 'a' and 'b' of different ranks," but argues that the figure is "simplified" and is only "zooming-in on a pair of memory devices in two respective ranks." Br.48, 49-50

(citing Appx92 (24:31-34)). However, the '912 patent states that "FIG. 6B schematically illustrates … an exemplary ***memory module*** 10" without referring to any "zooming-in" or simplification. Appx92 (24:28-31).

The embodiments discussed above with single-device ranks are the only disclosed embodiments that satisfy claim 16, which requires that "the ***command*** signal is transmitted to ***only one*** DDR memory device at a time." Appx103 (3:42-43). Netlist's proposed construction improperly excludes the only disclosed embodiments for claim 16, which "is rarely, if ever correct and would require highly persuasive evidentiary support." *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022) (quoting *Epos Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1347 (Fed. Cir. 2014)).

Netlist's arguments to the contrary are misplaced. Netlist points to "Example 2" of the Verilog code in the '912 patent (Appx87 (14:5-16), Appx89-90), *see* Br.50, and cites to extrinsic evidence consisting of attorney argument (Appx1563 (71:5-17)) and its expert's testimony that a rank with multiple memory devices, such as the example in Figure 1A, could practice claim 16 because "Example 2 [of the Verilog code] teaches how to transmit a ***command*** to a single memory device on a physical rank of multiple memory devices," Appx18298 ¶ 40. But that Verilog code concerns "logic to reduce potential problems due to … 'BBARX,'" Appx87 (14:11-14), which as discussed above and shown in Figure 6B concerns "the DQS ***data***

strobe signal lines 104," Appx92 (24:35-58), not any ***command*** signal, *see* Appx19-21; *see also* Appx21158 (Petitioner's slide 27); Appx1548-59 (56:5-57:26) (discussing Appx21341 (Netlist's slide 100 quoting Appx18297-98 ¶ 40)). Thus, the Board reasonably concluded that "[f]rom inspection of Figure 6B and the code of Example 2, we agree with Petitioner that the code of Example 2 relates to enabling and disabling a FET 122 on the DQS data strobe line, not the command line discussed in the 'Logic Tables' section of the '912 patent." Appx21. The Board specifically disagreed with the testimony of Netlist's expert on this issue. *See* Appx21-23 ("[W]e find the Verilog code in the '912 patent supports Petitioner's position that a rank may be only one device.").

Netlist also wrongly suggests that the '912 patent's alleged goal of increasing memory capacity requires that a "*rank*" includes multiple devices. Br.41. But the Court's "task is not to limit claim language to exclude particular devices because they do not serve a perceived 'purpose' of the invention." *Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1345 (Fed. Cir. 2008). Moreover, the patent explains that capacity can be increased ***either*** by "increasing the number of memory devices per rank ***or*** by increasing the number of ranks," Appx81 (2:24-28), meaning Netlist's alleged purpose could be satisfied regardless of whether a "*rank*" has one device or more.

C. Netlist misinterprets the reexamination history

Netlist argues that the prosecution history trumps the express claim language and disclosures of single-device ranks in the specification discussed above. Br.33-34, 36-38, 41-45. Notably, Netlist's arguments to this Court about the reexamination rely on disclaimer—a doctrine invoked to "***depart*** from the [claim language's] plain meaning." *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016). Netlist's disclaimer arguments thus tacitly concede that the plain meaning of the claim language encompasses single-device ranks.

Moreover, Netlist fails to acknowledge its considerable burden to "demonstrate[e] the existence of a 'clear and unmistakable' disclaimer" of single-device ranks. *Mass. Inst. of Tech. v. Shire Pharms., Inc.*, 839 F.3d 1111, 1122 (Fed. Cir. 2016). Where, as here, "the prosecution history is used solely to support a conclusion of patentee disclaimer, the standard for justifying the conclusion is a high one." *Maquet Cardiovascular LLC v. Abiomed Inc.*, 131 F.4th 1330, 1339 (Fed. Cir. 2025) (quoting *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016)). If "the alleged disavowal is ambiguous, or even amenable to multiple reasonable interpretations," this Court "decline[s] to find prosecution disclaimer." *Id.*

Netlist cannot meet its burden for disclaimer because the Board correctly rejected the fundamental premise in Netlist's argument: that "*rank*" was construed

during reexamination. *See* Appx305-11, Appx960-61 (Netlist's argument); Appx493-94, Appx23 (Board's rejection of Netlist's argument). Netlist asserts that "[t]he Board never explained why the Patent Office's own view of the claim during the reexamination—when claim 16 issued—would not be determinative to any reader of the intrinsic record." Br.34; *see also* Br.21, 43-45 (similar). But the Board did explain its reasoning: the Board determined that the reexamination statements, quoted below, referred to Amidi's teaching of a multi-device rank, which "is not the same as stating that claim 16 requires a plurality of memory devices in a rank." Appx493-94.

Netlist's entire argument rests on conflating two distinct statements during reexamination, the first about what claim 16 requires and the second about what Amidi discloses:

> The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank.*

Appx10561 (emphasis from Board); *cf.* Br.37, 44. The reexamination Board conspicuously did ***not*** say that claim 16 requires "a plurality of memory devices in a rank." The Board said only that claim 16 requires sending a signal "to only ***one*** DDR memory device at a time." The Board then noted how the cited Amidi reference was different: Amidi teaches sending the command signal to ***multiple***

memory devices in the same rank. Indeed, immediately after the above statement, the reexamination Board clarified that it was referring to Amidi's disclosure: "That is, ***Figures 6A and 6B of Amidi*** show various command signals . . . being transmitted to more than one memory device." Appx10561; *see also* Appx6413 (Examiner citing Figure 6 of Amidi, Appx11874-75).

Netlist asserts that "Requester 2" in the reexamination "argued that Amidi taught sending a signal to only one memory device at a time by teaching a 'rank' that purportedly 'encompasses' just '"***one memory device***."'" Br.16 (citing Appx6951-52); *see also* Br.36-37 (citing Appx6910-12). But the Examiner found those arguments "**defective**, because they propose new rejections," so they were neither considered by the Examiner nor adopted by the Board. Appx7211. Netlist also asserts that during the reexamination "the Board did not deny the possibility that a rank in Amidi could include only one memory device." Br.37. To the contrary, the Board found that "Figures 6A and 6B of Amidi show various command signals . . . being transmitted ***to more than one memory device***." Appx10561. This was a factual finding about Amidi, not a claim construction determination or a disclaimer of claim scope. Appx493-94.

D. JEDEC standards do not require a different construction of "*rank*"

Because the claims and specification make clear that a rank can include only one device, the Board reasonably concluded "we need not resort to extrinsic evidence." Appx23-24.

Nonetheless, extrinsic evidence in this case—including JEDEC standards—supports the Board's conclusion that a "*rank*" may include just one device. The Jacob textbook, for example, defines the term "rank" as "one or more DRAM devices that operate in lockstep in response to a given command." Appx11702. The textbook expressly states that there may be "as few as one device per rank," Appx11703, directly contrary to Netlist's assertion that "[a] 'rank' of one item—*e.g.*, one DRAM chip—makes no sense in JEDEC's usage or the term's origins." Br.40.

Consistent with this textbook description of "ranks," the JEDEC standards contemplate examples of ranks having a single device. For example, the below excerpts from JEDEC Standard No. 21-C also show a 32-bit DDR memory device with a 32-bit-wide module, which means the rank must have only one device (as confirmed by the second figure showing only one memory device receiving the chip-select (CS) signal):

4.5.9 – 144 PIN DDR SGRAM SO–DIMM FAMILY

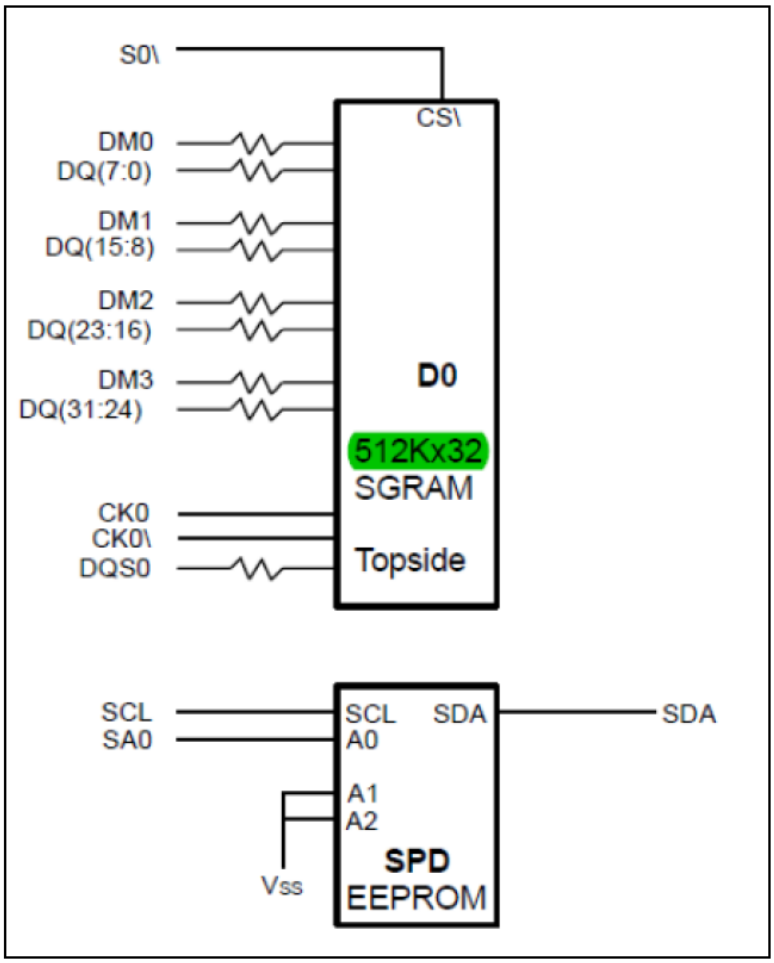
GENERAL FEATURES

- 144-pin small outline dual in line memory module (SO-DIMM)
- 64-bit data bus with no ECC and no parity
- Module capacity ranges from 1 MB to 8 MB
- Supports 8 Mb and 16 Mb double data rate (DDR) SGRAMs
- Dual supply 3.3 V and 2.5 V
- 2.5 V DDR I/O Class B on single data rate (SDR) signals
- 2.5 V DDR I/O Class A on double data rate signals
- Similar to existing SDR SO-DIMM

CAPACITY—Module capacity ranges from 1 MB to 8 MB

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT without PARITY
—64 BIT without PARITY

CONFIGURATION—4 Different Configurations are defined using X32 SGRAM memories in 1 and 2 bank configurations.



Appx21151 (annotating Appx20427, Appx20433).

The ’912 specification further discloses that “[m]emory modules typically include a serial-presence detect (SPD) device … comprising data which characterize various attributes of the memory module, including but not limited to, … the data width of the memory devices, the number of ranks, … the number of memory devices.” Appx85 (9:22-37). A POSITA, who was undisputedly familiar with the JEDEC standards, understood from this disclosure that there were JEDEC standards for the SPD, *see, e.g.*, Appx20382, which the Board found “permitted 8-bit and 16-bit modules” with a single 8-bit or 16-bit memory device per rank. Appx51 (citing, e.g., Appx20116 (149:10-18), Appx20118-20 (151:3-153:22); Appx20388 (“Rank: any DRAMs connected to same physical CS”); Appx20389 (Byte 6); Appx20394 (Byte 13)); *see also* Appx21160. It is undisputed that DRAM devices could be 8 bits or 16 bits wide. Br.7 (“Individual ***DRAM chips*** also must read/write a set of bits in parallel—4, 8, or 16 bits at a time under the JEDEC DDR standard.”). Thus, the Board correctly found that a POSITA understood that the SPD disclosed in the ’912 patent and in the corresponding JEDEC standards allowed an 8-bit-wide memory module with 8-bit-wide memory devices, resulting in single-device ranks. Appx51. Netlist does not even address this finding about JEDEC, much less refute it. *See* Br.39-40.

In view of the above, Netlist is incorrect that “JEDEC standards preclude memory modules with one DRAM chip per rank” and only permit “memory-module

bit-widths of 64 or 72 bits." Br.39 (emphasis omitted). As reflected both in the SPD standard and in Standard No. 21-C, JEDEC is not limited to any specific width for the module or any specific number of memory devices per rank. Netlist's attempts to rely on JEDEC for a narrower construction of "*rank*" thus fail.

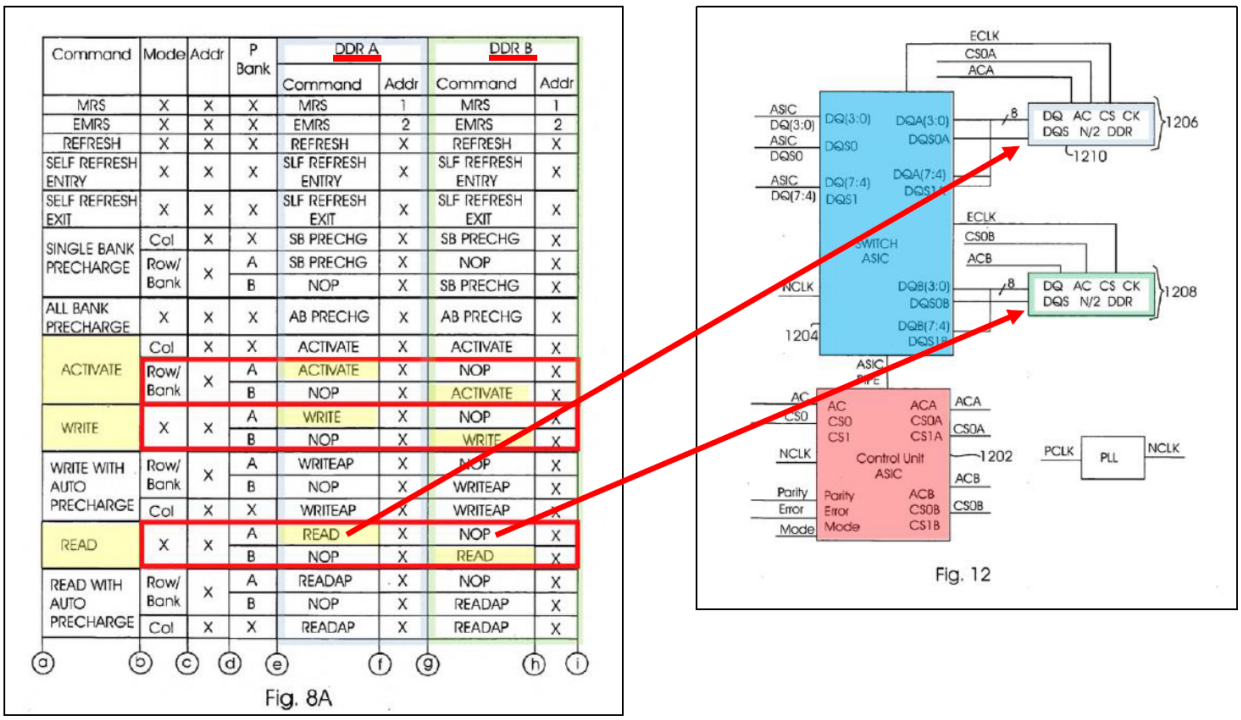
III. Substantial evidence supports the Board's determination that Ellsberry discloses all limitations of claim 16

The Board properly concluded that Ellsberry discloses every limitation of claim 16. Appx37-51. Netlist only disputes the sufficiency of the Board's analysis for limitation [16.e], *see* Appx45-51, because, according to Netlist, "Figure 12 [of Ellsberry] does not show a rank with only one memory device (chip); it shows a 'data group' that contains only ***part*** of a rank." Br.50-51. Netlist's arguments regarding limitation [16.e] fail because Ellsberry's Figure 12 embodiment discloses a complete memory module with single-device ranks. The Board's finding that Ellsberry discloses single-device ranks is not in tension with the Board's analysis of Ellsberry in prior IPRs, which addressed a different embodiment from Ellsberry with multi-device ranks.

A. Figure 12 of Ellsberry discloses a single-device rank

Ellsberry directly states that the memory module shown in Figure 12 has one memory device per rank: "FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202 and one bank switch 1204 are used to

control two memory [r]anks[4] 1206 & 1208, ***each memory [r]ank having one memory device*** 1210." Appx11908 ¶ [0055]; *see also* Appx11908 ¶ [0052]. As shown in Figure 8A (Appx11896)—and consistent with limitation [16.e]—the Read or Write command signal is transmitted to ***only one*** DDR memory device at a time:



Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

Fig. 8A

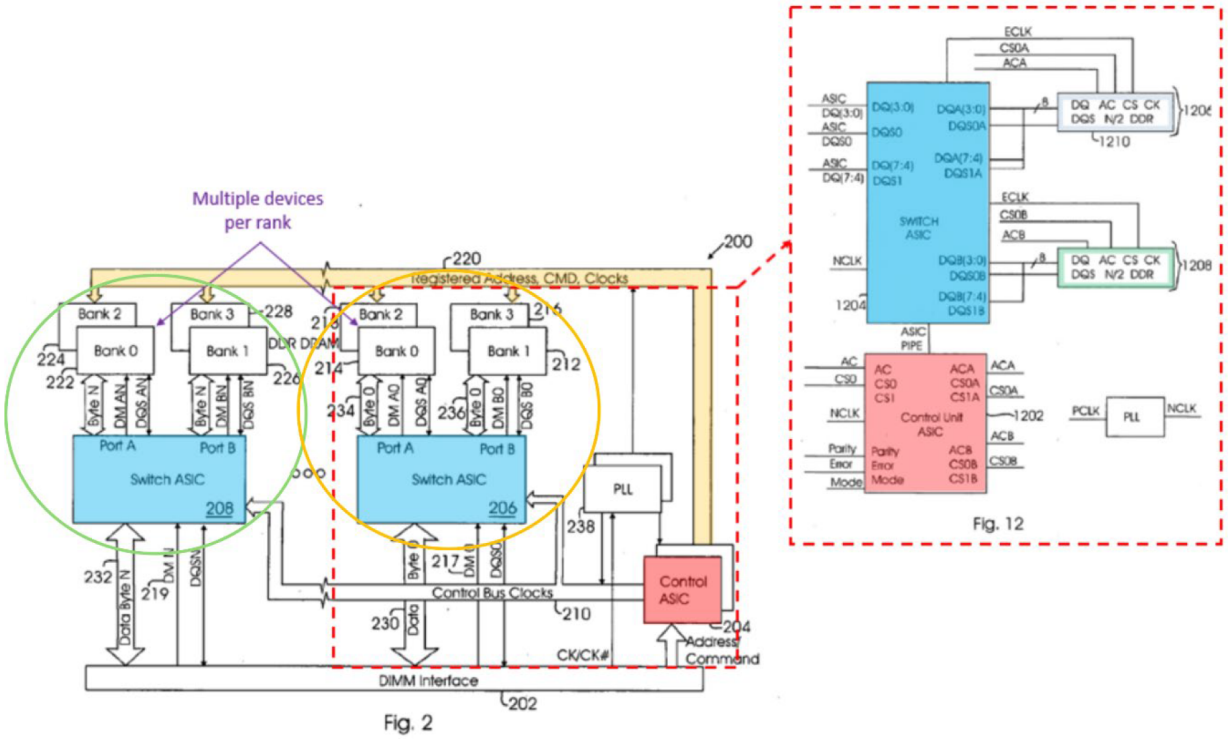
Fig. 12

Appx21206 (annotating Appx11896, Appx11901); Appx50.

Despite Ellsberry expressly stating that Figures 10-13 "illustrate different configurations of ***memory modules***" (Appx11908 ¶ 52), Netlist argues that Figure 12 is merely ***part*** of the larger memory module shown in Figure 2 (below left), which has two separate bank switches (or "Switch ASIC[s]," blue) with each

[4] As explained above, Ellsberry used the older term "bank" to refer to what is now called a "rank." *See supra* pp.7-9.

bank switch connected to one "data group" that has one memory device from each rank:



Br.51-52 (citing Appx11905-06 ¶¶ [0030, 0035]). By merging Figures 2 and 12 together this way, Netlist asserts that the memory devices in Figure 12 are part of larger multi-device ranks. *Id.* But Netlist is again directly contradicting Ellsberry's express disclosure that, in Figure 12, "each memory [r]ank ha[s] one memory device." Appx11908 ¶ [0055].

The Board correctly rejected Netlist's argument about Figure 12 because Ellsberry is not limited to the configuration shown in Figure 2 (with two bank switches and two "data groups" resulting in each rank having two memory devices). Appx49-50. Ellsberry expressly states that its invention may use "***one*** or more

memory bank switches 206 & 208" from Figure 2, consistent with the embodiment of Figure 12 showing ***one*** memory bank switch with ***one*** data group with ***one*** memory device per rank. Appx50 (quoting Appx11905 ¶ [0028]); *see also* Appx11908 (claim 6) (claiming a "memory module comprising: … ***one*** or more memory bank switches"), Appx11884 (Abstract, "A control unit and memory bank switch are mounted on a memory module …"). The Board had substantial evidence to find that Figures 10-13 disclose complete memory modules, independent from the embodiment shown in Figure 2. Appx50. Having concluded that Figure 12 can operate as a complete module, the Board recognized that "Ellsberry discloses transmitting a command (Activate, Write or Read) to only the selected one of the two memory devices in Figure 12[.]" *Id.* Ellsberry thus satisfies limitation [16.e].

Netlist's arguments about "Ellsberry's purpose" of expanding the capacity of the memory module and about JEDEC compatibility do not undermine Ellsberry's express disclosure. Br.52-53. Ellsberry expressly teaches that Figure 12 illustrates a combination of a "control unit and bank switch" according to an embodiment of the "invention," Appx11908 ¶ [0052], which is "expanding the memory capacity of a memory module," Appx11903 ¶ [0010]. Indeed, Figure 12 has ***two*** ranks instead of ***one*** rank that can be controlled in a "single chip-select memory configuration." Appx11908 ¶ [0055]. Therefore, Figure 12 of Ellsberry is like the '912 patent, where the "memory capacity of a memory module increases . . . by increasing the

number of ranks." Appx81 (2:23-27). Netlist's proposal of having more devices in each rank does not undermine that Figure 12 also increases the capacity of the module by increasing the number of ranks. Furthermore, Netlist's proposal increases the width of the bus which "is often undesirable and impractical." Appx11903 ¶ [0005]. As for JEDEC compatibility, *see* Br.53, the Board correctly concluded that it is not required by claim 16 and, in any event, is satisfied since "JEDEC standards permitted 8-bit . . . wide modules," like the one shown in Figure 12 of Ellsberry. Appx51 (citing Appx20388-89, Appx20394; Appx20352-53, Appx20358; Appx20108 (141:11-19), Appx20111-14 (144:10-147:25), Appx20116 (149:10-18), Appx20118-20 (151:3-153:22)).

Furthermore, Netlist's citation to *Medtronic, Inc. v. Teleflex Innovations, S.à.r.l.* is misplaced. Br.53 (citing 69 F.4th 1341, 1349 (Fed. Cir. 2023)). *Medtronic* dealt with "modifications" to a prior art reference, and it does not suggest that expressly disclosed embodiments can be ignored. *See* 69 F.4th at 1347-49.

Lastly, the standard of review is particularly salient for this dispute. Even if Ellsberry ***could*** be interpreted as Netlist suggests, that does not mean the Board lacked substantial evidence for its interpretation of Ellsberry. *See Incept LLC v. Palette Life Scis., Inc.*, 77 F.4th 1366, 1373 (Fed. Cir. 2023) (quoting *Consolo*, 383 U.S. at 620). Ellsberry's statements about Figure 12 and the use of "one or more" switches, discussed above, constitute substantial evidence supporting the Board's

factual finding. Appx50. The testimony of Petitioner's expert, Dr. Wolfe, cited by the Board, *id.*, provides additional substantial evidence supporting the Board's conclusion. Appx13225-28 ¶ 264 (explaining that in Figure 12 of Ellsberry a command signal is sent to only one memory device at a time); *see also* Appx13181-83 ¶¶ 215-17 (explaining that Figure 12 of Ellsberry discloses a module having "two x8 DDR memory devices arranged in two ranks," each with its own respective chip select signal CS0A and CS0B, and having the same bit width as the module). Tellingly, Netlist repeatedly cites the declaration of its own expert to support its alternative interpretation of Ellsberry. Br.52 (citing Appx18450-51). But the Board already considered that testimony, Appx45-47, and explained in detail the reasons for its finding to the contrary, Appx49-51. "That the Board gave more credit to one expert witness than another is not grounds for reversal." *Parus*, 70 F.4th at 1374.

B. Prior IPRs involving Ellsberry's *other* embodiments are irrelevant

Netlist argues that the Board's analysis of Ellsberry "contradicts" previous IPRs finding that Ellsberry discloses "***multiple*** . . . Data Group[s]" and thus multi-device ranks. Br. 53-54. But there is no contradiction, because neither Petitioner nor the Board has suggested that Ellsberry ***only*** discloses embodiments with single-device ranks. To the contrary, Ellsberry discloses some embodiments with single-device ranks (such as Figure 12 as found in this IPR), and other embodiments with multi-device ranks (such as Figure 2 as found in previous IPRs). In the previous

IPRs, the Board compared features of Ellsberry's Figure 2 to a different patent that expressly required "a plurality of memory devices" in a rank. Appx11928-30. In those previous IPRs, the Board also relied on Figure 2 ***in combination with*** Figures 11 and 13 for certain dependent claims. Br.54; Appx11958-59, Appx11965-66, Appx11986-87. It is unremarkable that the Board considered different embodiments from Ellsberry in different IPRs. There is no inconsistency with the Board relying on Figure 2 in prior IPRs (alone or in combination with Figures 11 and 13) and relying on Figure 12 alone in the present IPR. As found by the Board here, "Figures 10–13 are memory modules notwithstanding that they could also be used as parts of a larger memory module according to Figure 2's configuration." Appx50.

IV. Ellsberry is prior art to claim 16

The Board correctly found that Ellsberry is prior art because the '436 patent and '244 provisional do not provide written description support for claim 16. Appx26, Appx29-30, Appx31-34. Substantial evidence supports the Board's findings because the '436 patent fails to disclose a "*circuit comprising a logic element and a register*" (among other limitations), and the '244 provisional fails to disclose "*bank address signals*" (among other limitations), in stark contrast to the express disclosures for those limitations in the '912 patent. *Id.*

Netlist does not and cannot argue that the '436 patent and '244 provisional directly describe each and every limitation of claim 16. Instead—just like it did

before the Board—Netlist resorts to the flawed argument that alleged knowledge of a POSITA can fill in the missing support for claim 16. *See, e.g.*, Br.56-57 (arguing that a POSITA would understand "sequential logic" may include the claimed "register"); Br.63-65 (arguing that a POSITA would understand "control signals" may include the claimed "bank address signals"). But "a description that merely renders the invention obvious does not satisfy the [written description] requirement." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc); *see also Impact Engine, Inc. v. Google LLC*, No. 22-2291, 2024 WL 3287126, at *10 (Fed. Cir. July 3, 2024) (nonprecedential) (rejecting argument that knowledge of a POSITA could supplement "black-box" disclosure of a compiler for written description), *cert. denied*, No. 24-836, 2025 WL 663721 (U.S. Mar. 3, 2025).

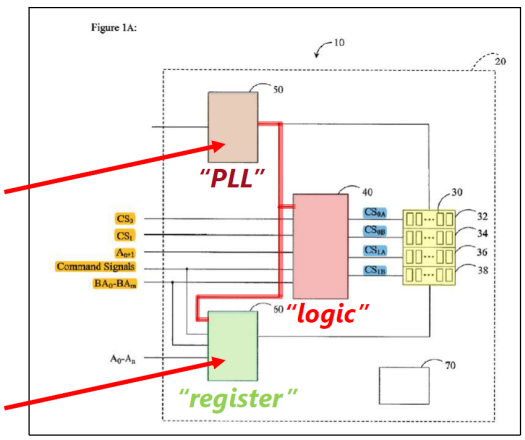
A. Claim 16 is not supported by the '436 patent

Netlist's arguments about the '436 patent should be rejected for three independent reasons. First, whether the "sequential logic" that Netlist relies on in the '436 patent discloses the claimed "*register*" is a factual dispute, which the Board properly resolved in Petitioner's favor. Second, Netlist cannot rely on the knowledge of a POSITA to supply the written description support for the "*register*." Third, Netlist did not even attempt to show that every limitation of claim 16 is supported by the '436 patent. Any one of these three points is sufficient to uphold the Board's finding that the '436 patent does not support claim 16.

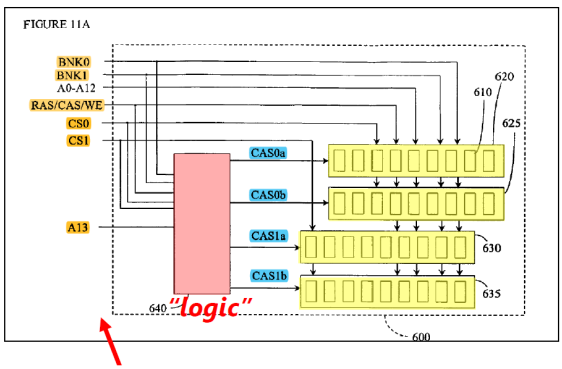
1. Substantial evidence supports the Board's conclusion that the '436 patent does not disclose a circuit with both a "*register*" and a "*logic element*"

The Board correctly recognized that the '436 patent does not disclose a circuit that has both a "*register*" and a "*logic element*" as required by claim 16. Appx30-32. The Board found, and Netlist does not dispute, that the '436 patent (shown below right) contains "no mention" of a register, Appx31, in clear contrast to the '912 patent (shown below left) which expressly discloses a register (60, green), a logic element (40, red), and a phase-lock loop (PLL) (50, brown), Appx7-8, Appx26:

The '912 Patent [EX1001]



The '436 Patent [EX1009]



Appx21219 (annotating Appx63, Appx2494). The deficiency in the earlier '436 patent is not limited to Figure 11A, shown above on the right—no embodiment in the '436 patent contains a "*logic element*" and a "*register*," much less a register coupled to a "*phase-lock loop [PLL] device*" (50, brown, in the '912 patent above left) as required by claim 16. The PLL is important to the "*register*" because, according to the '912 patent, it "transmits clock signals to the plurality of memory

devices 30 [yellow], the logic element 40 [red], and the register 60 [green]." Appx83 (5:29-31). Using the clock signal from the PLL, the "register 60 [green] receives and buffers a plurality of control signals . . . and transmits corresponding signals to the appropriate memory devices 30 [yellow]." Appx83 (5:31-36).

Netlist does not contend that the '436 patent expressly discloses a circuit with a "*logic element*" and "*register*." Instead, Netlist relies on a two-step inference. First, Netlist asserts that PLD 642—a subpart of the red "logic element 640" in Figure 11A above right—uses "sequential logic," and, second, Netlist argues that a POSITA would understand that "sequential logic" may include a type of register. Br.56, 61 (citing Appx2503 (17:41-45, 18:6-11)). To support its position, Netlist depends on expert testimony about sequential logic incorporating a "register or an equivalent." Br.56.

The Board, however, rejected Netlist's arguments about sequential logic because there was also testimony in the record that sequential logic need ***not*** include a register: "For example, [Netlist's expert] recognizes that devices other than a register could be used when he refers to a '*storage* or register' as holding state, as does [Petitioner's expert] when he refers to a 'register or an *equivalent*.'" Appx31 (emphasis added by Board, internal citations omitted) (quoting Appx18345-46 ¶ 78;

Appx18694 (118:16-20)).[5] In view of this testimony, the Board found that the '436 patent's description of sequential logic does not demonstrate possession of a circuit with both a "*logic element*" and a "*register*," as in claim 16. Appx31-32.

Netlist's arguments on appeal do not show that the Board lacked substantial evidence. Netlist has merely identified a factual dispute that the Board resolved in Petitioner's favor. The Board was entitled to rely on expert testimony about sequential logic—along with the plain differences in the patent disclosures discussed above—to conclude that the '436 patent failed to disclose a "*circuit comprising a logic element and a register*." On appeal, Netlist asks this Court to weigh the same evidence differently, which is improper. "[The] task on appeal is simply to evaluate whether substantial evidence supports the Board's fact finding; we may not reweigh evidence." *Arthrex, Inc. v. Smith & Nephew, Inc.*, 935 F.3d 1319, 1329 (Fed. Cir. 2019) (cleaned up).

[5] The Board also cited online literature describing well-known devices like flip-flops and memory that could hold state. Appx31 n.7 (citing Appx21376-77). Because this citation merely confirms record testimony (quoted above) that other devices besides a register could be used in sequential logic, there has been no unfair surprise or prejudice to Netlist, *see Nike, Inc. v. Adidas AG*, No. 21-1903, 2022 WL 4002668, at *9 (Fed. Cir. Sept. 1, 2022) (nonprecedential) ("we find no APA violation here because neither citation was essential to the Board's . . . analysis"), contrary to Netlist's arguments, Br.58-59. Indeed, Netlist had accepted "the skill level proposed by Petitioner," Appx950, which included familiarity with "flip flops and registers," Appx134 (citing Appx13060 ¶ 50).

Netlist also contends that the Board's findings depended on an improper "*sua sponte* claim construction" requiring that "the logic element and register must be separate components." Br.60. To the contrary, neither party proposed any special constructions for the claimed "*register*" and "*logic element*," *see* Appx192, Appx1000-02, so the Board simply compared the disclosure of the '436 patent to the claim language. Appx31-32. Because claim 16 "lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (cleaned up); *accord Regeneron Pharms., Inc. v. Mylan Pharms. Inc.*, 130 F.4th 1372, 1379 (Fed. Cir. 2025). Indeed, Netlist itself recognizes that there is a "presumption that listing elements separately implies their separateness[.]" Br.60-61 (cleaned up). Consistent with that presumption, the '912 patent discloses that the "*logic element*" (40 in Figure 1A, *see* Appx63, Appx83 (5:30)) may include a PLD (42) with sequential logic, *see* Appx91 (22:60-61), Appx92 (23:18-19)—which Netlist contends implies some type of register, *see* Br.56—yet the '912 patent still discloses that the claimed "*register*" (60 in Figure 1A) is different from the "*logic element*" that Netlist contends includes registers (40 in Figure 1A, *see* Appx63, Appx83 (5:30-36)). Thus, even under Netlist's theory that sequential logic must include some type of register—which the Board rejected as discussed above—the Board reasonably determined that Netlist's theory would

not satisfy the claim language because "claim 16 recites that the 'logic element' and 'register' are two different things whereas the '436 patent [under Netlist's theory] describes the register as included in the logic element." Appx32.

The cases cited by Netlist are distinguishable. Br.61 (citing *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221 (Fed. Cir. 2021); *Linear Technology Corp. v. ITC*, 566 F.3d 1049 (Fed. Cir. 2009)). In *Powell*, the specification taught that one claim limitation ("cutting box") "may ***also*** function as" another claim limitation ("dust collection structure"), so unsurprisingly this Court concluded that the two claim limitations need not be "separate structures." 663 F.3d at 1231-32. The '912 patent, in contrast, never teaches that the claimed "*logic element*" may also function as the claimed "*register*," as explained above. And *Linear Technology* simply recognized that a "second circuit" and "third circuit" could share "overlapping components"—as was uncontested. 566 F.3d at 1055-56.

2. Netlist cannot rely on inferences from a POSITA's knowledge to show written description

Beyond the standard of review, Netlist's arguments about sequential logic should also be rejected because Netlist is seeking to impermissibly rely on the knowledge of a POSITA in place of any actual written description in the '436 patent. *See Knowles Elecs. LLC v. Cirrus Logic, Inc.*, 883 F.3d 1358, 1366 (Fed. Cir. 2018) (affirming lack of written description despite "prior art knowledge" of the claimed solder reflow process). While arguments about a POSITA's knowledge are

appropriate for enablement, the written description requirement serves a different purpose and has different requirements. *Ariad Pharms.*, 598 F.3d at 1351-52. Even if a POSITA could design a circuit with a logic and a register, that would not demonstrate Netlist possessed such an invention at the time of the '436 patent. *See id*.

None of the cases cited by Netlist supports reading a register into the disclosures of the '436 patent. Br. 55-58. The quote that a patent "preferably omits[] what is well known" refers specifically to the enablement requirement, not written description. *Hybritech Inc. v Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384 (Fed. Cir. 1986). In *Alcon Research Ltd. v. Barr Laboratories, Inc.*, the Court relied on direct disclosures from the patents in question, not the knowledge of a POSITA, to determine that written description was satisfied. 745 F.3d 1180, 1191 (Fed. Cir. 2014). In *Nalpropion Pharmaceuticals, Inc. v. Actavis Laboratories FL, Inc.*, the parties disputed whether data disclosed in a table supported a claim directed at administering specific amounts of compounds, not whether additional elements or steps could be inferred. 934 F.3d 1344, 1350 (Fed. Cir. 2019). Similarly, in *Hologic, Inc. v. Smith & Nephew, Inc.*, the parties disputed how a POSITA would interpret a disclosed feature (e.g., whether a light guide was "permanently affixed"), which the Court found was different than "rel[ying] on prior art to supply missing claim elements." 884 F.3d 1357, 1362, 1364 (Fed. Cir. 2018).

The cases cited by Netlist do not conflict with this Court's guidance about the role of knowledge of a POSITA for written description: "The knowledge of ordinary artisans may be used to inform what is actually in the specification, but not to teach limitations that are not in the specification, even if those limitations would be rendered obvious by the disclosure in the specification." *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017) (citations omitted). Here, Netlist is trying to do what this Court has repeatedly foreclosed—i.e., infer a "*register*" in the '436 patent based solely on the supposed knowledge of a POSITA. The Board correctly rejected Netlist's argument. Appx31.

3. Netlist did not attempt to show that every limitation of claim 16 is disclosed by the '436 patent

Netlist also failed to meet its burden of production, which required Netlist to show that every limitation of claim 16 is supported by the written description in the '436 patent. Appx33-34. In the Institution Decisions, the Board specifically instructed Netlist that it had a "burden of production . . . to show that the subject matter of claim 16 of the '912 patent is supported by its priority applications such that Ellsberry is not prior art." Appx488; Appx879-80. In its Patent Owner Response, Netlist acknowledged that it "needed to show support from the priority applications for ***each*** element of claim 16," Appx1016, but Netlist only tried to make that showing with its '244 provisional, *see* Appx1016-21, and not its '436 patent. Although Netlist discussed its '436 patent, Netlist did not attempt to show that ***each***

element of claim 16 was supported by the '436 patent, *see* Appx1000-08, as Petitioner pointed out in Reply, Appx1196-201.[6]

The Board correctly recognized that Netlist had not carried its burden of production to show that "an ancestor to the ['912] patent, with a filing date prior to the [Ellsberry] date, contains a written description that supports all the limitations of claim [16]." Appx34 (alterations by Board) (quoting *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008)).

Under the *Dynamic Drinkware* framework, "when a patent owner attempts to antedate an asserted prior art reference, the patent owner assumes a temporary burden of production." *Parus Holdings*, 70 F.4th at 1371 (citing *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378-79 (Fed. Cir. 2015)). That means Netlist needed to present evidence that the '436 patent "contains a written description that supports ***all the limitations*** of claim [16]." *Tech. Licensing*, 545 F.3d at 1327. "The burden of production cannot be met without some combination of citing the relevant record evidence with specificity and explaining the significance of the produced material in briefs. Here, [Netlist] did neither."

[6] Netlist raised new arguments in its Sur-Reply addressing additional limitations of claim 16 (including [16.e]), but still not all limitations. Appx1279-80. Petitioner sought to strike these untimely arguments. Appx21094-98; Appx1317-19, Appx1370-74. While the Board suggested that Netlist's new arguments may be improper, the Board did not expressly exclude Netlist's new arguments because "they would not negate the other discussed deficiencies in the '436 patent's written description." Appx32-33.

Parus Holdings, 70 F.4th at 1372. Because Netlist ignored several limitations of claim 16, the Board rightly held that Netlist fell short of this burden. Appx34.

Because the Board properly followed this Court's precedent from *Technology Licensing* and *Dynamic Drinkware*—and specifically instructed Netlist about its burden of production, Appx879-80, which Netlist acknowledged, Appx1016—Netlist's invocation of *Jicarilla* is misguided. Br.63 (citing *Jicarilla Apache Nation v. U.S. Dep't of Interior*, 613 F.3d 1112, 1119 (D.C. Cir. 2010)). *Jicarilla* dealt with contradictory decisions by the Department of the Interior on the calculation of gas royalties for the same leasing agreements, which were upheld in a first case but struck down in a later case. 613 F.3d at 1115-16. The facts here are different: the previous non-precedential Board decisions that Netlist cites involved entirely different patents, parties, and facts. *Jicarilla* itself confirms that the Board does not need to go as far as Netlist suggests in addressing different prior decisions: "we do not require an agency to grapple with every last one of its precedents, no matter how distinguishable." *Id.* at 1120. In any event, the Board's decision here was consistent with this Court's precedent as well as previous Board decisions. *See* Appx1554-55 (62:10-63:3) (quoting *Cont'l Auto. Sys., Inc. v. Intell. Ventures II LLC*, IPR2022-00972, Paper 49, at 28 (PTAB Dec. 5, 2023) ("Petitioner was not required to rebut in advance Patent Owner's argument and evidence alleging priority to the '421

application.")); *MaxLite, Inc. v. Jiaxing Super Lighting Elec. Appliance Co.*, IPR2020-00208, 2021 WL 2221251, at *1-4 (PTAB June 1, 2021) (similar).

Netlist also overstates the non-precedential Board decisions on this issue. None of the cases cited by Netlist shows that the Board previously "require[d] patentees to address ***only*** 'the specific points and contentions raised' in the petition." Br.62 (emphasis by Netlist) (quoting *Lupin Ltd. v. Pozen, Inc.*, IPR2015-01775, Paper 15, at 10-11 (PTAB Mar. 1, 2016)). *Lupin* was an institution decision, made on a preliminary record, that merely held for purposes of denying institution on a particular ground that "Patent Owner provides a sufficient showing of entitlement to the filing date of the '216 application (the '255 publication) in a manner that is commensurate in scope with the specific points and contentions raised by Petitioner." *Lupin*, Paper 15, at 11, 15. But that does not absolve a Patent Owner of its burden of production at trial, after institution, with respect to each limitation, as required by *Technology Licensing* and *Dynamic Drinkware*.

None of the other Board decisions cited by Netlist for this allegedly "established precedent" found that a patent owner addressing less than all of the claim limitations had met its burden of production. The Board expressly recognized in *Fitbit, Inc. v. BodyMedia, Inc.*, that "Patent Owner has provided citations to written description support in the June 2000 applications for the remaining limitations" of the claim at issue. IPR2016-00707, Paper 9, at 10-11 (PTAB Sept.

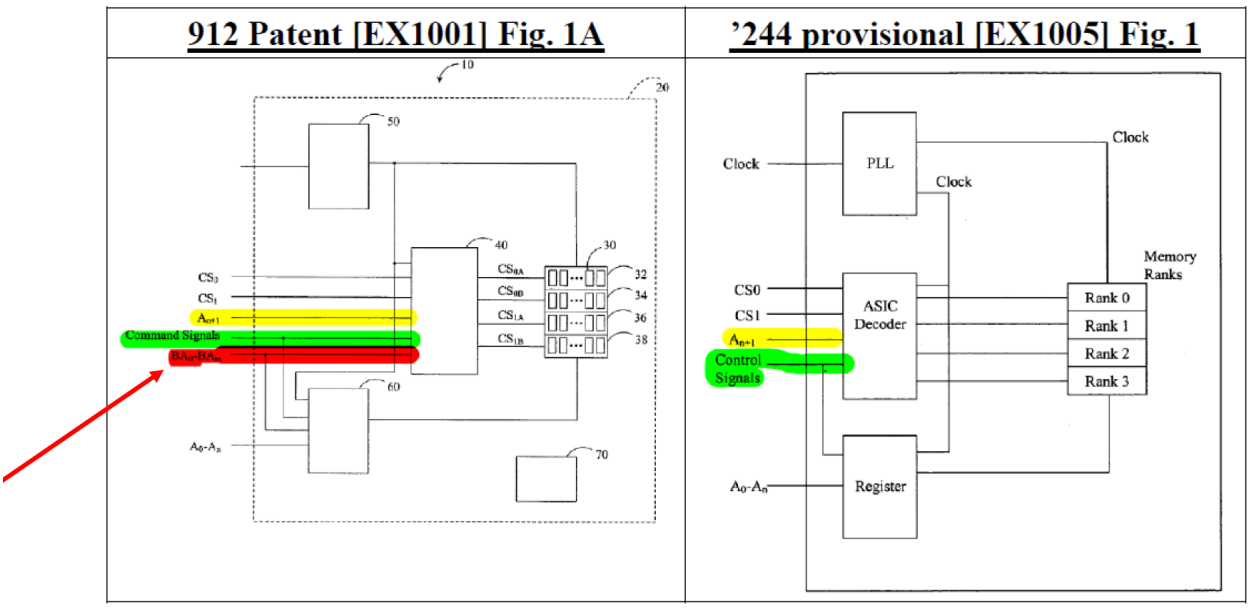
8, 2016). In *Mission Integrated Technologies, LLC v. Clemente*, the Board held that the petitioner's single-sentence argument was insufficient to even shift the burden to the patent owner on priority. IPR2023-01285, 2024 WL 752892, at *8 (PTAB Feb. 23, 2024). And in *Lumi Legend Corp. v. Manehu Product Alliance, LLC*, the patent owner never even substantively disputed the petitioner's priority argument, and the Board therefore accepted the *petitioner's* position. PGR2024-00014, 2024 WL 3656822, at *4 (PTAB Aug. 5, 2024).

At most, Netlist has identified one non-appealable institution decision (*Lupin*) where the Board accepted a Patent Owner's preliminary arguments about priority without evaluating every limitation. That Board decision is insufficient to overcome this Court's prior holding that a priority application must "contain[] a written description that supports ***all the limitations*** of claim [16]." *Tech. Licensing*, 545 F.3d at 1327. The Board was correct to find that Netlist's "attempt to gain the benefit of the filing of the '436 patent fails for this additional reason." Appx34.

B. Claim 16 is not supported by the '244 provisional

Substantial evidence also supports the Board's finding that the '244 provisional does not provide written description for at least the claimed "*bank address signals*." Appx24-30, Appx34. Figure 1A of the '912 patent, below left, shows bank address signals (BA_0-BA_m, red below) being sent to the logic element (Appx84 (7:50-51))—in addition to command signals (green, Appx84 (8:17, 8:44-

48))—but Figure 1 of earlier the '244 provisional, below right, conspicuously ***omits*** these bank address signals while still showing the same control signals (green, Appx2340-41 ¶¶ [0011 note 4], [0019]):



Appx21212 (annotating Appx63, Appx2344); Appx27. In addition to the facial differences between the '912 patent and '244 provisional above, substantial evidence for the Board's conclusion can be found in the declaration of Petitioner's expert. Appx13164 ¶ 189 (explaining the absence of bank address signals in the '244 provisional); Appx25-29 ("We agree with Petitioner").

Similar to its arguments for the '436 patent, Netlist does not argue that the '244 provisional directly discloses "*bank address signals*." That is because the '244 provisional never mentions bank address signals and never suggests they would be sent to the alleged "*logic element*" (i.e., the ASIC Decoder) as required by limitation

[16.c.i]. Appx2338-44. Instead, Netlist argues a POSITA would have understood the "control signals" appearing in the '244 provisional figure (green above) included "*bank address signals*." Br.63-64. Netlist bases that assertion on the disclosure of "bank address signals" in the JEDEC standard for DDR memory devices, rather than anything in the '244 provisional. *Id.* (citing Appx11193). But that JEDEC standard does not call bank address signals "control signals"—instead it distinguishes between "address and control" signals—and it teaches that bank address signals go to the memory device, *see* Appx11188-93, not to a "*logic element*" (e.g., the ASIC Decoder in the '244 provisional) as required by limitation [16.c.i]. Similarly, Figure 1 in the '244 provisional, shown above on the right, also distinguishes "control signals" (green) from address signals (A_{n+1} and A_0-A_n) and teaches that address signals "A_0-A_n" (on the bottom left of the figure above) do ***not*** go to the "*logic element*" (e.g., ASIC Decoder), so there is no reason to assume that any bank address signals (if they existed in the '244 provisional) would go to the "*logic element*" as claimed. Appx2339-40 ¶¶ [0009-0011], Appx2344.

In any event, as the Board correctly observed, the '244 provisional itself is completely silent as to JEDEC standards and a skilled artisan would need to "infer[]" that the JEDEC standard should be used after "assum[ing]" that the '244 provisional refers to DDR devices. Appx29-30. And there is no basis for even that assumption: The '244 provisional does not "mention" DDR memory devices at all (as required

by limitation [16.b]). Appx29. It simply refers to "DRAM" devices. *See, e.g.*, Appx2338 ¶ [0001]. Netlist argues that use of terms like "rank" and "chip-select" suggests a "JEDEC-style memory module." Br.63 (quoting Appx18313-14). But those terms do not suggest ***DDR*** memory devices, given that numerous other "DRAM" devices were known at the time and standardized by JEDEC that were ***not*** capable of DDR operations. Appx29; *see, e.g.*, Appx18649 (73:3-8); Appx11813-14; Appx12268 (JESD 21-C), Appx12341-48 (Page 3.9-1 to 3.11.4-34), Appx12175-78. And Petitioner's expert did not testify that personal computers "***w***ould" use DDR, as Netlist incorrectly argues. Br.64. He merely said they "***c***ould." Appx18649 (73:9-15).

Because the '244 provisional is not limited to JEDEC standards and does not incorporate any particular standard by reference, Netlist cannot cherry pick particular JEDEC standards to fill gaps in the '244 provisional's written description. *See, e.g.*, *L.A. Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1058 (Fed. Cir. 2017); *Rivera*, 857 F.3d at 1322.

Netlist ignores this precedent and turns instead to a discussion of indefiniteness in *Wellman, Inc. v. Eastman Chemical Co.* to assert that "skilled artisans 'interpret[]' patent-application disclosures in view of industry 'standard[s].'" Br.63 (quoting 642 F.3d 1355, 1367-68 (Fed. Cir. 2011)). This sleight of hand fails to address that the test for written description is different, and

must always focus on the four corners of the specification, not what was obvious or known by others. *Rivera*, 857 F.3d at 1322 (citing *Ariad*, 598 F.3d at 1351). Furthermore, *Wellman* rejected the district court's indefiniteness conclusion based on a factual determination, not a sweeping statement of law about industry standards as suggested by Netlist: "The record suggests no reason that a [POSITA] would have been incapable of applying those moisture conditioning standards to the claimed invention to achieve consistent, repeatable TCH measurements." 642 F.3d at 1368. *Wellman* provides no reason to rewrite the law of written description.

Accordingly, Netlist's arguments about "*bank address signals*" in the '244 provisional fail. Every argument that Netlist makes depends on the JEDEC DDR standard to provide the missing "*bank address signals*" for the '244 provisional. But substantial evidence supports the Board's conclusion that "there is no mention of DDR" in the '244 provisional and thus no basis for Netlist's arguments. Appx29-30.

Substantial evidence also supports the Board's rejection of Netlist's "chain of inferences." Appx29-30. First, Netlist improperly focuses on just the final of the five inferences. Br.65. But the Board properly concluded that Netlist's proposed chain of inferences was "too long and speculative to show that the '244 provisional demonstrates that the inventors had possession of the subject matter of claim 16." Appx30. Second, substantial evidence supports the Board's rejection of the

inference "that the bank address signals are used for rank multiplication (when row/ and column/address could have been used for this purpose)." *Id.* Netlist itself showed during reexamination that rank multiplication does ***not*** require "*bank address signals*," as Petitioner pointed out. Appx1202, Appx1196-97 (citing Appx9582-87 / Appx10555-60; Appx20034-35 (67:15-68:6); Appx20038 (71:4-12); Appx11874-75, Appx11877). Thus, the Board was justified in concluding that a POSITA would not infer that bank address signals would be used by the "*logic element*" in the manner recited by claim 16—especially since bank address signals are not mentioned anywhere in the '244 provisional.

V. Netlist insufficiently presented its alternative arguments for vacatur

In the final paragraph of its brief, Netlist disagrees with binding precedent for "issue-preservation purposes," Br.66 (citing *Lynk Labs* and *Thryv*), but Netlist's "conclusory assertion with no analysis is insufficient to preserve the issue for appeal." *Trading Techs. Int'l, Inc. v. IBG LLC*, 921 F.3d 1378, 1385 (Fed. Cir. 2019).

CONCLUSION

For the foregoing reasons, Appellees respectfully request that the Court affirm the Board's determination that claim 16 the '912 patent would have been obvious in light of Ellsberry (Ground 3). Otherwise, Appellees request remand for the Board to consider Grounds 1 and 2 in the first instance. Appx133.

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Respectfully submitted,

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FORM 19. Certificate of Compliance with Type-Volume Limitations **Form 19**
July 2020

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2024-2304

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