Nos. 2023-2158, -2159

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VLSI TECHNOLOGY LLC,

Appellant,

v.

OPENSKY INDUSTRIES, LLC,

Cross-Appellant,

INTEL CORPORATION,

Appellee,

DERRICK BRENT, Acting Under Secretary of Commerce for Intellectual Property and Acting Director of the United States Patent and Trademark Office,

Intervenor.

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2021-01064 and IPR2022-00366

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PATENT CLAIMS AT ISSUE

1. A method comprising:

monitoring a plurality of master devices coupled to a bus;

receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

in response to receiving the request from the first master device:

providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and

providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

14. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

receive the request provided by the first master device;

provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device

coupled to the bus in response to receiving the request provided by the first master device; and

provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

17. The system of claim 14, wherein the instructions to provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus include instructions to adjust the clock frequency of the bus.

18. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus;

an arbiter coupled to the bus and coupled to the first master device, the arbiter configured to control flow of data on the bus; and

a clock controller coupled to the arbiter and coupled to the first master device, the clock controller configured to output a clock frequency of a high-speed clock to control the variable clock frequency of the bus and to control a clock frequency of a second master device coupled to the bus, the clock controller configured to receive a request to change the clock frequency of the high-speed clock from the first master device, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the clock controller is configured to adjust the variable clock frequency of the bus in response to receiving the request from the first master device, and wherein the predefined change in the performance is due to loading of the first master device as measured within a predefined time interval.

21. The system of claim 18, wherein adjusting the variable clock frequency of the bus comprises decreasing the clock frequency of the bus.

22. The system of claim 18, wherein adjusting the variable clock frequency of the bus comprises selecting the variable clock frequency to be a frequency divisible by a factor of 1, 2, 4, 8, or 16.

24. The system of claim 18, wherein the predefined change in the performance of the first master device comprises a variation in load of the first master device.

Appx251-252.

CERTIFICATE OF INTEREST

Counsel for Appellee Intel Corporation certifies the following:

1. Represented Entities. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

Intel Corporation

2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

None.

3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

WILMER CUTLER PICKERING HALE AND DORR LLP: David Cavanaugh

5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

[X] Yes (file separate notice; see below) [ ] No [ ] N/A (amicus/movant)

Already Filed.

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). Please do not duplicate information. This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None.

Dated: January 21, 2025

/s/ William F. Lee

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STATEMENT OF RELATED CASES

This Court previously decided an appeal from a district-court judgment that involved the same patent at issue in this IPR appeal. *See VLSI Technology LLC v. Intel Corporation*, No. 2022-1906, 87 F.4th 1332 (Fed. Cir. Dec. 4, 2023) (Taranto, J., joined by Lourie & Dyk, JJ.). This Court also previously dismissed Intel's appeals challenging the Patent Trial and Appeal Board's discretionary decisions not to institute IPRs of several patents, including the one at issue in this appeal. *See Intel Corporation v. VLSI Technology LLC*, Nos. 2021-1614, -1616, -1617, 2021 WL 5968443 (Fed. Cir. May 5, 2021) (Prost, C.J., joined by O'Malley & Wallach, JJ.).

The Court's decision in this IPR appeal may directly affect or be directly affected by the parallel district-court litigation: *VLSI Technology LLC v. Intel Corporation*, No. 6:21-cv-00057 (W.D. Tex.) (formerly No. 6:19-cv-00254). Intel is not aware of any other case pending in this Court or any other court that will directly affect or be directly affected by the Court's decision in this appeal.

INTRODUCTION

This appeal involves U.S. Patent No. 7,725,759, which VLSI asserted against Intel in the Western District of Texas in 2019. This Court has since held that Intel does not infringe the '759 patent, and the Patent Trial and Appeal Board has found all of the asserted claims (and others) to be unpatentable in an *inter partes* review. VLSI now appeals from the Board's final written decision, but the Board correctly

determined that every challenged claim of the '759 patent would have been obvious on two independent prior-art grounds. The Board's decision is well-reasoned and supported by substantial evidence, and should be affirmed.

VLSI's substantive challenges to the Board's obviousness determinations merely rehash arguments that the Board properly decided against VLSI based on the record evidence. For one prior-art ground, VLSI disputes only the Board's factual finding that skilled artisans would have been motivated to combine the two references to save power. That finding is amply supported by substantial evidence, including the prior art itself and testimony from both sides' experts. For the other prior-art ground, VLSI raises a claim-construction argument concerning the word "request." The Board correctly applied the claim language's plain meaning and rejected VLSI's attempt to read in an unsupported negative limitation. While the Board was correct to find obviousness on both grounds, affirmance on ***either*** ground requires upholding the Board's unpatentability determinations for all challenged claims.

VLSI also tries to sidestep the Board's well-supported obviousness findings by raising a handful of procedural arguments that have no bearing on the challenged claims' unpatentability. For example, VLSI objects to the form of the Board's written decision on issues that VLSI never disputed during the IPR. The Board's 44-page explanation was more than sufficient: the Board fully addressed every

argument that VLSI raised and properly adopted Petitioners' arguments and evidence on uncontested issues. VLSI also challenges Intel's participation in the IPR, but Intel was properly joined to this proceeding under 35 U.S.C. §315, which expressly provides that its one-year limit for infringement defendants to file IPR petitions "shall not apply" to joinder requests.

VLSI spends the bulk of its brief attacking the Director's decisions addressing OpenSky's misconduct.[1] Though VLSI would have preferred a different result, the Director was well within her discretion not to void the entire IPR as a sanction against OpenSky. The Director engaged in a thorough review process and provided reasoned explanations for how she dealt with OpenSky's behavior. The Director made clear that she sought to balance deterring misconduct with ensuring reliable patent rights and, after considering the facts, concluded that terminating the IPR was unwarranted because OpenSky's petition presented "compelling" unpatentability arguments. Appx84; *see* Appx119-124. The Director ultimately ordered OpenSky to pay VLSI $413,264.15 in attorney fees—an amount that VLSI fails to mention but that includes all of VLSI's requested fees for its time spent addressing OpenSky's behavior found to be abusive during the IPR. The Director's decision to

[1] To be clear, Intel did not engage in any misconduct. Appx139. VLSI does not contend otherwise.

impose sanctions less than termination of the whole proceeding was easily within her broad discretion and should be affirmed.

JURISDICTIONAL STATEMENT

This Court lacks jurisdiction to review the Board's decision allowing Intel's joinder (Appx17-20) and the Director's decision not to terminate the IPR (Appx119-124; Appx90-102; Appx81-87) because VLSI's arguments on those issues are challenges to institution decisions, which are "nonappealable" under 35 U.S.C. §314(d). *Infra* pp. 46-48, 50-53.

STATEMENT OF ISSUES

1. Whether the Board's obviousness determinations should be affirmed based on the Chen/Terrell ground, where substantial evidence supports the Board's motivation-to-combine finding.

2. Whether the Board's obviousness determinations should additionally be affirmed based on the Shaffer/Lint ground, where the Board: (a) correctly construed "request" to have its plain meaning without reading in VLSI's proposed negative limitation, and (b) provided a sufficient written decision when it adopted Petitioners' undisputed contentions regarding Lint.

3. If reviewable, whether the Board properly allowed Intel's joinder, where 35 U.S.C. §315(b) provides that its one-year limit for infringement defendants to file IPR petitions "shall not apply" to joinder requests.

4. If reviewable, whether the Director acted within her discretion in denying VLSI's request to terminate the IPR as a sanction against OpenSky.

STATEMENT OF CASE

A. The '759 Patent

The '759 patent relates to "managing clock speeds within electronic devices." Appx248(1:6-7). Clock speed, or frequency, is the speed at which an electronic device operates. Appx4045-4046(¶62). As was well known in the art, increasing clock speed increases a device's performance or speed of operation, but it also consumes more power. Appx248(1:16-21); Appx4045-4047(¶¶60-63). The '759 patent sought to balance the competing goals of faster performance and power savings by "selectively deliver[ing]" clock speeds in an electronic device—that is, increasing clock speed when faster performance is desired and decreasing clock speed at other times. Appx248(1:22-24); Appx4054-4055(¶72).

The '759 patent describes an electronic system that includes two or more "master devices" (120, 122)—which may be, for example, central processing units ("CPUs") or processors—connected via a "bus" (102):

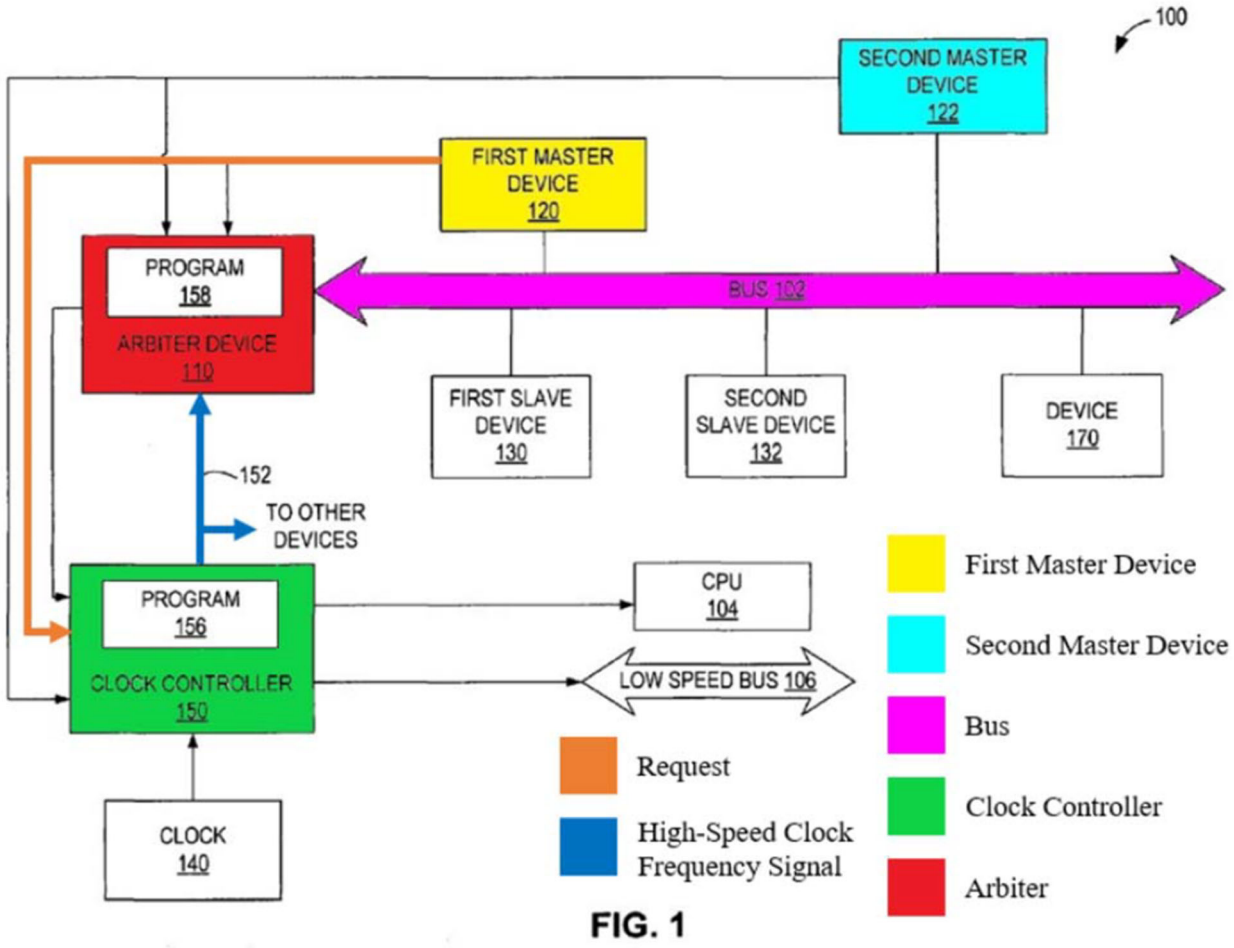

FIG. 1

Appx1015; *see* Appx242(Fig.1); Appx248-249(2:58-3:10, 3:22-28). A "first master device" (120) sends a "request" to a "clock controller" (150) to change the frequency of a high-speed clock. Appx240(abstract); Appx248(1:45-53). The request may be triggered, for instance, by an increase in needed performance due to increased workload demands for the first master device. Appx249(3:64-4:19). In response to the request, the clock controller provides the new clock frequency to the bus and other devices (e.g., "second master device" 122) connected to the bus. Appx249(4:20-29). In some embodiments, the system also includes an "arbiter"

(110) that controls the bus's data flow. Appx249(3:11-12, 4:30-41); *see* Appx4052-4055(¶¶69-73).

Claim 1 provides:

> 1. A method comprising:
>
> monitoring a plurality of master devices coupled to a bus;
>
> receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and
>
> in response to receiving the request from the first master device:
>
> providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and
>
> providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

Appx251(7:66-8:15). Claim 14 and dependent claim 17 recite a system (rather than a method) that incorporates similar limitations as claim 1. Appx251-252(8:50-9:4, 9:15-18); *see* VLSI Br. at inside cover, 7 (describing claim 1 as "representative" and "illustrative" on appeal).

Claim 18 and dependent claims 21, 22, and 24 are also similar, but they additionally require an "arbiter" that is "coupled to the bus and … first master device[.]" Appx252(9:19-40, 10:10-23).

B. The Prior Art

Like the '759 patent, many prior-art references describe dynamically selecting clock speeds for devices connected via a bus. The Board's unpatentability determinations focused on five references from this field, summarized below.

1. Chen

U.S. Patent 5,838,995 ("Chen") discloses a bus system with circuitry "for switching between different data transfer speeds." Appx4315(1:61-62). More specifically, the system includes control logic to allow "bus transactions at both a high frequency and a lower frequency." Appx4315(2:1-6); *see* Appx4311-4318; Appx4058-4065(¶¶75-82).

Chen's Figure 1 depicts a system with two devices (34, 36) connected to a bus (40):

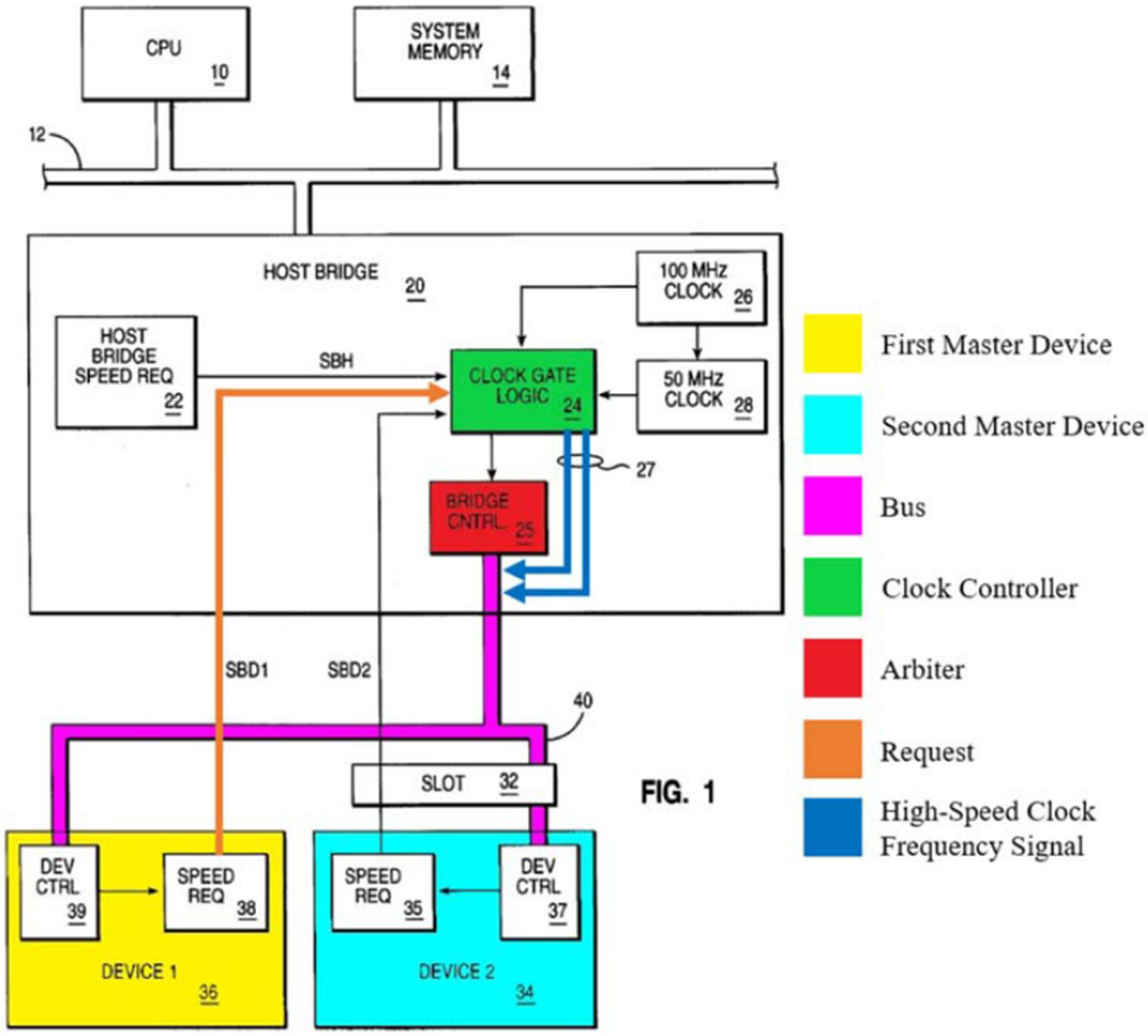

FIG. 1

Appx1018; *see* Appx4312(Fig.1). Each device includes a "speed requesting circuit" (35, 38) that may send a signal (SBD1, SBD2) requesting a specific clock speed to a "clock gate logic circuit" (24). Appx4316(3:4-22). In response to such a request, the clock gate logic circuit dynamically changes the bus's frequency by providing a faster or slower clock (26, 28) to the bus and both devices (34, 36). Appx4316(3:20-22).

Although Chen discusses the performance benefits from increasing clock speed, Chen also recognizes that not all devices should always be operated at the fastest possible speed. Appx4063-4065(¶82). For example, Chen discloses that a device may request a faster clock speed (e.g., 100 MHz) for certain types of transactions (e.g., when writing to or reading from memory) but operate at a lower clock speed (e.g., 50 MHz) for other transactions. Appx4316(4:11-33). Chen also teaches that devices not directly involved in a particular high-speed transaction may operate at a lower clock speed. Appx4317(5:21-24).

2. Terrell

U.S. Patent Application 2004/0098631 ("Terrell") discloses controlling the frequency of a common clock shared by two or more processors connected to a bus. Appx4319-4326; *see* Appx4087-4092(¶¶105-111). Terrell states that "it is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the process[ors] to function correctly while using the least amount of power." Appx4323(¶5); *see* Appx4323(¶¶6-8).

Terrell's Figure 1 is below:

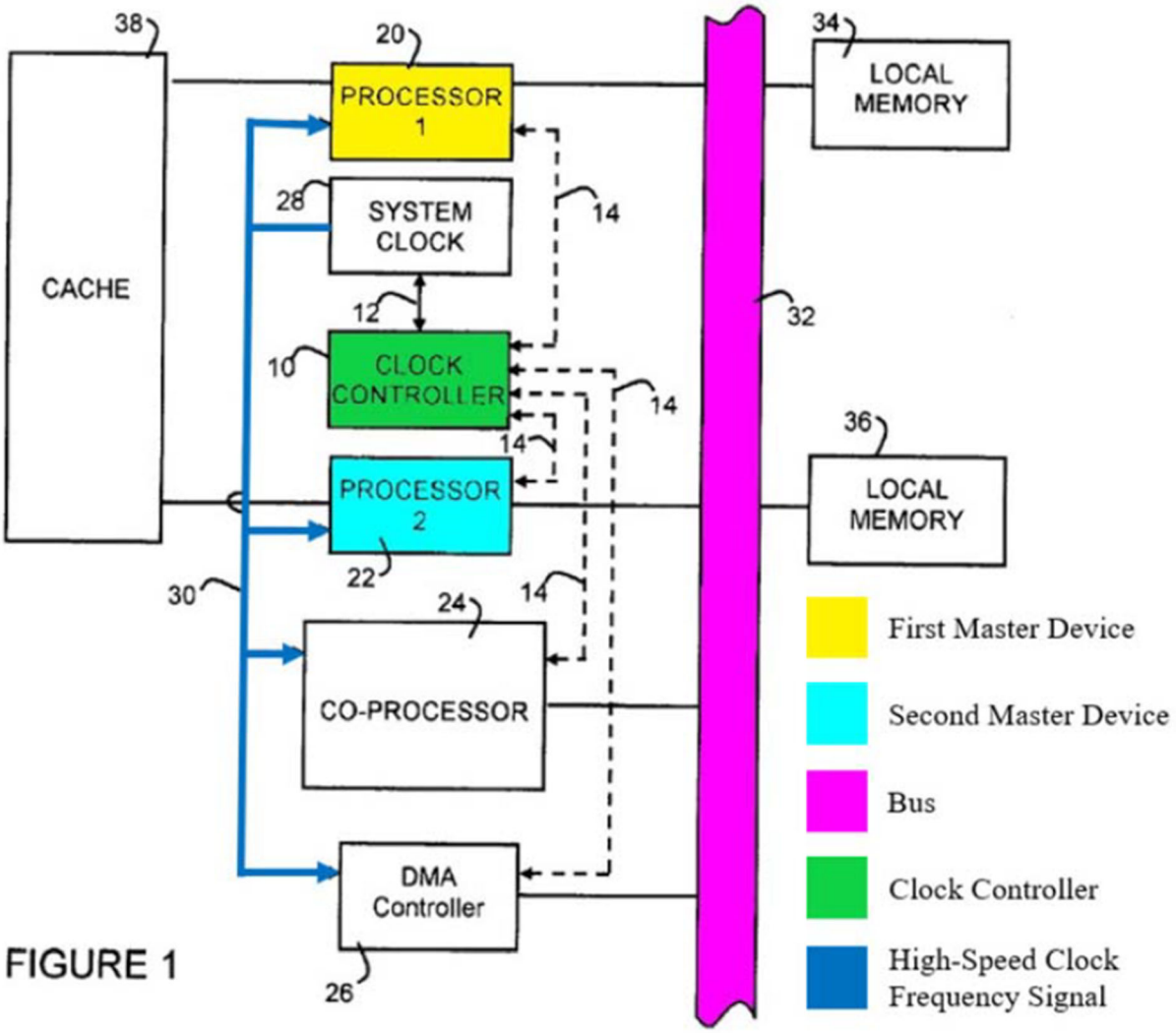

FIGURE 1

Appx1019; *see* Appx4320(Fig.1). Multiple processors (e.g., 20, 22) are connected to a bus (32) and share a common system clock (28). Appx4324(¶¶22-23). A clock controller (10) communicates with both the clock and processors. Appx4324(¶24).

Terrell teaches that the system clock's frequency may be varied "upwardly and downwardly, as a function of the measured 'idleness' of the processors[.]" Appx4325(¶54). Terrell discloses a two-step process for dynamically changing the clock speed based on performance needs: (1) measure how busy each processor is

during a sample period; and (2) adjust the system clock to the lowest speed required by the processor with the greatest workload. Appx4324(¶¶25-27); Appx4322(Fig.3). For instance, if the system has been 50% idle during a recent period, the clock speed may be reduced by roughly a factor of two. Appx4092(¶111). This approach allows the system to reduce the power consumed while still meeting performance requirements. *Id.*

3. Shaffer

U.S. Patent 6,298,448 ("Shaffer") discloses a system that provides "the CPU and other system buses in the device with a variable clocking frequency based on the application or interrupt being executed by the device." Appx4327(abstract); *see* Appx4327-4334. Shaffer's Figure 1 is below:

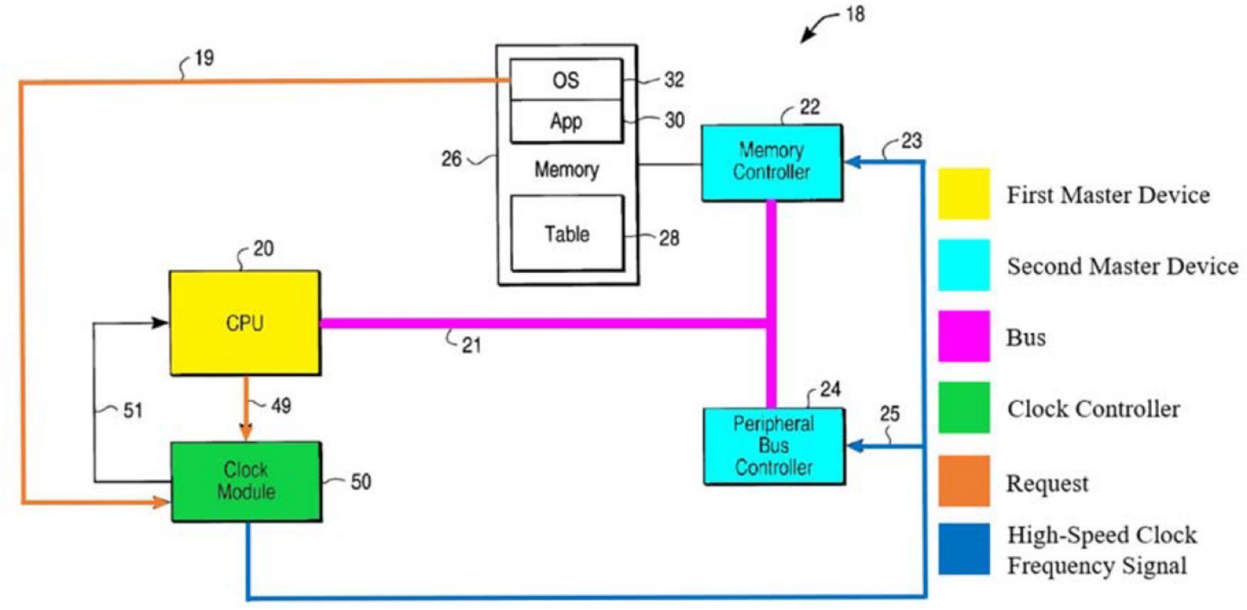

FIG. 1

Appx1020; Appx4328(Fig.1). A number of master devices—which may be multiple CPUs (20)—are connected via a bus (21). Appx4331(3:8-11); Appx4332(6:2-5). A "programmable clock module" (50) provides the CPUs and other devices with a clock signal (via lines 51, 23, 25). Appx4331(3:8-16).

The CPU sends "instructions" via line 49 to change the frequency of clock module (50) as needed. Appx4331(3:16-22). The operating system (OS 32) may also generate "an interrupt to the clock module 50," via line 19, "instructing it to raise or lower the clocking frequency provided to the CPU 20." Appx4332(5:5-8); *see* Appx4331(3:52-56, 4:3-4, 4:50-54). The OS may do this based on "a CPU utilization application that dynamically monitors the level of CPU usage." Appx4331(4:53-54); *see* Appx4331-4332(4:50-5:20). Shaffer teaches that its system improves power efficiency because "the most cost effective method to reduce power consumption is to vary the CPU 20 clock speed." Appx4332(6:12-14); *see* Appx4330(1:38-40) ("Power saving features have become increasingly important over the past few years[.]"); Appx4071-4078(¶¶89-96).

4. Lint

U.S. Patent 7,360,103 ("Lint") describes a hardware mechanism for determining a processor's frequency based on processor utilization data. Appx4335-4348. Lint's Figure 6 shows two processors (670, 680) connected through a chipset to a bus (616):

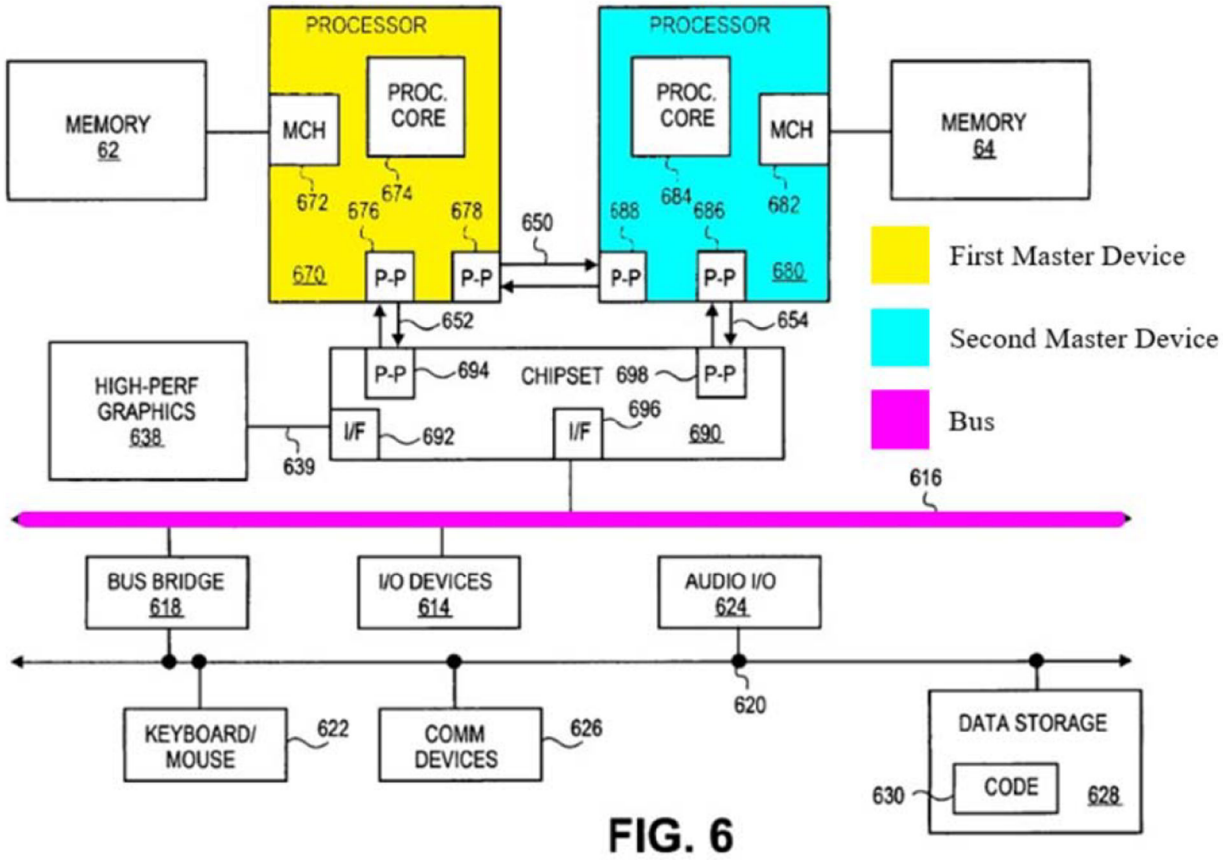

FIG. 6

Appx1021; *see* Appx4341; Appx4346(9:25-60).

Lint discloses that its operating system requests a processor "P-state," which corresponds to clock frequency, based on a processor's utilization level (e.g., a processor's "average performance" over a recent period). Appx4343(3:1-7); *see* Appx6108-6109. The operating system sends a signal—interchangeably referred to as a "request," "instruct[ion]," or "command"—to set the new P-state. Appx4343-4346(3:18-19, 4:43-44, 5:46-48, 9:16-20). Lint teaches that its approach aims "to provide for the best performance while saving power." Appx4342(2:29-32); *see* Appx4065-4070(¶¶83-88).

5. Kiriake

U.S. Patent Application 2003/0159080 ("Kiriake") discloses a bus system with multiple processors, a clock controller, and an "arbiter." Appx4805-4816; *see* Appx1022. The arbiter "performs arbitration relating to use of th[e] system bus." Appx4812(¶11); *see* Appx4813(¶22); Appx5339-5344(¶¶95-99).

C. VLSI's Lawsuits Against Intel And Intel's Initial IPR Petitions

VLSI was formed in 2016 by Fortress Investment Group LLC, a hedge fund represented by VLSI's counsel. No. 2022-1906, ECF 17 at 6-7 (Fed. Cir.). Days after its formation, VLSI began acquiring patents from NXP Semiconductors. *Id.* VLSI has two employees and has never made or sold products. *Id.* VLSI's only business has been suing Intel for alleged infringement of its purchased patents, though nearly all of VLSI's asserted patents have been found invalid or not infringed or have been dismissed from VLSI's lawsuits.

VLSI initially sued Intel in California and Delaware alleging infringement of thirteen patents. In March 2019, VLSI filed another Delaware lawsuit to assert the '759 patent and five others. No. 1:19-cv-00426 (D. Del.). One month later, VLSI voluntarily dismissed that case and refiled it as three actions (with two additional patents) in the Western District of Texas. Appx7321-7322. Through this forum-shopping, VLSI obtained a much faster time-to-trial schedule than available in California or Delaware. *See* Anderson & Gugliuzza, *Federal Judge Seeks Patent*

Cases, 71 Duke L.J. 419, 468 (2021) (noting the Texas court's practice of "setting early trial dates … allow[ed] litigants to avoid PTAB review").

Intel filed two timely IPR petitions against the '759 patent in October 2019 and February 2020. Intel's petitions, which were supported by expert declarations from Dr. Bruce Jacob, challenged several claims as obvious over Shaffer and Lint (and Kiriake) as well as Chen and Terrell (and Kiriake). Appx17001-17087; Appx18001-18096; *see* IPR2020-00106, Ex. 1002; IPR2020-00498, Ex. 1102. In May and August 2020, the Board denied Intel's petitions without reaching the unpatentability merits. Appx17159-17173; Appx18168-18179; *see* Appx43. The Board discretionarily denied institution under its then-applicable interpretation of *Apple Inc. v. Fintiv, Inc.*, 2020 WL 2126495 (P.T.A.B. Mar. 20, 2020) (precedential), reasoning that it would be unlikely to issue IPR decisions before the then-scheduled Texas trial. Appx17165-17166; Appx17170-17171; Appx18173; Appx18177.[2]

The Texas trial did not occur on the schedule that VLSI leveraged to oppose Intel's IPR petitions. It took place nearly five months later in February/March 2021. At trial, VLSI alleged that Intel infringed claims 14, 17-18, and 24 of the '759 patent.

[2] Two years later, the new Director issued a *Fintiv* memorandum explaining that the Board must "consider[] the merits of a petition[]" and "compelling, meritorious challenges will be allowed to proceed at the PTAB even where district court litigation is proceeding in parallel." Appx7370-7372.

Appx4798-4800. Intel denied infringement and contended that the asserted claims were invalid as anticipated by a prior-art product known as the "Yonah" processor. Appx4801. The jury found that Intel infringed under the doctrine of equivalents (but not literally) and that Intel had not proved invalidity based on "Yonah" by clear-and-convincing evidence, and awarded damages of $675 million for the '759 patent. Appx4798-4803. The district court entered final judgment in April 2022, well over two years after Intel's IPR petitions. Appx7365-7367.

Intel appealed on infringement and damages. In December 2023, this Court reversed the infringement judgment for the '759 patent, holding that VLSI's expert testimony was "insufficient" and "VLSI's doctrine of equivalents theory fail[ed] as a matter of law." *VLSI*, 87 F.4th at 1344-1345.

D. The IPR Proceedings

1. The Board's institution and joinder decisions

In June 2021, OpenSky—an entity with no connection to Intel—filed an IPR petition challenging certain claims of the '759 patent on grounds included in Intel's earlier petitions:

Challenged Claims	Obviousness Grounds
1, 14, 17	Shaffer, Lint
18, 21-22, 24	Shaffer, Lint, Kiriake
1, 14, 17	Chen, Terrell
18, 21-22, 24	Chen, Terrell, Kiriake

Appx1001-1065; *see* Appx1525-1557. OpenSky's petition was supported by two expert declarations from Dr. Jacob, which Intel had submitted with its earlier IPR petitions and which OpenSky subsequently attached to its own petition. Appx4014-4277; Appx5276-5711; *see also* Appx5914-6000 (reply declaration).

The Board instituted review in December 2021. Appx1215-1244. Immediately thereafter, Intel filed an IPR petition based on the same prior-art references and grounds as OpenSky's petition and moved to join the OpenSky proceeding. Appx14001-14086; Appx14087-14107. In June 2022, the Board instituted Intel's petition and granted Intel's joinder request, noting that joining Intel would not "add significant issues or evidence burdening the Board." Appx15; *see* Appx1-21.

2. The Director's review of institution

In response to VLSI's rehearing request following institution of OpenSky's IPR petition, the Director initiated "review of the Board's [i]nstitution [d]ecision" in June 2022. Appx1449. The Director commenced proceedings to address VLSI's allegations that OpenSky had abused the IPR process. Appx30-31. In addition to requesting briefing, the Director ordered the parties to produce documents and answer interrogatories relating to OpenSky's business and communications about the '759 patent or the IPR. Appx31-34. Intel responded by providing the requested discovery, making clear that Intel had never heard of OpenSky before OpenSky filed

its petition and explaining why the IPR should continue to a final merits decision. Appx1669-1702; Appx2095-2115. VLSI asked the Director to terminate the IPR. Appx1769; Appx1788-1792.

In October 2022, the Director determined that OpenSky engaged in sanctionable conduct in multiple respects. Appx38-88. The Director found that OpenSky failed to comply with her discovery order by refusing to produce confidential documents or a privilege log and providing insufficient interrogatory responses. Appx56-62. Given those discovery violations, the Director applied adverse inferences against OpenSky in analyzing whether its conduct was an abuse of process. Appx39-40; Appx62-65. The Director then determined that "OpenSky, through its counsel, abused the IPR process by filing this IPR in an attempt to extract payment" from both VLSI and Intel. Appx40. As the Director explained, "such double-dealing suggests that a petition was filed purely to extract rents, in either direction, rather than for legitimate purposes." Appx76-77. The Director also found that "OpenSky engaged in abuse of process and unethical conduct by offering to undermine and/or not vigorously pursue this matter in exchange for a monetary payment." Appx40. For example, OpenSky threatened that it would not depose VLSI's expert or file a reply brief in the IPR as part of its efforts to extract payment from Intel—which Intel, of course, refused to do. Appx69-71; Appx77-79; *see* Appx66-81.

The Director then addressed what sanctions to impose for OpenSky's misconduct. Appx81-87. Regarding VLSI's request to terminate the IPR, the Director explained that "the unique dynamics of this case, coupled with the public interest in evaluating patent challenges with compelling merits," counseled continuing the IPR if "the unpatentability merits were compelling as of the time of institution[.]" Appx84. The Director accordingly remanded for the Board to determine whether OpenSky's petition presented "a compelling, meritorious challenge" based on the institution record. Appx41-42; *see* Appx81-87.

Additionally, the Director ordered OpenSky "to show cause" why it should not "pay compensatory damages to VLSI, including attorney fees." Appx41; *see* Appx87-88. The Director also barred OpenSky and its counsel from "actively participating" in the IPR "unless expressly instructed" to do so by the Board or Director. Appx41; *see* Appx10. The Director subsequently dismissed OpenSky from the proceeding (Appx116-117), but later vacated that decision while continuing to consider what sanctions to impose (Appx128).

3. The Board's and Director's compelling-merits decisions

On remand, the Board determined that the institution record established "a compelling, meritorious challenge" to the '759 patent. Appx91-92. The Board found that the petition's arguments and evidence would plainly lead to an unpatentability determination for both obviousness grounds (i.e., Shaffer/Lint and

Chen/Terrell). Appx93-100. Thus, the Board concluded, "the record prior to institution supports that it was highly likely that Petitioner would prevail" on at least one claim. Appx100.

The Director then reviewed the Board's compelling-merits decision. In December 2022, after considering "the record as it stood before institution" as well as the Board's institution and remand decisions, the Director concluded that "the combination of Chen and Terrell, as presented in the Petition, presents a compelling, meritorious challenge based on the record prior to institution." Appx119-120.[3] The Director therefore affirmed the Board's compelling-merits determination and ordered the Board to continue its unpatentability review. Appx124.

The Director also "admonish[ed] VLSI and its counsel for supporting their arguments with misleading statements of law and fact[.]" Appx117; *see* Appx121-123. As the Director noted, "[t]his [wa]s not the first time VLSI ha[d] made misleading statements of law or fact in an attempt to mislead [the Director] or the Board." Appx117-118 n.2.

4. The Director's sanctions order awarding fees against OpenSky

In February 2023, the Director awarded attorney fees as a sanction against OpenSky. Appx126-141. The Director determined it was appropriate to award fees

[3] The Director did not reach the Shaffer/Lint ground because doing so was unnecessary. Appx119 n.3.

to VLSI for the time spent addressing OpenSky's misconduct during the proceeding (but not for time spent addressing the IPR merits), explaining that the awarded fees "[we]re commensurate with the harm caused by OpenSky's abuse." Appx129; *see* Appx128-138. The Director accordingly authorized VLSI to request a specific amount of fees. Appx138.

5. The Board's final written decision

The Board issued its final written decision in May 2023, finding every challenged claim unpatentable for obviousness. Appx163-206.

Claim construction. The Board construed "request" to have its plain meaning. Appx168-172. In so doing, the Board rejected VLSI's argument seeking to read in "a negative limitation that excludes a signal, e.g., a command or instruction, acted upon without assessment." Appx168-169. The Board explained that the claim language, specification, prosecution history, and extrinsic evidence all "support[] a construction of 'request' that does not require assessing the request before acting in response to the request." Appx172.

Obviousness. The Board then found each challenged claim obvious on two independent grounds.

First, the Board determined that claims 1, 14, and 17 were rendered obvious by Shaffer and Lint and claims 18, 21-22, and 24 by Shaffer, Lint, and Kiriake. Appx175-191. The Board found that Shaffer discloses most claim limitations,

including sending a "request" to change clock frequency, and adopted Petitioners' contentions that Lint provides additional reasons to send the request in response to a "predefined change in performance." Appx175-185; Appx189. VLSI did not dispute that Shaffer discloses the claimed "request" under the Board's claim construction. Appx178. Nor did VLSI challenge any contentions concerning Lint. Appx1381-1405.

Second, the Board determined that claims 1, 14, and 17 were rendered obvious by Chen and Terrell and claims 18, 21-22, and 24 by Chen, Terrell, and Kiriake. Appx191-202. As relevant here, the Board found that skilled artisans would have been motivated to modify Chen's master devices so that they send their "requests" to change clock frequency "in response to a predefined change in performance" as taught by Terrell. Appx191-197. In particular, the Board found that the evidence demonstrated that "the prospect of achieving power savings would have motivated skilled artisans to operate Chen's system at a reduced clock frequency when not required by performance demands." Appx194-195.

The Board further determined that VLSI's purported secondary-considerations evidence (which VLSI does not address on appeal) was insufficient to establish non-obviousness. Appx185-188.

Dr. Jacob's declarations. Lastly, the Board denied VLSI's request to exclude the two Dr. Jacob declarations attached to OpenSky's petition as

"inadmissible hearsay." Appx202-205. The Board explained that its rules permit "'the filing of sworn witness declarations in lieu of live testimony in administrative patent trials.'" Appx204 (citation omitted); *see* 37 C.F.R. §42.51(b)(ii). The Board then found that "Dr. Jacob has made himself available for cross-examination and confirmed that the declarations express his opinions here, in this proceeding" and thus "are no different than the other testimony relied on by the parties, and are not hearsay subject to exclusion." Appx204-205.

6. The Director's order granting VLSI's fee motion

In December 2023, the Director granted VLSI's motion for attorney fees and ordered OpenSky to pay VLSI $413,264.15. Appx209-237. In March 2024, the Director clarified that OpenSky's payment of the sanction is not due until after appeal. Appx3339-3349.

SUMMARY OF ARGUMENT

1. The Board correctly found each challenged claim obvious on two independent grounds.

For the Chen/Terrell ground, substantial evidence supports the Board's factual finding that skilled artisans would have been motivated to combine those references to save power. Substantial evidence also supports the Board's finding that this combination does not contradict Chen's principle of operation. As the Board

explained, VLSI's reading of Chen to require always operating devices at the fastest possible speed is "implausible" in light of the evidence. Appx196.

For the Shaffer/Lint ground, the Board correctly construed "request" to have its plain meaning and to encompass signals that ask, instruct, or command. The Board's construction is supported by the claim language, specification, prosecution history, and how skilled artisans would ordinarily understand the term. By contrast, VLSI's proposed interpretation would improperly read in a negative limitation requiring the claimed system to assess whether to grant or deny each request. VLSI does not dispute that Shaffer discloses the claimed "request" under the Board's construction.

The Board also provided a sufficient written explanation concerning Lint and claims 17-18, 21-22, and 24. The Board made clear that it adopted Petitioners' contentions on those issues because it agreed that Petitioners provided evidence and arguments demonstrating obviousness and VLSI did not dispute those contentions.

2. The Board acted within its discretion in allowing Intel's joinder. VLSI's argument that Intel's IPR petition was "untimely" and not "properly filed" is unreviewable under §314(d). VLSI also misreads the statute, as §315(b) provides that the one-year limit for infringement defendants to file petitions "shall not apply to" joinder requests. And Intel's joinder did not prejudice VLSI: Intel presented the

same prior-art challenges as OpenSky, which the Director found warranted review because the merits were "compelling."

3. The Director's denial of VLSI's request to terminate the IPR due to OpenSky's conduct is not reviewable under §314(d). Nevertheless, the Director was well within her discretion not to impose such a sanction and provided a reasoned explanation for her decision: she sought to balance deterring misconduct with ensuring reliable patent rights, and concluded that termination was unwarranted because OpenSky's petition presented "compelling" unpatentability arguments. Nor did the Director abuse her discretion in rejecting VLSI's hearsay objections at the compelling-merits stage, or by dismissing and then reinstating OpenSky as she considered what sanction to impose for its misconduct. At all stages, the Director acted reasonably, carefully considered the facts, and articulated her rationales.

ARGUMENT

I. THE BOARD'S OBVIOUSNESS DETERMINATIONS SHOULD BE AFFIRMED.

The Board determined that each challenged claim would have been obvious on two independent grounds (i.e., Chen/Terrell and Shaffer/Lint). Appx168-202. As detailed below, the Board's obviousness determinations for both grounds were well-reasoned and supported by substantial evidence. Affirmance as to ***either*** ground requires affirmance of the Board's unpatentability determinations for all challenged claims.

A. Substantial Evidence Supports The Board's Finding Of A Motivation To Combine Chen And Terrell.

The Board correctly determined, based on substantial evidence, that the challenged claims would have been obvious over Chen and Terrell (and Kiriake for some claims). Appx191-202. VLSI does not dispute that Chen and Terrell (and Kiriake) together teach or suggest every claim limitation. For this ground, VLSI challenges (at 64-67) only the Board's factual finding that skilled artisans would have been motivated to combine Chen and Terrell. But as discussed below, substantial evidence supports the Board's motivation-to-combine finding. *See Skky, Inc. v. MindGeek, s.a.r.l.*, 859 F.3d 1014, 1021 (Fed. Cir. 2017) (motivation to combine is factual question reviewed for substantial evidence).

As the Board explained, Chen discloses a system with two or more master devices connected via a bus, where the master devices send "requests" to control logic that dynamically changes the clock speed in response to those requests. Appx191-192 (citing Appx4312(Fig.1); Appx4315(1:6-8, 1:61-62); Appx4316(3:4-22)). Terrell discloses a similar bus system, but introduces a way to adjust clock speed based on performance needs as measured by how busy a device is (e.g., if a device has recently been 50% idle, it might request a clock frequency of half speed). Appx193 (citing Appx4323(¶¶5, 8); Appx4324(¶¶25-27)). Citing the references themselves and expert testimony, the Board found it would have been obvious to modify Chen's master devices, making "only modest changes" (Appx197), so that

they send their requests "in response to a predefined change in their performance" as Terrell teaches. Appx191-197; *see* Appx1040-1049.

Substantial evidence supports the Board's finding that skilled artisans would have been motivated to combine Chen and Terrell in this manner to save power. Appx194-195. As the Board explained, "the record supports a finding that skilled artisans would have understood power savings as an important consideration." Appx194. For instance, Terrell teaches "it is desirable to be able to reduce the frequency of a shared clock to the minimum frequency that allows the processing elements to function correctly while using the least amount of power." Appx194-195 (quoting Appx4323(¶5)). And VLSI's own expert emphasized that "power savings in designing a processor" is "extremely important." Appx194 (quoting Appx6045); *see* Appx6044-6046 (VLSI's expert testifying "power was a key consideration" in "all the processors [he has] been involved with"); *see also* Appx4107-4113(¶¶128, 135-138), Appx5985-5988(¶¶112, 117) (Dr. Jacob discussing power-savings benefit in Chen/Terrell combination). The record thus supports the Board's finding "that the prospect of achieving power savings would have motivated skilled artisans to operate Chen's system at a reduced clock frequency when not required by performance demands." Appx195.

Contrary to VLSI's assertion (at 66-67), the Board's motivation-to-combine finding was not "generic" or "conclusory." Rather, the Board found—and VLSI

does not dispute—that Terrell expressly discloses the goal of saving power. Appx194-195 (citing Appx4323(¶5)). In fact, Terrell teaches it would be "desirable" to reduce power in a system—like Chen's—with "two or more" master devices that "share a common system clock." Appx4323(¶¶6-8). Adding further support, the Board also "credit[ed] Dr. Jacob's testimony" that skilled artisans would have been motivated to conserve power while still meeting performance requirements in the Chen/Terrell combination. Appx195 (citing Appx5985(¶112); Appx5987-5988(¶117)). Nothing more was required. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797-799 (Fed. Cir. 2021) (reversing Board's rejection of "energy-efficiency rationale" as "generic"); *Nike, Inc. v. Adidas AG*, 812 F.3d 1326, 1337 (Fed. Cir. 2016) (affirming obviousness where Board identified motivation of "minimi[zing] waste"); *see also Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) ("'[U]niversal' motivations known in a particular field to improve technology provide 'a motivation to combine prior art references even absent any hint of suggestion in the references themselves.'" (citation omitted)).

Substantial evidence also supports the Board's finding that the Chen/Terrell combination would not "defeat[] Chen's intended purpose." Appx196. Although VLSI insists (at 64-65) that Chen requires operating at the maximum possible speed at all times, the Board correctly rejected that argument as "implausible" in view of the evidence. Appx196. As the Board pointed out, Chen itself "discloses operating

at lower speeds for certain circumstances." Appx194. For example, Chen states that "I/O devices which normally operate at 66 M[H]z can be operated at 50 M[H]z." Appx4316(3:42-43) (cited at Appx196). Chen also recognizes that "low frequency operation [may be] necessary … depend[ing] on the type of transaction." Appx4316(3:25-29). And Chen discloses embodiments that use an increased frequency for "only memory read and write operations," while using a lower frequency for "[a]ll other operations." Appx4316(4:24-36) (cited at Appx194); *see* Appx4317(5:21-24) ("The remaining devices on the bus, which are not involved in the current high frequency data transfer transaction, will continue to receive the lower frequency clock.").

Moreover, Chen teaches that operating some devices "at a lower frequency" may "minimize the cost and complexity of providing high frequency operation." Appx4316(4:28-33). Skilled artisans also would have understood that operating devices at less than the fastest possible speeds, as Chen expressly describes, would reduce power consumption. Appx4106-4107(¶127) (Dr. Jacob explaining "Chen makes sure not to increase the operating frequencies of any devices or busses not directly involved in a particular transaction, to ensure that no excess power is dissipated needlessly"); Appx5997(¶131) (Dr. Jacob explaining "Chen is concerned with efficiency in some significant instances, even to the point where efficiency takes precedence over performance"); Appx5991-5997(¶¶122-131). Substantial

evidence thus supports the Board's finding that Chen's "principle of operation" does not require always using the fastest speed possible. *See In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (affirming unpatentability where substantial evidence supported "Board's determination that eliminating" certain components of prior-art reference "would not destroy its principle of operation"); *University of Md. Biotech. Inst. v. Presens Precision Sensing GmbH*, 711 F. App'x 1007, 1010-1011 (Fed. Cir. 2017) (affirming unpatentability where substantial evidence supported Board's finding that combining references would not require changing prior art's "basic principles").

In any event, substantial evidence supports the Board's finding that skilled artisans would have understood that it was preferable to save power at times when more performance was not needed rather than always operating at the fastest speed. Appx196. As the Board noted, Terrell recognizes that systems may spend time in the idle state (i.e., not active). Appx4325(¶54) (cited at Appx196). Skilled artisans would have considered it "implausible" to operate a system at maximum speed, which means supplying the additional power necessary to do so, even during idle states. *See id.* They would have understood it to be more practical and beneficial overall, as in the Chen/Terrell combination, for bus speed to be "reduced when performance needs allow and then increased to the limit of a device's capabilities when required." Appx196; *see* Appx4110-4112(¶¶134-136); Appx5985-

5988(¶¶112, 117). Because that approach still "satisf[ies] a performance demand," the Board properly found "that Chen's 'principle of operation and stated goal' are preserved by the asserted combination." Appx196.

The Board also correctly rejected VLSI's contention (at 65-66) that Chen and Terrell could not be combined because they supposedly have "opposite goals." Appx195. Based on the record evidence, the Board found that the Chen/Terrell system "would have been able to operate at reduced frequency (conserving power) in low-activity times and increased frequency when the system required higher performance." *Id.* (citing Appx5987-5988(¶117)). The Board explained that this combination "is consistent with Chen's teachings of increasing frequency for certain operations, and also consistent with Terrell's teachings of reducing frequency when possible." *Id.*; *see* Appx4315(1:6-8, 1:61-62, 2:1-6) (cited at Appx192); Appx4323(¶5) (cited at Appx193). The Board further credited Dr. Jacob's testimony that the combination would have balanced "the inherent trade-off between highest performance at the highest cost, and lower (but perhaps still acceptable) performance at a lower cost." Appx195 (quoting Appx5985(¶112)); *see* Appx4102-4117(¶¶122-145), Appx5985-5988(¶¶112-117) (Dr. Jacob explaining how Chen's and Terrell's teachings are "complementary").

In sum, substantial evidence supports the Board's motivation-to-combine finding. VLSI's mere disagreement with the Board's factual findings provides no

basis to disturb the Board's well-reasoned decision. The Board's obviousness determinations based on Chen and Terrell (and Kiriake) should be affirmed. *See Voice Tech Corp. v. Unified Patents, LLC*, 110 F.4th 1331, 1344 (Fed. Cir. 2024) (affirming obviousness where substantial evidence supported Board's motivation-to-combine finding); *Skky*, 859 F.3d at 1022 (same).

B. As An Independent Ground, The Board Also Correctly Found The Claims Obvious Over Shaffer And Lint.

The Board separately determined that the challenged claims would have been obvious over Shaffer and Lint (and Kiriake). Appx175-191. As discussed below, the Board's finding that Shaffer discloses the claimed "request" applied a correct interpretation of that term. And the Board provided a sufficient written explanation for its findings relating to Lint, which VLSI never disputed. The Board's obviousness determinations therefore can—and should—be affirmed on this additional ground.

1. The Board correctly construed the term "request" in finding obviousness over Shaffer.

The Board correctly interpreted "request" to have its plain and ordinary meaning. Appx168-172. The Board did not, as VLSI inaccurately claims (at 55), construe "'request' to mean command." Rather, the Board recognized that the plain meaning of "request" is broad enough to encompass a signal that asks, instructs, or commands. *Id.* In so doing, the Board rejected VLSI's attempt to read in "a negative

limitation that excludes a signal, e.g., a command or instruction, acted upon without assessment." Appx168-169. The Board's construction is supported by intrinsic and extrinsic evidence, and should be affirmed.

Each challenged claim recites a "request" sent from a first master device "in response to a predefined change in performance." Appx251-252(8:1-5, 8:52-55, 9:30-34). The claims state that, "in response to receiving the request," a clock frequency is provided to control the clock frequency of a second master device and the bus. Appx251-252(8:9-15, 8:62-9-4, 9:26-30, 9:34-37). The claims nowhere specify "how a request is processed" or suggest that the claimed system or method must be able to decide whether to grant or deny each request. Appx170. As the Board put it, the claim language simply "does not include a limitation that requires assessing whether to act on an incoming request." Appx169-170 & n.7.

Unable to point to anything else in the claim language, VLSI contends (at 55-56) that the word "request" ***alone*** means that the request "may or may not be granted." *See* VLSI Br. 62 (seeking construction of "request" that means "an ask that can be granted or denied"). But as the Board observed, VLSI's argument actually addresses the capability of the system and how it responds to a request rather than the nature of the request itself. Appx169. That is, even if a "request" in the abstract could be granted or denied, nothing in the patent precludes the claimed system from being designed to grant all requests. Indeed, the challenged claims

describe ***only*** what happens when a request is granted (i.e., providing a clock frequency to the second master device and bus); they nowhere address denying a request. Appx251-252(8:9-15, 8:62-9-4, 9:26-30, 9:34-37).

The Board also correctly determined that VLSI's interpretation of "request" is narrower than "typical usage of the term in the relevant art." Appx172. As the Board found, prior art "uses the terms 'command,' 'instruction,' and 'request' synonymously." *Id.* (citing Appx5931-5933(¶¶29-32)); *see* Appx2552(18:12-25); Appx2554(20:8-17); Appx2555(21:2-5). Lint makes this crystal clear, as it uses each of those terms interchangeably. Appx4343(3:16-17) ("OS makes a ***request*** to set the P-state"); Appx4343(4:40-44) ("***request*** made by the OS to enter a P-state"); Appx4344(5:47-49) ("OS specifies a first P-state via SET_PSTATE ***command***"); Appx4346(9:16-20) ("OS communicates with the processor to ***instruct*** … the new P-state").[4, 5] VLSI has no response to this evidence, other than to call it "irrelevant" (at 61). But as the Board properly found, the ordinary usage in the relevant field indicates "that 'request' did not carry the special meaning for which [VLSI] now argues." Appx172; *see Sisvel Int'l S.A. v. Sierra Wireless, Inc.*, 81 F.4th 1231, 1236-1237 (Fed. Cir. 2023) (noting general rule that claim terms are given their ordinary meaning, and affirming Board's rejection of patentee's narrower interpretation);

[4] "P-state" corresponds to frequency. Appx6109-6110(1062:25-1063:3).

[5] Emphasis is added unless otherwise noted.

Polaris Innovations Ltd. v. Brent, 48 F.4th 1365, 1376-1378 (Fed. Cir. 2022) (same).[6]

Consistent with the claim language and ordinary usage of "request," "[n]othing in the specification describes a request that itself requires independent assessment." Appx170. VLSI nonetheless contends (at 56-60) that the specification "uniformly" describes a system in which the clock controller may decide whether to grant or deny a request. But claim 1 does not even recite a "clock controller." Appx251(7:66-8:15). Moreover, the Board correctly found that VLSI's cited examples from the specification are described merely as "embodiments." Appx170; *see* Appx249-250(4:58, 5:12, 5:49) ("In a particular embodiment …."); Appx248-250(1:65, 2:5, 2:10-11, 5:18-19) (similar). In fact, most of VLSI's examples disclose "alternative embodiments" for "setting [or monitoring] bus speed control flags"—a feature that is not recited in any of the challenged claims. Appx248(1:30-42) (describing Figs. 2-6); Appx250(6:1-2) ("alternative method of setting bus speed control flags"); *see* Appx250-251(5:47-48, 6:26-27, 6:49-50, 7:7-8) (similar). As the Board explained, the specification's disclosure of "alternative embodiments"

[6] How skilled artisans understood "request" is more informative than how the word was used in *Beauty and the Beast* (VLSI Br. 56 n.12). Even so, the teacups and candlesticks recognized during "Be Our Guest" that a command is a type of "request." *See* https://www.youtube.com/watch?v=afzmwAKUppU (2:43-2:44) ("Our command is your request!").

does not "establish[] that the claimed 'request' mandates deciding whether to act on the request." Appx170; *see Sisvel*, 81 F.4th at 1236 (rejecting construction that would "improperly limit the claims to embodiments").

In any event, the Board correctly found that the specification discloses "at least one example … consistent with a system that makes no independent assessment of a request." Appx170-171. That example provides that "[t]he clock controller can output a variable clock frequency that varies in response to one or more inputs from the at least one master device." Appx248(2:38-40). In other words, the example—like the challenged claims—only addresses changing clock frequency in response to granting a request and says nothing about denying a request. Simply put, the specification does not support reading VLSI's negative limitation (i.e., excluding a system that grants all "requests" without an intervening assessment) into the broader claim language. *See Uniloc 2017 LLC v. Sling TV, L.L.C.*, 2024 WL 4038034, at *2 (Fed. Cir. Sept. 4, 2024) ("[W]e decline to import a negative limitation into the claim that cannot be found in the claim language itself."); *Ethicon LLC v. Intuitive Surgical, Inc.*, 847 F. App'x 901, 907-908 (Fed. Cir. 2021) ("[T]he claim language and specification reveal[] no intent to confer on the claim language the meaning imparted by Ethicon's proffered negative limitation."); *Linear Tech. Corp. v. ITC*, 566 F.3d 1049, 1060 (Fed. Cir. 2009) (declining to add negative limitation to claim where "there is no basis in the patent specification").

Finally, the Board correctly found that "[t]he prosecution history further supports an understanding of the claimed 'request' as not requiring assessment before acting." Appx171. The applicant initially proposed a dependent claim that recited "determining whether to enable the request to increase the clock frequency of the bus." Appx4470 (original claim 2). During prosecution, however, the applicant "intentionally cancelled" that claim and did not add the "determining" limitation to any new or amended claims. Appx171; *see* Appx4655-4664 (showing cancelled and new claims proposed to overcome examiner's prior-art rejections). That is, "the applicant understood the possibility of claiming the distinction now sought [by VLSI], but decided not to limit the claims in that manner." Appx171-172. Although VLSI tries (at 61) to downplay the prosecution history as "murky," it is directly on point and provides a strong indication that the challenged claims do not include VLSI's proposed limitation. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 909, 913 (2004) (reversing narrower claim construction requiring a "pressure jacket" where, during prosecution, "the applicants replaced claims that had included references to a pressure jacket with a new set of claims, many of which did not include the pressure jacket limitation").

* * *

In determining that the challenged claims would have been obvious over Shaffer and Lint (and Kiriake), the Board found that Shaffer discloses the claimed

"request." Appx178 (citing Appx4331(3:8-22, 4:50-54); Appx1023-1024); *see* Appx175-177; Appx4328(Fig.1); Appx4331-4332(3:53-56, 5:5-20); Appx4205-4213(¶¶235, 241-242). VLSI does not dispute that, if this Court agrees with the Board's construction, it should also affirm the Board's finding that Shaffer teaches the "request" limitations. *See* VLSI Br. 62.

The record further demonstrates that Shaffer discloses the claimed "request" even under VLSI's proposed construction. VLSI and its expert admitted during the IPR that Shaffer discloses "request[s]." *See* Appx8030-8031(¶45) (VLSI's expert Dr. Conte stating "Shaffer's multiprocessor system teaches at most a single master device—CPU 40 [*sic*]—***requesting*** a speed change."); Appx1125-1126 (VLSI repeating same). Petitioners also showed that Shaffer's system may "grant" or "ignore" individual "request[s]" to change clock speed under certain circumstances. Appx5933-5935(¶¶33-34); *see* Appx2552-2555(18:18-21:1). This Court may therefore affirm the Board's unpatentability findings based on Shaffer even under VLSI's proposed construction. *See Micrografx, LLC v. Google Inc.*, 672 F. App'x 988, 990-992 (Fed. Cir. 2016) (affirming Board's unpatentability determination where Board's broader claim construction was harmless error).[7]

[7] At minimum, however, the Court should remand for the Board to make findings on whether Shaffer teaches the claimed "request" under any new construction. *See Seabed Geosolutions (US) Inc. v. Magseis FF LCC*, 8 F.4th 1285, 1290 (Fed. Cir. 2021) (remanding for further proceedings after overturning Board's construction).

2. The Board properly relied on Lint.

VLSI next contends (at 62-64) that "[t]he obviousness determinations based on Schaffer/Lint fail because the [Board] failed to make any reasoned findings about Lint." VLSI's argument is a red herring: VLSI did not contest ***any*** issues relating to Lint during the IPR (Appx1381-1405), and it similarly identifies no substantive errors concerning Lint on appeal. VLSI instead resorts to criticizing the Board's written decision, but the Board provided a sufficient explanation to support its obviousness determinations. Appx177.

More specifically, the Board acknowledged that Petitioners relied on Shaffer as teaching most limitations for claim 1 and on Lint as teaching that a "predefined change in performance is due to loading of the first master device as measured within a predefined time interval." Appx177 (citing Appx1022-1031). The Board then explained that Petitioners relied on Lint "as an alternative to Shaffer's teachings" and stated what the proposed combination was—with supporting citations to both the petition and Lint. Appx177 ("Petitioner reasons … that Shaffer describes a 'CPU utilization percentage,' [and] that Lint discloses a way of calculating the utilization percentage that would allow Shaffer's system 'to better interface with processor chips featuring hardware coordination of [performance]-states' by saving power[.]" (citing Appx1027-1030; Appx4342-4343(3:1-7, 2:33)); *see* Appx4342(2:31-33) (Lint teaching "provid[ing] for the best performance while saving power").

After analyzing every disputed issue concerning the Shaffer/Lint combination in detail (Appx175-188), the Board made clear it had "considered the full record, including evidence and arguments presented by Petitioner and [VLSI] on whether Shaffer and Lint teach or suggest claim 1's limitations" and whether skilled artisans "would have combined Shaffer and Lint as asserted." Appx189; *see* Appx189-190 (same for claim 14). The Board then "conclude[d] that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Shaffer and Lint." Appx189; *see* Appx190 (same for claim 14). For the reasons explained below, that analysis—which cited the relevant portions of the petition containing the arguments and evidence supporting Petitioners' contentions on issues that VLSI did not contest—was more than sufficient to support the Board's obviousness determinations. *Infra* pp. 41-43.

C. The Board Provided Sufficient Reasoning For Claims 17-18, 21-22, And 24.

Lastly, VLSI challenges (at 68) the sufficiency of the Board's written decision for claims 17-18, 21-22, and 24. For the limitations added by those claims, the Board adopted Petitioners' contentions because Petitioners provided evidence and arguments demonstrating obviousness and VLSI did not dispute those contentions. Appx191; Appx202. Contrary to VLSI's suggestion, the Board was not obligated to address arguments VLSI never raised. *See Novartis AG v. Torrent Pharms. Ltd.*, 853 F.3d 1316, 1327-1328 (Fed. Cir. 2017) (it would be inappropriate "to find fault

in the Board's arguably limited treatment of [certain] arguments" where Board's treatment was "commensurate with" patentee's presentation).

Regardless, the Board's analysis for claims 17-18, 21-22, and 24 was sufficient. The Board unambiguously determined that Petitioners carried their burden of proving unpatentability. Appx191, Appx202 ("We … determine that Petitioner has shown [claims 17, 18, 21, 22, and 24] would have been obvious[.]"). For each of those claims, the Board noted that Petitioners identified where the prior-art references "teach or suggest the additional limitations" and cited the specific pages from the petition for the contentions. Appx191 (citing Appx1033; Appx1034-1038; Appx1038-1039); *see* Appx202 (citing Appx1052-1053; Appx1054-1059; Appx1059-1060). The Board then pointed out that VLSI "d[id] not dispute" any contentions beyond claims 1 and 14, and made clear it had independently "reviewed the record, including [VLSI's] asserted objective indicia of nonobviousness." Appx191; *see* Appx202. Only then did the Board conclude that claims 17-18, 21-22, and 24 "would have been obvious." Appx191; Appx202.

This Court has affirmed unpatentability determinations based on similar Board decisions. For example, in *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 904-906 (Fed. Cir. 2018), this Court rejected the patentee's argument that "the Board failed to adequately explain its rationale for finding [several claims] unpatentable, and instead improperly adopted [the petitioner's] arguments without explanation."

The Court explained that—like here—the Board's decision "[wa]s commensurate with [the patentee's] arguments" and cited "the relevant portions of [the petitioner's] briefing that explain how the prior art discloses the relevant claim limitations." *Id.* at 905. "In this context," the Court concluded, "the Board's [obviousness] analysis is readily discernible and sufficient[.]" *Id.*

VLSI's cited cases do not require more. *See* Br. 62-64, 68 (citing, e.g., *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1047 (Fed. Cir. 2017)). This Court can readily discern the Board's reasons concerning the undisputed claim limitations and combinations: it was the evidence and argument presented on the petition's cited pages. Appx191 (citing Appx1033-1039); Appx202 (citing Appx1052-1060); *see Intel Corp. v. Alacritech, Inc.*, 817 F. App'x 1014, 1018 (Fed. Cir. 2020) ("[W]e can discern that the Board found the cited passages from [the] petition persuasive …. We therefore decline to overturn the Board's [obviousness] decision."); *Ignite USA, LLC v. CamelBak Prods., LLC*, 709 F. App'x 1010, 1015 (Fed. Cir. 2017) (finding analysis sufficient because this Court "c[ould] discern" that the Board found the petitioner's arguments and supporting evidence more persuasive than the patentee's). The Board's unpatentability determinations for all challenged claims should be affirmed.

II. THE BOARD ACTED WITHIN ITS DISCRETION IN JOINING INTEL.

Section 315(c) allows the Board to discretionarily "join as a party to [an instituted IPR] any person who properly files a petition under section 311[.]" 35 U.S.C. §315(c). Intel's petition satisfied §311's requirements: Intel is not the patentee; the petition asserted obviousness based on prior-art patents and printed publications; and the petition was filed more than nine months after the '759 patent issued. *Id.* §311(a)-(c). Intel's joinder request also was timely because it was filed within "one month after" institution of OpenSky's IPR. 37 C.F.R. §42.122(b). The Board was accordingly entitled to join Intel. Appx1-21.

A. Intel's Joinder Was Not Time-Barred.

Section 315(b) does not prohibit Intel's joinder. Its first sentence provides that an IPR "may not be instituted if the petition requesting the proceeding is filed more than 1 year after … the petitioner … is served with a complaint alleging infringement[.]" 35 U.S.C. §315(b). Its second sentence, however, creates an exception:

> The time limitation set forth in the preceding sentence shall ***not*** apply to a request for joinder under subsection (c).

Id. The one-year time bar is thus inapplicable where, as here, a party seeks to join an already-instituted IPR.

The Supreme Court and this Court have acknowledged this plain-text interpretation, albeit not directly as a case holding. In *Thryv, Inc. v. Click-to-Call*

Technologies, LP, 590 U.S. 45, 55 (2020), the Supreme Court explained that "failure to satisfy §315(b)" does not "prevent [a petitioner] from participating on the merits" in an IPR because an otherwise time-barred party "can join a proceeding initiated by another petitioner." As the Court observed, the exception to the one-year bar for joinder petitions "confirm[s] that Congress prioritized patentability over §315(b)'s timeliness requirement." *Id.*; *see VirnetX Inc. v. Mangrove Partners Master Fund, Ltd.*, 144 S. Ct. 1001 (Feb. 20, 2024) (Mem.) (denying certiorari on same §315 question VLSI raises).

Similarly, in *Network-1 Technologies, Inc. v. Hewlett-Packard Co.*, 981 F.3d 1015, 1027 (Fed. Cir. 2020), this Court acknowledged that "HP was permitted to join the Avaya IPR 'as a party' even though HP was time-barred under §315(b) from bringing its own petition." And in *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1333 (Fed. Cir. 2020), the Court recognized §315(b)'s "specific exception to the time bar" for joinder requests. *See also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1020 (Fed. Cir. 2017) (Dyk, J., joined by Wallach, J., concurring) (§315(b)'s exception "appl[ies] where time-barred Party A seeks to join an existing IPR timely commenced by Party B" when no new patentability issues introduced).

The USPTO likewise properly treats §315(b)'s time bar as inapplicable "when the petition is accompanied by a request for joinder." 37 C.F.R. §42.122(b); *see*

Proppant Express Investments, LLC v. Oren Techs., LLC, IPR2018-00914, Paper 38 at 17-18 (P.T.A.B. Mar. 13, 2019); U.S. Br. 4, *VirnetX Inc. v. Mangrove Partners Master Fund, Ltd.*, No. 23-315 (U.S. Dec. 27, 2023) (Solicitor General stating "[t]he USPTO has understood" §315 this way).

B. VLSI's Argument Misreads §315 And Is Unreviewable.

VLSI's argument (at 50-55) that Intel's joinder was barred because its petition was not "properly file[d]" misreads the statute.[8] Section 315(c) refers to petitions "properly file[d] … ***under section 311***," which Intel's petition was. *Supra* p. 44. Section 311's "[f]iling [d]eadline" requires filing a petition at least nine months after the patent's issuance and after termination of any post-grant review. 35 U.S.C. §311(c). It makes no reference to §315(b)'s one-year limit.

The legislative history does not support a different understanding. Senator Kyl's statements snipped by VLSI (at 51) nowhere mentioned §315(b)'s time bar, and his reference to "time deadlines for filing petitions" likely meant the "[f]iling [d]eadline" that became §311(c). *See* S. 3600, 110th Cong. §5(c) (2008); 154 Cong. Rec. S9982, S9988 (daily ed. Sept. 27, 2008) (Senator Kyl explaining "there [was] no time deadline that applies to [IPR] petitions … other than that they not be filed before [post-grant reviews] are concluded"). Regardless, one legislator's equivocal

[8] VLSI never made this argument to the Board. Appx14113-14133; Appx146 (Board stating VLSI's argument against joinder "is not based on statutory prohibitions" but on "discretionary denial").

words cannot override §315's text. *State Farm Fire & Cas. Co. v. United States ex rel. Rigsby*, 580 U.S. 26, 36-37 (2016).

VLSI points (at 51-53) to the difference between IPR "petition[s]" and "request[s] for joinder," but that only underscores the flaws in VLSI's interpretation. The time limitation in §315(b)'s first sentence applies to IPR petitions, not joinder requests. It makes sense that the exception in §315(b)'s second sentence likewise applies to petitions; otherwise, it would not exempt anything. Indeed, if VLSI were correct that a party may seek joinder only if it files a petition within the one-year limit, then §315(b)'s second sentence—the time-bar exception—would have no meaning because the first sentence's time bar effectively ***would*** "apply to a request for joinder under subsection (c)." *See ClearCorrect Operating, LLC v. ITC*, 810 F.3d 1283, 1294 (Fed. Cir. 2015) (statute should be interpreted so "no clause, sentence, or word shall be superfluous").

VLSI's distinction between "petition[s]" and "request[s] for joinder" also highlights another problem with VLSI's argument: this Court lacks jurisdiction to consider it. While joinder decisions are generally reviewable, *Facebook*, 973 F.3d at 1332, VLSI's argument—that Intel's petition was not "properly filed" because it was untimely under §315(b)—clearly is not. *Thryv*, 590 U.S. at 48, 52-60 (Board's "application of §315(b)'s time limit" is "closely related" to institution decision and therefore "nonappealable"); 35 U.S.C. §314(d) (institution decisions

"nonappealable"). Because §314(d) means this Court must accept the Board's decision to institute Intel's "petition" as correct and VLSI concedes (at 52) that §315(b) exempts Intel's "request for joinder" from the one-year limitation, there is nothing left of VLSI's §315 argument to review.

C. Intel's Joinder Did Not Prejudice VLSI.

VLSI's §315 challenge independently fails because VLSI has not shown prejudice. 5 U.S.C. §706(2)(C) (reviewing court shall consider "prejudicial error" when interpreting statute). VLSI's complaint (at 53-55) that Intel's IPR participation was itself prejudicial is unsupported. As the Board found, Intel raised "challenges and evidence nearly identical to" OpenSky (Appx4-5) and added no "significant issues" (Appx15). Intel's joinder therefore did not alter the Board's mandate to determine whether the same prior art invalidated the same claims in the same proceeding. *See VirnetX Inc. v. Mangrove Partners Master Fund, Ltd.*, 778 F. App'x 897, 901-902 (Fed. Cir. 2019) (patentee failed to show prejudice from otherwise time-barred party's joinder because, among other reasons, the joinder petition "brought the same challenges" as already-instituted petition).

While VLSI asserts (at 54) that "Intel used its joinder to inject new evidence and arguments" and to "successfully oppose[] VLSI's request for rehearing of the [Board's] compelling-merits decision," this Court rejected a similar argument when it found no prejudice in *VirnetX*. *See* VirnetX Reply Brief at 26-27, No. 17-1368,

ECF 69 (Fed. Cir. June 19, 2018) (patentee arguing that joined party "had taken over Appellees' communications, expert depositions, and oral hearing" and submitted "additional evidence"). Regardless, VLSI ignores that the Board and Director determined that OpenSky's petition presented a "compelling, meritorious challenge" based on the "record before institution"—i.e., ***before*** Intel's joinder. Appx94-100; Appx119-123.

VLSI's speculation (at 54) that the IPR could have ended absent Intel's joinder similarly fails to demonstrate prejudice. Although the Director dismissed OpenSky (Appx116-117), she reconsidered that decision and "restore[d] OpenSky as a petitioner" soon thereafter (Appx128). Moreover, the Director did not deny VLSI's termination request "*because Intel was a party*" (VLSI Br. 54 (emphasis original)). She declined to terminate the IPR because of "the public interest in evaluating patent challenges with compelling merits." Appx84; *see infra* pp. 55-56.

In any case, Intel's joinder did not affect the Board's final written decision. Even if Intel had not been joined, the Board still would have reviewed OpenSky's petition (and could have done so even if no petitioners remained, 35 U.S.C. §317(a)). In short, VLSI has shown no prejudice from the Board making unpatentability determinations it would have made regardless of its joinder decision. *See Pfizer Inc. v. Sanofi Pasteur Inc.*, 94 F.4th 1341, 1354 (Fed. Cir. 2024) ("harmless" procedural

violations "cannot serve as a basis to reverse or vacate the Board's [unpatentability] decisions").

III. THE DIRECTOR ACTED WITHIN HER DISCRETION AND COMPLIED WITH THE APA DURING THE REVIEW PROCEEDINGS.

A. If Reached, The Director's Decision Not To Terminate The IPR Should Be Affirmed.

The Director was well within her discretion not to terminate the IPR based on OpenSky's conduct. Although VLSI would prefer a different outcome, this Court should not substitute its judgment for the Director's on this highly fact-specific, discretionary issue. *Genentech, Inc. v. ITC*, 122 F.3d 1409, 1423 (Fed. Cir. 1997) ("[D]ismissal is universally recognized as a sanction of last resort[.]"); *Abrutyn v. Giovenniello*, 15 F.3d 1048, 1053 (Fed. Cir. 1994) (severe sanctions like termination "should be used as 'a weapon of last … resort'").

1. The Director's non-termination decision is unreviewable.

After VLSI sought rehearing following institution, the Director initiated proceedings to "review … the Board's [i]nstitution [d]ecision." Appx1449. As part of that process, the Director asked how she should address VLSI's abuse-of-process allegations against OpenSky. Appx30.

VLSI's response urged the Director to "repudiate the institution" of the IPR "by terminating [the IPR] and vacating the institution and joinder decisions." Appx1790. According to VLSI, the IPR "never should have been instituted."

Appx1788; *e.g.*, Appx1769 ("[T]his IPR should be terminated and the underlying institution and joinder decisions should be vacated."); Appx1778-1779 ("This IPR should be terminated and voided *ab initio*."); Appx1781 ("[I]nstitution decisions premised on abusive petitions should be vacated[.]"); Appx2132-2133 ("This case should be terminated and voided *ab initio*.").

In considering VLSI's termination request, the Director remanded the institution decision to the Board to evaluate "whether the record before the Board prior to institution indicates that the [p]etition presents a compelling, meritorious challenge." Appx85-86. "Consistent with the ordinary course of institution," the Director did "not authorize the parties to provide any additional briefing or argument" on this issue. Appx87. The Director instructed that "the Board shall move forward with the proceeding" only if a compelling-merits "challenge was made prior to institution[.]" *Id.*

On remand of the institution decision, the Board determined based on "the record prior to institution … that the [p]etition present[ed] a compelling, meritorious challenge." Appx92; *see* Appx100. The Director then "reviewed the record as it stood before institution" and agreed with the Board that the petition "present[ed] a compelling, meritorious challenge[.]" Appx119-120; *see* Appx124. The Director accordingly denied VLSI's termination request and instructed the Board to continue its unpatentability review. Appx124.

As this procedural history demonstrates, the Director's decision declining to terminate the IPR based on the petition's compelling merits was a review of institution. It is therefore "final and nonappealable." 35 U.S.C. §314(d); *see Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 274 (2016) (§314(d) "preclud[es] review" of institution decisions); *CyWee Grp. v. Google LLC*, 847 F. App'x 910, 912 (Fed. Cir. 2021) (motion to terminate was effectively "request for the Board to reconsider its institution decision," which was "nonappealable"), *mandate recalled on other grounds*, 2021 WL 9979071 (Fed. Cir. Sept. 23, 2021).

VLSI's attempts (at 48-49) to distinguish the Director's non-termination decision from her review of institution all fail. Even though the Director separately considered additional sanctions issues (such as attorney fees), the Director made clear that her consideration of VLSI's request to terminate the proceeding due to an alleged abuse of process by OpenSky was part of her review of institution. *See* Appx127 (Director describing October 2022 decision as "decision on Director review of the institution decision"); Appx136 ("[T]he Director review process … is an exercise of the Director's unilateral authority over the institution phase[.]"); Appx137 ("[T]he Director review process was initiated to examine OpenSky's misconduct and determine whether to reverse the institution decision."). Nor was there any reason the Director could not consider OpenSky's post-institution conduct in deciding whether to revisit the institution decision—that was, after all, what VLSI

asked her to do. When it came to re-evaluating the merits of the institution decision, however, the Director allowed consideration of only ***pre-institution*** evidence. *Supra* p. 51. And it was entirely reasonable (and, in fact, beneficial to VLSI) for the Director to apply the higher "compelling-merits" standard when deciding whether to vacate the institution decision as compared to the "reasonable likelihood" standard required to grant institution in the first instance. *Infra* pp. 56-57.

VLSI appears to concede (at 49 n.9) that §314(d) "bars review" of the Director's denial of its request to "vacate" the institution decision. VLSI nevertheless claims (at 47-49) that the Director's denial of its request to "terminate" the IPR is separately reviewable. It is not. VLSI's requests to terminate the IPR (and void it *ab initio*) and to vacate the institution decision were one and the same. Appx1769; Appx1788; Appx1790-1792; Appx2133; Appx2152-2153; *supra* pp. 50-53. However VLSI tries to slice it, the Director's non-termination decision is unreviewable. *See Atlanta Gas Light Co. v. Bennett Regulator Guards, Inc.*, 33 F.4th 1348, 1352-1353 (Fed. Cir. 2022) (Board decision regarding IPR termination unreviewable because it "was based in part" on review of institution-related time-bar issue).

2. The Director did not abuse her discretion in declining to terminate the IPR.

Sanctions decisions fall squarely within the Director's discretion. *Apple Inc. v. Voip-Pal.com, Inc.*, 976 F.3d 1316, 1322 (Fed. Cir. 2020). The Director "may"

sanction a party for "misconduct" including "[f]ailure to comply with an applicable rule or order," "[m]isrepresentation of a fact," or "[a]buse of process." 37 C.F.R. §42.12(a). The USPTO's regulations provide a non-exhaustive list of possible sanctions, such as "holding facts to have been established," "compensatory expenses, including attorney fees," and "[j]udgment in the trial or dismissal of the petition." *Id.* §42.12(b).

Other regulations impose "a duty of candor and good faith." 37 C.F.R. §42.11(a). Practitioners must certify that submitted papers are truthful and not being used for improper purposes. *Id.* §§11.18(b), 42.11(b)-(c). If a practitioner fails to meet these obligations, the Director may impose "appropriate" sanctions. *Id.* §§11.18(c)-(d), 42.11(d)(1). Any sanction should be "limited to what suffices to deter repetition of the conduct or comparable conduct by others." *Id.* §42.11(d)(4).

Under this framework, the Director clearly did not abuse her discretion in denying VLSI's request to terminate the IPR. The Director took seriously VLSI's allegations that OpenSky abused the IPR process. She ordered briefing, document discovery, and interrogatory responses. Appx30-35. She encouraged *amicus* participation, recognizing the "importance to the [USPTO], the [U.S.] innovation economy, and the patent community." Appx30-31. And she provided detailed opinions at each step as she carefully considered the arguments, evidence, and policy objectives. *E.g.*, Appx38-88; Appx103-112; Appx2653-2659; Appx115-124. VLSI

glosses over much of this process, but it demonstrates how meticulous the Director was.

The Director also provided a well-reasoned explanation for why she did not terminate the IPR. She acknowledged the public interest "in discouraging conduct that is abusive or otherwise thwarts Congress's goals in passing the AIA and the [USPTO's] goals[.]" Appx83. At the same time, she recognized the importance of reliable patent rights and weeding out unpatentable claims to promote and protect innovation. *Id.*; *see* Appx2656 ("[T]he USPTO's primary mission is to issue and maintain robust and reliable patent rights…. The [AIA] advances that goal when the Board upholds patents as well as when it removes patent claims that are 'of questionable validity.'"). Seeking to balance these considerations, the Director explained that "the unique dynamics of this case, coupled with the public interest in evaluating patent challenges with compelling merits, counsel[ed]" that the IPR should continue if "the unpatentability merits were compelling" at institution. Appx84-85; *see* Appx41-42; Appx106-107; Appx2656-2658.

The Director then remanded for the Board to determine whether "compelling merits" of unpatentability existed at the time of institution. Appx86. The Board analyzed the institution record and found that OpenSky's petition met that heightened standard. Appx92-100. Upon review of that remand decision, the Director likewise determined that the petition presented compelling merits of

unpatentability. Appx119-123. Given that determination, the Director appropriately allowed the IPR to continue.

3. The Director appropriately applied the "compelling-merits" standard.

In challenging the Director's denial of its request to terminate the IPR, VLSI takes aim (at 32-34) at the Director's decision to apply the "compelling-merits" standard. But as the Director explained, she has broad discretion to fashion a suitable remedy for abuse of process and, in her careful estimation, "[p]redicating dismissal on the application of the compelling-merits standard best serves the competing interests here." Appx84-85; *see* Appx81-82; Appx106-107; Appx2656-2658.

VLSI ignores the Director's justification and criticizes her (at 32-34) for borrowing the "compelling-merits" standard from a June 2022 memorandum addressing discretionary institution denials under *Fintiv* (Appx7368-7376). But like *Fintiv*, the Director was reviewing the Board's institution decision and deemed it appropriate to hold the petitioner to a heightened standard ("compelling merits" versus "reasonable likelihood" of prevailing) in determining whether to proceed with the IPR. Appx84-87. It therefore made good sense to point to the *Fintiv* memorandum in explaining how she would evaluate the unpatentability merits of OpenSky's petition when considering VLSI's termination request. Indeed, the Director "recognize[d] that" although "the 'compelling merits' analysis would not normally apply where the *Fintiv* factors are not implicated … , when determining

whether to continue an IPR initially filed for improper purposes, [she] must consider the public interest, which compels the USPTO to evaluate unpatentability challenges that, at the institution stage, evidence compelling merits." Appx86.

Nor is there any conflict between the *Fintiv* memorandum and the Director's application of its underlying principles here. The memorandum underscores that the Board has flexibility to reach a just outcome when addressing an abuse of process. Appx7371 ("[T]he PTAB ***retains discretion*** to deny institution for proceedings where abuse has been demonstrated."); Appx7376 ("the PTAB ***may*** deny institution" if circumstances "such as abuse of process" exist). Nothing in the memorandum establishes an expectation that institution should be denied whenever there is an abuse of process. Here, the Director engaged in the context-dependent inquiry contemplated by the memorandum and the regulations, explaining that "'the unique dynamics of this case, coupled with the public interest in evaluating patent challenges with compelling merits' counseled against immediate termination." Appx106-107 (quoting Appx84).

4. VLSI's "hearsay" challenge to the compelling-merits determination is meritless.

VLSI further challenges (at 38-43) the Board's and Director's compelling-merits determinations as "rest[ing] on inadmissible hearsay." The compelling-merits decisions, however, are not reviewable because they were part of the Director's institution review. *Supra* pp. 51-53. Notably, VLSI's hearsay argument

focuses entirely on Dr. Jacob's declarations at the time of institution and treats post-institution events as "mak[ing] no difference." Br. 42. VLSI's quarrel with the Board's and Director's analysis of the institution-phase evidence is simply not reviewable on appeal. 35 U.S.C. §314(d).

VLSI's hearsay argument is also wrong on the merits. "Hearsay" refers to a statement, "offer[ed] in evidence to prove the truth of the matter asserted," that "the declarant does not make while testifying ***at the current trial or hearing***." Fed. R. Evid. 801(c). But during the institution phase, there is no "trial or hearing." Consequently, the Board typically waits until ***after*** institution to resolve hearsay objections. *E.g.*, *Intel Corp. v. Qualcomm Inc.*, IPR2018-01429, Paper 8 at 12-13 (P.T.A.B. Feb. 15, 2019) (hearsay arguments "premature" at institution stage); *Valve Corp. v. Ironburg Inventions Ltd.*, IPR2016-00949, Paper 10 at 5 (P.T.A.B. Sept. 26, 2016) (same). In fact, the USPTO's regulations provide that "[a]ny objection to evidence submitted during a preliminary proceeding" need not be filed until ten business days ***after*** "institution of the trial." 37 C.F.R. §42.64.

The Director was clear that the compelling-merits analysis should consider only the institution-phase record: "In making its determination, the Board must analyze the evidence and the parties' arguments as they existed at the date of institution." Appx87; *see* Appx86 (remanding for Board to consider "whether the record … prior to institution indicates that the Petition presents a compelling,

meritorious challenge"). The Director, moreover, instructed that the compelling-merits analysis should consider whether the "'evidence, ***if unrebutted at trial***, would plainly lead'" to unpatentability. Appx86; *see* Appx91-92. Under that standard, it was clearly appropriate for the Board and Director to consider Dr. Jacob's declarations, treating them as "unrebutted" for purposes of the compelling-merits analysis, and to address VLSI's hearsay objections in the IPR's post-institution "trial" phase. Appx96; Appx99.

Analogously, district courts routinely treat hearsay objections as premature at the motion-to-dismiss stage, when considering whether a complaint presents sufficient evidence for a lawsuit to continue. *See Prince v. Madison Square Garden*, 427 F. Supp. 2d 372, 378 (S.D.N.Y. 2006) ("[I]t is inappropriate at this [motion-to-dismiss] stage to consider whether or not the factual support underlying [the complaint] constitutes hearsay."); *Guzman v. Mana*, 2018 WL 10150989, at *2 n.2 (D.N.J. Dec. 6, 2018) ("[T]hat the [complaint] contains alleged hearsay statements is irrelevant because at the motion to dismiss stage, the Court is required to accept all factual statements as true in order to 'test the legal sufficiency of the complaint.'"); *Polar Molecular Corp. v. Amway Corp.*, 2007 WL 3473112, at *4

(W.D. Mich. Nov. 14, 2007) ("Whether the allegations in the complaint are based on hearsay is not relevant to a motion under Rule 12(b)(6) or 12(c).").[9]

Regardless, even after institution of an IPR, "the Board regularly considers sworn declarations in lieu of live testimony." Appx122. Indeed, the USPTO's regulations require that "[u]ncompelled direct testimony ***must*** be submitted in the form of an affidavit." 37 C.F.R. §42.53(a). Dr. Jacob's declarations were thus similarly situated to expert declarations in every IPR, where there is no opportunity to present live direct testimony for an expert (or any witness). *See Grünenthal GmbH v. Antecip Bioventures II LLC*, PGR2018-00062, Paper 32 at 15 (P.T.A.B. Oct. 29, 2019) ("Without exception, the Board accepts … sworn witness declarations in lieu of live testimony in administrative patent trials."); *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2016-00130, Paper 35 at 19, 22-23 (P.T.A.B. May 8, 2017) ("[W]e do not consider [the] declarations to be hearsay, as

[9] VLSI's cited Board decisions (at 40) do not address the same situation. Two involved hearsay determinations as part of ***final written decisions***. *ABS Global, Inc. v. XY, LLC*, IPR2018-01224, Paper 28 at 17-19 (P.T.A.B. Dec. 9, 2018); *Unified Patents Inc. v. Sound View Innovations, LLC*, IPR2018-00599, Paper 50 at 50-51 (P.T.A.B. Sept. 9, 2019). The third involved a panel declining to give weight to a declaration submitted by the ***patentee*** (not the petitioner) in deciding whether there was sufficient evidence to institute an IPR. *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, IPR2017-01188, Paper 22 at 33 (P.T.A.B. Oct. 11, 2017). VLSI's cited district court appeals (at 40) are similarly off-point, as they involved decisions excluding hearsay ***at trial***. *Wilson v. Wexford Health Sources, Inc.*, 932 F.3d 513, 522 (7th Cir. 2019); *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489 (5th Cir. 2021).

they are not out-of-court statements. In an [IPR], direct testimony is typically provided via affidavit, with cross-examination taken via deposition.").

Faced with this reality, VLSI attempts (at 41 & n.8) to distinguish Dr. Jacob's two declarations here from all other expert declarations submitted in IPRs by pointing out that they were originally prepared for the two IPRs that Intel initially filed against the '759 patent. As the Board explained, though, "[t]he fact that the Jacob declarations were prepared for another proceeding is immaterial in this case because Dr. Jacob has expressly adopted them for *this* proceeding." Appx205 (emphasis original). Specifically, Dr. Jacob made himself available for cross-examination by deposition ***in this IPR***, where he testified that "all of [his] opinions regarding the '759 patent [were] set forth in [his two original] declarations." Appx10600(73:4-6); *see* Appx10596(69:12-17); Appx10599(72:11-21); *see also* Appx16746(¶5) ("I stand behind and reaffirm my October 30, 2019 Declaration … and my February 4, 2020 Declaration[.]"). Accordingly, as the Board found, Dr. Jacob's declarations "are no different than the other testimony relied on by the parties, and are not hearsay subject to exclusion." Appx204.

Consistent with that understanding, VLSI does not challenge the Board's determination that Dr. Jacob's declarations were not hearsay at the time of the final written decision, where the Board explained that Dr. Jacob's "reaffirmance of the prior testimony" and "cross-examination in this proceeding overcomes any plausible

hearsay argument." Appx203-205 (emphases omitted). VLSI nevertheless argues (at 41) that "nothing in 'the record before the Board ***prior to institution***' … showed that Dr. Jacob would be available for cross-examination." But as discussed above, it would have been premature to address VLSI's hearsay objection during the institution phase. *Supra* pp. 58-60. Even so, the Board correctly observed in its institution decision that the pre-institution record "d[id] not indicate that Dr. Jacob would be unwilling to participate in this proceeding or [wa]s constrained by a prior agreement from participating." Appx1221. That Dr. Jacob later reaffirmed his declarations and submitted to cross-examination via deposition confirms the wisdom of the Board's and Director's decisions. *See* Appx204-205.

Despite its protestations, VLSI nowhere denies that Dr. Jacob's two original declarations—which were prepared for IPRs filed by Intel and signed by Dr. Jacob pursuant to 18 U.S.C. §1001 (Appx4276-4277; Appx5710-5711)—have the same guarantees of trustworthiness as declarations created specifically for this IPR. This further establishes that they are not inadmissible hearsay. *See Apple Inc. v. VirnetX Inc.*, IPR2016-00332, Paper 29 at 81-82 (P.T.A.B. June 22, 2017) (allowing declaration submitted under oath in different proceeding because it "has the same circumstantial guarantees of trustworthiness as those declarations actually created for this proceeding"); *ClearOne, Inc. v. Shure Acquisition Holdings, Inc.*, IPR2019-00683, Paper 91 at 13-14 (P.T.A.B. Aug. 14, 2020) (holding that declaration and

transcript testimony from a different proceeding "fall within the residual exception under FRE 807, because the testimony was given under oath and has the same guarantees of trustworthiness as testimony created for this proceeding").

Ultimately, the Board found that VLSI "suffered no prejudice from Dr. Jacob's [o]riginal [d]eclarations." Appx203-204. VLSI does not challenge that finding on appeal, and it confirms that any error in considering the declarations during the compelling-merits stage would have been—at most—harmless. For all these reasons, VLSI has not shown that the Board or Director abused their discretion by considering Dr. Jacob's declarations as part of the institution-phase, compelling-merits analysis. *See Tiger Lily Ventures Ltd. v. Barclays Capital Inc.*, 35 F.4th 1352, 1366 (Fed. Cir. 2022) (holding that appellant's allegations based on hearsay "lead only to the conclusion that [appellant] disagrees with the Board's rulings on the evidentiary issues and the weighing of the evidence," but appellant "offers no basis to conclude that the Board abused its discretion").

5. The Director's non-termination decision is consistent with the statute, regulations, and precedent.

Finally, the Director's discretionary decision not to terminate the IPR is consistent with governing law. VLSI identifies no case where this Court vacated and ordered the Director or Board to dismiss an entire proceeding as a sanction. Nor is Intel aware of any case where this Court imposed stricter sanctions than the Director or Board found warranted under 37 C.F.R. §§11.18, 42.11, or 42.12.

Simply put, this Court typically does not second-guess the Director's or Board's sanctions. *E.g.*, *Voip-Pal.com*, 976 F.3d at 1324 (affirming Board's denial of case-dispositive sanction); *Abrutyn*, 15 F.3d at 1053 ("As long as the tribunal's [sanction] falls within a reasonable range, it cannot constitute an abuse of discretion.").

VLSI's assertion (at 34-36) that the Director departed from the applicable statute and regulations by ignoring deterrence and punishment concerns goes nowhere. The Director made clear that she would impose sanctions "proportional to the conduct" and "necessary to deter such conduct by OpenSky or others in the future." Appx41; *see* Appx63; Appx81-83; Appx106-108. To that end, the Director ordered OpenSky to show cause why it should not pay compensatory damages including attorney fees (and later ordered OpenSky to pay $413,264.15 in fees). Appx41; Appx87-88; *see* Appx237.

VLSI also wrongly claims (at 36-38) that the Director violated the APA by deviating from USPTO practice. In fact, the Board has previously rejected requests to terminate or not institute IPRs based on accusations of impropriety where—like here—the accused conduct did not affect the unpatentability merits. *E.g.*, *Coalition for Affordable Drugs VI, LLC v. Celgene Corp.*, IPR2015-01092, Paper 19 at 3-5 (P.T.A.B. Sept. 25, 2015) (denying termination where patentee asserted that petitioners falsely identified "motive" for filing IPR but nowhere alleged that patentability challenge was "non-meritorious"); *Coalition for Affordable Drugs II*

LLC v. NPS Pharms., Inc., IPR2015-01093, Paper 26 at 28-30 (P.T.A.B. Oct. 23, 2015) (instituting IPR despite patentee's contention that petition was filed for "improper purpose" where there was no allegation of "a nonmeritorious patentability challenge").

Ignoring these examples, VLSI alludes (at 36-37) to cases where the Board terminated an IPR "upon 'finding that [the] IPR was improperly instituted.'" That is not what happened here. Appx82. Rather, the Director found that the Board properly instituted review of OpenSky's "meritorious" petition and "agree[d] with" the institution decision. Appx29-30 & n.4. *I.M.L. SLU v. WAG Acquisition, LLC*, IPR2016-01658, Paper 46 at 6-7 (P.T.A.B. Feb. 27, 2018), is additionally distinguishable because the original petitioner there sought an adverse judgment against itself, implicitly acknowledging that the IPR never should have been instituted. Also unlike *I.M.L.*, the record here is clear that the joined party (Intel) is not a real-party-in-interest to the original petitioner (OpenSky). Appx1682-1683.

VLSI's complaint (at 36) about Intel getting "a fourth bite at the apple" is also misplaced. Intel initially filed its IPR petitions against the '759 patent within one year of being sued. Appx43; Appx85. The Board discretionarily denied those petitions without reaching the merits, relying on the fast-tracked and unrealistic Texas trial schedule that VLSI obtained through forum-shopping and applying *Fintiv* in a way that contradicts the USPTO's current rules. Appx43-44; Appx85-86;

Appx107; *supra* pp. 15-17. And, as the Director recognized in these proceedings, Intel was not "complicit in OpenSky's abuse." Appx85; *see* Appx108. VLSI's cry that it was unfair for the Board to consider unpatentability arguments it should have considered years earlier thus rings hollow.

B. The Director Did Not Abuse Her Discretion In Demoting, Dismissing, Or Reinstating OpenSky.

VLSI next criticizes (at 44-45) the Director for relegating OpenSky to an understudy role, contending that this was "a reward, not a sanction" because it allowed OpenSky to "shift costs to Intel." But the Director explained why demoting OpenSky was a sanction—and a particularly appropriate one—given the specific misconduct here: "[r]emoving OpenSky's control of the IPR removes its ability to leverage that control for or against a particular party." Appx84. As the Director emphasized, removing OpenSky's control was "indeed a sanction" because "the record demonstrates OpenSky's desire to profit from [its] leverage." Appx108.

VLSI also argues (at 45-46) that the Director acted arbitrarily by dismissing OpenSky from the proceeding and then reinstating it weeks later. But there was nothing amiss with the Director's actions, which she explained at each step. The Director chose to dismiss OpenSky from the IPR so that OpenSky "d[id] not benefit from its abuse of the IPR process." Appx116-117. Upon further consideration, however, the Director restored OpenSky as a petitioner to eliminate any questions concerning her jurisdiction to impose further sanctions against OpenSky, which she

was continuing to evaluate. Appx128 (citing *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2021-01229, Paper 108 at 4 (P.T.A.B. Jan. 27, 2023)). The Director was plainly entitled to revisit her earlier decision while she considered the unusual circumstances of this case. *GTNX, Inc. v. INTTRA, Inc.*, 789 F.3d 1309, 1313 (Fed. Cir. 2015) (Board has "'inherent authority to reconsider [its] decisions'"). Moreover, the Director acted reasonably in reinstating OpenSky, as she was obligated to satisfy her own jurisdictional concerns, and appropriately addressed those concerns proactively.

C. The Director's Fee Award Does Not Somehow Suggest That The Director Should Have Terminated The IPR.

After denying VLSI's request to terminate the IPR, the Director determined it was "appropriate to award attorney fees to VLSI for the time spent addressing OpenSky's abusive behavior" and authorized VLSI to file a motion for fees. Appx127; *see* Appx128-141. With termination no longer at issue, the Director then granted VLSI's fee motion and ordered OpenSky to pay $413,264.15 to VLSI. Appx211; *see* Appx225-237.

VLSI characterizes (at 46-47) that monetary sanction as a "hollow gesture" that "cannot excuse" the Director's "refusal to terminate," based on VLSI's own speculation that OpenSky might not be able to pay the amount awarded. VLSI never argued to the Director that OpenSky's ability (or inability) to pay should factor into the fee award, much less that it would be a reason to terminate the IPR. That

argument is thus forfeited. *In re NuVasive*, 842 F.3d 1376, 1380 (Fed. Cir. 2016) ("[A] party waives an argument that it 'failed to present to the [USPTO].'").

Regardless, whether OpenSky can pay the fee award has nothing to do with the Director's earlier decision not to terminate the IPR: as discussed above, the Director declined to terminate the IPR because OpenSky's petition presented "compelling merits" of unpatentability. The Director subsequently considered what sanction was appropriate for OpenSky's misconduct, and chose to award attorney fees "because of the manner in which OpenSky conducted itself after the [p]etition was filed." Appx134. That fee award readily falls within the range of possible sanctions the Director could impose (*supra* pp. 53-54), and the Director "explain[ed] why [she] deemed the sanctions employed to be appropriate for this particular situation." Appx107-108. VLSI has demonstrated no reason for this Court to second-guess the Director's discretionary sanctions decisions.

* * *

VLSI concludes (at 49) that "[o]nly termination" of the IPR "will provide adequate deterrence and punishment." The Director thought otherwise, and whatever consequence VLSI would prefer, the Director in no way abused her discretion by declining VLSI's request to terminate the entire IPR. *See* Appx108 ("That VLSI would have made the policy choice to use a different sanction here does not demonstrate error in how [the Director] exercised [her] discretion.").

Alternatively, VLSI requests (at 49) vacatur for the Director to reconsider sanctions, including termination. There is no need for any remand. The Director has already considered extensive briefing and evidence, and she issued multiple detailed opinions to craft sanctions calibrated to the facts. But if this Court were inclined to remand on any sanction issue, it should make clear that termination of the IPR is off the table—as the Director appropriately decided when she affirmed the Board's compelling-merits determination in December 2022 (Appx123-124; *see* Appx84-87). Any other sanctions proceeding, such as further consideration of attorney fees, would be collateral to and cannot affect the Board's unpatentability determinations. *See Elbit Sys. Land & C4I Ltd. v. Hughes Network Sys., LLC*, 927 F.3d 1292, 1296-1306 (Fed. Cir. 2019) (affirming district court's infringement judgment, while recognizing that court's unquantified fee award was not final and thus not appealable).

CONCLUSION

The Board's unpatentability determinations should be affirmed. If reviewed, the Director's decision not to terminate the IPR should also be affirmed.

Respectfully submitted,

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