No. 2023-1712

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

XMTT, INC.
Plaintiff-Appellant,

v.

INTEL CORPORATION,
Defendant-Appellee.

On Appeal from the United States District Court for the District of Delaware,
No. 1:18-cv-01810-MFK, Judge Matthew F. Kennelly

COMBINED PETITION FOR PANEL REHEARING AND REHEARING EN BANC BY XMTT, INC.

MORGAN CHU
ANTHONY ROWLES
BENJAMIN HATTENBACH

IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067
(310) 277-1010

Attorneys for Plaintiff-Appellant XMTT, Inc.

January 3, 2025

CERTIFICATE OF INTEREST

Counsel for Plaintiff-Appellant XMTT certifies the following:

1. Represented Entities. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

XMTT, Inc.

2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

None.

3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

4. Legal Representatives. Fed. Cir. R. 47.4(a)(4). List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court.

Irell & Manella LLP: Philip Warrick, Jordan Nafekh

Farnan LLP: Brian Farnan, Michael Farnan

5. Related Cases. Fed. Cir. R. 47.4(a)(5). Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case.

Intel Corporation v. XMTT, Inc., 2021-2127, April 19, 2022, United States Court of Appeals for the Federal Circuit.

6. Organizational Victims and Bankruptcy Cases. Fed. Cir. R. 47.4(a)(6). Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees).

None.

/s/ *Anthony Rowles*

Anthony Rowles

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*** All emphasis is XMTT's unless otherwise noted ***

STATEMENT OF COUNSEL

Pursuant to Federal Circuit Rule 40(c)(1) and Federal Rule of Appellate Procedure 40(b)(2), based on my professional judgment, I believe the panel decision is contrary to the following decisions of the Supreme Court of the United States or the precedents of this Court: *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc) (holding that patent claims must be construed through the eyes of the person of ordinary skill in the art, who "is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field"); *id.* at 1321 (cautioning against focusing "on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent"); *id.* at 1316 (confirming that claim construction requires "a full understanding of what the inventors actually invented and intended to envelop with the claim," and that "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction'" (quoting *Renishaw PLC v. Marposs Societa' per Azioni,* 158 F.3d 1243, 1250 (Fed. Cir. 1998))). This conflict with binding precedent supports rehearing by either the panel or the *en banc* Court.

/s/ *Anthony Rowles*
Anthony Rowles
Counsel for Plaintiff-Appellant XMTT, Inc.

POINTS OF LAW AND FACT OVERLOOKED OR MISAPPREHENDED

This Court's decision summarily affirming the district court's judgment under Rule 36 without elaboration necessarily relied upon a flawed district court claim construction interpreting claim terms including the words "serial processor" in a manner inconsistent with: 1) their "meaning in the field" (including by Intel itself outside of this dispute), 2) the full language of the claims, and 3) their "meaning … within the context of the patent" (including the very purpose of the invention) contrary to this Court's seminal *Phillips* claim construction decision. *Phillips*, 415 F.3d at 1313, 1321. By affirming the district court's grant of summary judgment, the Court overlooked or misapprehended the established meaning of a "serial processor" to those of skill in the relevant art of computer architecture at the time of the invention, resulting in a construction that neither "stays true to the claim language" nor "aligns with the patent's description of the invention." *Id.* at 1316 (quoting *Renishaw*, 153 F.3d at 1250).

This simplistic construction cannot be reconciled with the express claim language defining the "serial processor" as executing "software instructions…primarily in serial," the use of the term by the inventor in these and other patents to describe modern CPUs, the purpose of the invention to improve the memory architecture for contemporaneous computers with CPUs and GPUs, as well as the goal of providing "efficient computation of serial processing." Appx42 (1:61-

64). As Intel admits, this construction excludes virtually all modern processors, including the CPUs in "contemporary personal computers" with CPUs and GPUs that Dr. Vishkin described as the foundation for his novel memory architecture. *See* Intel Br. 43-44; Appx42 (1:25-37); *see also SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1378 (Fed. Cir. 2013) ("A claim construction that excludes the preferred embodiment is rarely, if ever, correct and would require highly persuasive evidentiary support.").

This flawed claim construction leads to an absurd result, implying that Dr. Vishkin—a world-renowned computing expert with decades of experience in computer architecture—drafted patent claims nonsensically limited to a type of processor unused by virtually anyone for decades, and incompatible with the processors described throughout the patents and commonly used in the art. Furthermore, these patents do not purport to describe or claim a different method of executing instructions from that known in the art. Rather, Dr. Vishkin foresaw the need for improvements to the memory architectures used for serial and parallel-type processors, respectively, and claimed an improved system marrying that improved memory architecture with the processors used in existing hybrid serial/parallel systems that included both serial (CPU) and parallel (GPU) processors. There is no plausible reason that Dr. Vishkin would endeavor to improve the memory

architecture of existing hybrid systems while simultaneously crippling the underlying processor performance.

The district court—and by extension this Court—reached this nonsensical conclusion through a series of fundamental claim construction errors. For example, even assuming "serial" has a commonly understood non-technical meaning, and even further assuming it had a narrow meaning at the dawn of modern computing, skilled artisans have not understood "serial processors"—much less those that explicitly execute instructions "primarily in serial"—to be limited to simplistic "one at a time" operation since well before the time of the invention. *See, e.g.*, Appx6335 (1:19-38). Additionally, the claims themselves expressly define a "serial processor" as executing instructions "primarily in serial." Appx33; Appx48. The district court effectively ignored this language, giving it no weight in either claim construction or its infringement analysis. Remedying those errors results in the correct, plain-meaning construction of "a serial processor to execute instructions in a computing program primarily in a sequential manner" (i.e., "in serial"). Even if the Court agreed with the district court's flawed interpretation of "serial" processing, it would at minimum need to correct the omission of "primarily in serial," i.e., "a processor that executes instructions **primarily** one at a time, in a sequential manner."

The district court expressly and necessarily relied on its "serial processor" construction in granting summary judgment, and this Court's Rule 36 affirmance

likewise necessarily relies on that flawed interpretation of the claim language. Indeed, Intel did not even attempt to defend the non-infringement judgment under any other claim construction. *See* Intel Br. 49, 67-68. XMTT did not waive the correct construction in the district court proceedings, and there are disputed issues of material fact as to whether Intel infringes under a proper claim construction. Remand is necessary because this Court should not perform that analysis in the first instance, particularly with regard to a term of degree like "primarily." *See, e.g.*, *Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1310-11 (Fed. Cir. 2003) (vacating construction that limited "generally parallel" to "parallel"); *Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 907-09 (Fed. Cir. 2005) (vacating construction limiting "substantially flattened surfaces" to "flat" surfaces).

ARGUMENT

A. The Flawed Construction of "Serial Processor" Cannot Be Reconciled with the Claim Language, the Term's Understood Meaning in the Field, or the Purpose of the Invention

The district court's claim construction adopted an unreasonably simplistic understanding of "serial processor" that requires executing instructions "one at a time." The district court identified no evidence supporting its imposition of the "one at a time" limitation, and the phrase "one at a time" appears nowhere in the claims or specification. *See* Appx9-12. The district court apparently relied on a lay

understanding of "serial" inconsistent with the intrinsic record, thereby improperly focusing "on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent." *Phillips*, 415 F.3d at 1321; *see also Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1320 (Fed. Cir. 2016) ("Ordinary meaning is not something that is determined 'in a vacuum.'" (quoting *Medrad, Inc. v. MRI Devices Corp.,* 401 F.3d 1313, 1319 (Fed. Cir. 2005))). At oral argument, the panel in this appeal appeared to accept this "plain meaning" of the claim terms divorced from the context of the claimed invention. For example, Chief Judge Moore stated that "the district court's construction of serial processor is what I think would be the plain meaning of serial processor" before asking XMTT's counsel if the inventor acted as his own lexicographer. Oral Arg. at 9:42-10:10, https://oralarguments.cafc.uscourts.gov/default.aspx?fl=23-1712_12032024.mp3.

The district court's judgment cannot be affirmed based on the meaning of "serial" in a vacuum. The actual claim element that the district court purported to construe was a "serial processor adapted to execute ***software instructions*** in a software program ***primarily in serial***." Appx48 (13:52-53), Appx9 (quoting the claim language). But the district court did not even attempt to address whether the alleged serial processor "***executes instructions primarily one at a time***, in a sequential manner." Instead, the district court concluded that any degree of concurrent operation, even if occurring at the more granular scale of "micro-

operations" rather than the claimed "software instruction," was outside the scope of the claims. *See* Appx16-18 (finding no infringement based on "'instruction-level parallelism' at the 'micro-operation' level"). Intel itself did not even seek affirmance of the district court's summary judgment under any other construction than the one requiring the serial processor to execute instructions exclusively "one at a time, in a sequential manner." *See* Intel Br. 36. Applying a term of approximation presents a particularly "difficult factual determination" that should be made by a factfinder rather than as a matter of law. *See Playtex*, 400 F.3d at 908 ("The point at which the gripping area curvature ceases to be *substantially* flattened and becomes *generally* cylindrical is a question of fact.").

The district court's misguided approach led to a construction that neither "stays true to the claim language" nor "aligns with the patent's description of the invention." *Renishaw*, 153 F.3d at 1250. At a minimum, the record here compels a different construction—one that incorporates the express definition of executing "instructions…primarily in serial" and reflects the patents' stated objective of providing an improved memory architecture in contemporary computers to interface with existing CPUs (with serial processor elements) and GPUs (with parallel processor elements).

1. The Claims Define the "Serial Processor" as Executing Instructions "Primarily in Serial"

The district court quoted the "primarily in serial" claim language (Appx9 n.5), but did not even attempt to explain its omission from the ordered construction or reconcile it with its brand new requirement of executing instructions "one at a time." The district court's construction effectively read "primarily in serial" out of the claim despite expressly acknowledging "that courts must interpret claims 'with an eye toward giving effect to all terms in the claim.'" Appx11 (quoting *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)). Interpreting claims to render terms void is highly disfavored by this Court. *See, e.g.*, *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809-10 (Fed. Cir. 2021) (collecting cases).

This Court appears to have accepted Intel's argument that the district court only construed "serial processor" and premised its judgment on the absence of a "serial processor" in the accused products. *See, e.g.*, Intel Br. 36. This would nonsensically require a "serial processor" that exclusively "executes instructions one at a time, in a sequential manner" to somehow be "[adapted] to execute instructions" in a more complex way, i.e., "primarily in serial." *See* Appx48 (claim 1). Furthermore, the district court's claim construction includes the supposedly "unconstrued" language about executing instructions, but simply omits the modifier "primarily." *See* Appx9 ("a processor that executes instructions one at a time in a sequential manner").

Indeed, just prior to summary judgment, the district court issued a claim construction order accepting XMTT's position that the claim "already states that a 'serial processor' is a 'processor adapted to execute software instructions in a software program primarily in serial.'" Appx14696. It rejected Intel's argument that "primarily" referred to a mode in which the "system" was operating. Appx14693, Appx14696-14697. This makes sense because, as described in the introduction of the patent specification, contemporary computer systems typically included two types of processors: e.g., a "CPU" for managing serial operations and a "GPU" for managing parallel computation. Appx42 (1:25-44). The claims thus use the terms "serial" and "parallel" as natural labels to distinguish the two in the claimed apparatus, but the claims do not stop there—as the district court correctly acknowledged, they go on to define how the two types of processors are different, e.g., the "serial processor" is "adapted to execute software instructions in a software program primarily in serial," while the "parallel processors" are "adapted to execute software instructions in the software program primarily in parallel." Appx48 (13:51-59).

At summary judgment, the district court did not revisit this reading of the claim structure; rather, it decided that the claimed "serial processor," i.e., the "processor adapted to execute software instructions in a software program primarily in serial," must always "execute[] instructions one at a time in a sequential manner."

See Appx9, Appx16. That construction was wrong and conflicts with both the literal claim language and the rest of the intrinsic evidence.

Even if Intel were correct regarding what the district court actually construed, the district court also failed to consider "primarily in serial" as part of its infringement analysis (*see* Appx16-18), thereby arriving at the same improper result. Intel argued on appeal that XMTT improperly focused on "surrounding claim language" (Intel Br. 36),[1] but this Court consistently requires precisely that analysis. *See, e.g.*, *ACTV, Inc. v. Walt Disney Co.,* 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms."). This Court corrected a similar error in *Mars, Inc. v. H.J. Heinz Co.*, 377 F.3d 1369 (Fed. Cir. 2004), reversing a summary judgment of non-infringement because the district court misconstrued the claim limitation "a mixture of solid and lipid ingredients" by focusing improperly on the term "ingredients" in isolation rather than in the context of the complete limitation. *Id.* at 1373-74.

[1] Intel itself repeatedly proposed constructions of "serial processor" that included the "primarily" language. *See e.g.*, Appx13932; Appx14565; Appx12464; Appx14693; Appx13627. Moreover, Intel previously insisted that "primarily in serial" modifies "serial processor." *See, e.g.*, Appx109; Appx12461.

2. The Court Misapprehended the Meaning of "Serial Processor" to Skilled Artisans at the Time of the Invention

The district court's construction also conflicts with the established meaning of the term in the field of the invention as reflected by the intrinsic evidence. As Dr. Vishkin's other patents (cited on the face of the patents-in-suit) explain, the "processing architecture employed by today's personal computers is based on the von-Neuman architecture developed in the late 1940s." Appx6335 (1:19-23). While "originally" (i.e., "in the late 1940s"), that architecture "presumed … a set of sequentially executed instructions without any concurrent operations," modern implementations in "today's personal computers" permit "execution of instructions in stages such that different instructions may be at different stages of processing at the same time, or 'multiple-issue'—the issuance of multiple instructions at the same time." *Id.* (1:26-38). That description is entirely consistent with the patents-in-suit, which describe improvements to "contemporary personal computers (PCs)" that perform "serial and parallel processing" using a "CPU" and "GPU," respectively, "within the same system" where the "serial processing" involves instructions being "executed serially as in a von Neumann or other sequential architecture, or the like." Appx42 (1:25-54); Appx43 (4:39-42). It also comports with the plain language of the claims, which—as discussed above—define the "serial processor" as one that executes "software instructions…primarily in serial." Limiting the claims instead to execution "one at a time" conflicts with all of this intrinsic evidence.

Intel defended the construction on appeal by pointing to "contemporaneous technical dictionaries" allegedly supporting its position. Intel Br. 8. This extrinsic evidence cannot outweigh the Vishkin patents that are part of the intrinsic record, but in any event none of the cited definitions addresses "serial processor" specifically, and the term "one at a time" originated not from these definitions, but rather from Intel's own expert report, which characterized a particular "traditional" implementation of a "serial scalar von Neumann architecture." Appx6501-6502.

Furthermore, Intel itself characterizes contemporary CPUs as "designed for serial processing" when seeking patent protection from the USPTO for its own technology. *See* Appx10410 (¶18) (characterizing a CPU as "a processor architecture … designed for ***serial processing***"). And in a prior appeal, Intel expressly argued that "primarily" modifies the processor itself. Specifically, Intel argued that the same "'primarily in serial' and 'primarily in parallel' terms describe characteristics of the serial and parallel processors as individual components," *Intel Corp. v. XMTT, Inc.*, No. 21-2127, ECF No. 13 (opening brief), at 37, and that "the processors themselves—as individual components—must be adapted to execute primarily in serial or primarily in parallel," *id.* at ECF No. 17 (reply brief), at 27-28.

As this Court has held, even construing "words of ordinary usage" requires "understanding [claim terms] in the context in which they were used by the inventor … and understood in the field of the invention." *Toro Co. v. White Consol. Indus.,*

Inc., 199 F.3d 1295, 1299 (Fed. Cir. 1999). That is particularly true for technical terms like the claimed "serial processor" because words in a patent "must be understood and interpreted by the court as they would be understood and interpreted by a person in that field of technology," who would "have knowledge of any special meaning and usage in the field." *Phillips*, 415 F.3d at 1313 (quotation omitted); *Eon*, 815 F.3d at 1321 ("[T]he question is not whether there is a settled ordinary meaning of the terms in some abstract sense of the words."). Here, the construction necessarily relied upon by this Court cannot be reconciled with the meaning of "serial processor" to a skilled artisan in the field of computer architecture.

The district court's narrow interpretation is particularly inappropriate in view of the prior-art nature of the "serial processor" recited in the claims. *See, e.g.*, *Lone Star Silicon Innovations LLC v. Iancu*, 813 F. App'x 512, 520 (Fed. Cir. 2020) (rejecting a narrow construction of a term that "the specification never characterizes … as part of the patent's inventive contribution, or providing particular advantages over prior art"). These patents do not even purport to reflect a new serial or parallel processor. As reflected in their titles and throughout the specifications, they are directed to novel memory architectures and related improvements to existing computing systems performing both serial and parallel processing (e.g., personal computers with a CPU and GPU). *See* Appx42 (1:25-54).

That is why the patents do not define "serial processor" beyond the meaning provided by the express claim language. Serial processors had an established meaning in the art at the time of the invention, and "[a] patent need not teach, and preferably omits, what is well known in the art." *E.g.*, *Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1336-37 (Fed. Cir. 2009) (affirming a construction of "transparent window layer" that included ITO because "ITO as a transparent conductive layer was already known to those of skill in the art," and thus the patent "did not need to make further enabling disclosures about its prior art uses").

3. The Simplistic Construction Used by the District Court Cannot Be Reconciled with the Purpose and Description of the Claimed Invention for Sophisticated Processing

The incorrectness of the district court's construction is "reinforced by the undisputed fact that [it] would exclude the … products that the patents were designed to cover." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007). These patents expressly relate to a "computer memory architecture for hybrid serial and parallel computing systems," describe a PC including both a CPU and GPU as the sole example of such existing hybrid systems, and identify inefficient transitioning between serial and parallel processing as a weakness of those existing systems. Appx42 (1:25-54). While the specifications describe various "novel features" and techniques to improve those transitions, *e.g.*, Appx42 (2:3-11); Appx44 (6:6-15), they consistently describe the serial processor in the same way as

a person of skill would understand a typical CPU core in "contemporary PCs" at the time. *See* Appx10356 (¶77). The patents describe and claim improvements via a novel memory architecture for those contemporary processors, but not improvements to the processors' methods of executing instructions. *See, e.g.*, Appx42.

There is no dispute that, by the time of the invention, virtually no computer processors—and certainly no computer processors used as CPUs in personal computers—executed instructions "one at a time" in the manner construed by the district court. *See* Intel Br. 43-44. The district court did not even attempt to explain why Dr. Vishkin, who spent decades researching improvements to contemporary general-purpose processors, would have invented such a complex memory architecture and mode management for hybrid computing environments but limited them to simple, archaic processors. Nor did it provide any reason to think that such an arbitrary and artificial constraint on processor performance would advance the stated goal of providing an improved hybrid computing architecture. *See, e.g.*, *Kaken Pharm. Co. v. Iancu*, 952 F.3d 1346, 1352 (Fed. Cir. 2020) ("A patent's statement of the described invention's purpose informs the proper construction of claim terms…."). Contrary to this Court's precedent, the district court failed to consider "what the inventor[] actually invented and intended to envelop with the claim." *Renishaw*, 158 F.3d at 1250. In sum, by interpreting a claim limitation related to a

prior-art component contrary to its express definition and contrary to the understanding of skilled artisans in the field, the district court effectively construed the invention out of the claims. *See, e.g.*, Appx42 (1:61-64) (explaining that the invention "may allow efficient computation of serial processing, parallel processing, or any mix of the two").

B. This Court Necessarily Relied on the Flawed District Court Claim Construction in Affirming the Grant of Summary Judgment of Non-Infringement That Expressly Relied on That Construction

This Court's Rule 36 summary affirmance necessarily rests on the district court's legally improper construction of the "serial processor" claim terms. The district court's non-infringement judgment itself expressly and necessarily relied on its erroneous claim construction, and the record does not support any alternative ground for affirmance.

1. The District Court's Grant of Summary Judgment Necessarily Relied on Its Flawed Claim Construction

The district court's summary judgment of non-infringement expressly and necessarily relied on its construction of "serial processor." *See* Appx16-18.

While the district court also misinterpreted the subsidiary term "execute," that flawed analysis does not provide an alternative basis for affirmance because it is encompassed within the "serial processor" construction. *See* Appx16 (concluding with a construction of "serial processor" following the analysis of "execute"). Furthermore, neither party asked for such a construction. *See* Appx12; Intel Br. 45-

48. In fact, the meaning of "execute" to those of skill in the art was not even in dispute—as XMTT applied Intel's own expert's definition. *See* Appx10152; Appx10356 (¶76).

2. Waiver Is Not a Proper Alternative Basis for Affirmance

On appeal, Intel argued that XMTT had waived argument that the claimed apparatus is "a serial processor to execute instructions in a computing program primarily in a sequential manner" (i.e., "in serial"). *E.g.,* Intel Br. 27-29. To the contrary, XMTT consistently maintained that the district court should give the "serial processor" limitations their plain and ordinary meaning. XMTT's appeal brief simply spells out what that plain and ordinary meaning is: a processor that executes instructions primarily in a sequential manner. Opening Br. 14. XMTT has consistently maintained that the "serial processor" limitations refer to a processor that executes instructions in a program primarily in a sequential manner. *See, e.g.*, Appx10144; Appx10151. The waiver doctrine does not preclude XMTT from pointing out the error in a claim construction it opposed below, or from "clarifying or defending the original scope of its claim construction." *Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1346 (Fed. Cir. 2001).

3. Correcting the District Court's Flawed Claim Construction Requires Reversal and Remand

As explained above, the district court expressly based its non-infringement judgment on its incorrect claim construction, and Intel sought affirmance based

solely on that construction. Once this Court corrects the claim construction, it should reverse the district court's erroneous summary judgment and remand for further proceedings under the correct claim construction. *See, e.g.*, *Amdocs (Israel) Ltd. v. Openet Telecom, Inc.*, 761 F.3d 1329, 1343 (Fed. Cir. 2014) (vacating non-infringement judgment after "correct[ing] the district court's erroneous construction").

Remand is particularly necessary here because the district court omitted a term of degree—"primarily"—from the claim construction. As this Court has acknowledged when applying the similar term "substantially," the point at which something ceases to be "substantially flattened" and becomes something else is a "question of fact" that requires a factfinder to make a "difficult factual determination."[2] *Playtex*, 400 F.3d at 908. This Court should not be the first to assess whether the factual record supports a finding that Intel's CPU cores are executing instructions primarily in serial.

[2] Indeed, the PTAB determined that the patents "use[] the term 'primarily' and 'substantially' interchangeably" and gave "primarily" the ordinary meaning of "substantially," i.e., "largely but not wholly." *Intel Corp. v. XMTT, Inc.*, IPR2020-00145, Paper 37, at 10 (PTAB May 11, 2021). Intel itself proposed that construction in district court. Appx14693.

CONCLUSION

For these reasons, XMTT respectfully requests that the Court grant this Petition and, upon rehearing or rehearing *en banc*, vacate the judgment and remand for further proceedings.

Dated: January 3, 2025

Respectfully submitted,

IRELL & MANELLA LLP

Morgan Chu
Anthony Rowles
Benjamin Hattenbach

By: /s/ *Anthony Rowles*
Anthony Rowles

Attorneys for Plaintiff-Appellant XMTT, Inc.

Addendum

NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

XMTT, INC.,
Plaintiff-Appellant

v.

INTEL CORPORATION,
Defendant-Appellee

2023-1712

Appeal from the United States District Court for the District of Delaware in No. 1:18-cv-01810-MFK, Judge Matthew F. Kennelly.

JUDGMENT

ANTHONY ROWLES, Irell & Manella LLP, Newport Beach, CA, argued for plaintiff-appellant. Also represented by MORGAN CHU, BENJAMIN W. HATTENBACH, Los Angeles, CA.

PAUL A. BONDOR, Desmarais LLP, New York, NY, argued for defendant-appellee. Also represented by JOHN M. DESMARAIS, JEFFREY SCOTT SEDDON, II; ADAM STEINMETZ, JUSTIN P.D. WILCOX, Washington, DC.

THIS CAUSE having been heard and considered, it is

ORDERED and ADJUDGED:

PER CURIAM (MOORE, *Chief Judge*, TARANTO, *Circuit Judge,* and SCHROEDER, *District Judge*[1]).

AFFIRMED. *See* Fed. Cir. R. 36.

ENTERED BY ORDER OF THE COURT

Jarrett B. Perlow
Clerk of Court

December 4, 2024
Date

[1] Honorable Robert W. Schroeder III, District Judge, United States District Court for the Eastern District of Texas, sitting by designation.

FORM 19. Certificate of Compliance with Type-Volume Limitations **Form 19**
July 2020

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2023-1712

Short Case Caption: XMTT, Inc. v. Intel Corporation

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Date: 01/03/2025

Signature: /s/ Anthony Rowles

Name: Anthony Rowles