IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

XMTT, INC.,	)	
	)	
Plaintiff,	)	
	)	
vs.	)	**Case No. 18-cv-1810-MFK**
	)	
INTEL CORP.,	)	
	)	
Defendant.	)	

MEMORANDUM OPINION AND ORDER

XMTT has sued Intel for infringement of two patents: U.S. Patent No. 7,707,388 (the '388 patent) and U.S. Patent No. 8,145,879 (the '879 patent). The patents are directed to a "computer memory architecture for hybrid serial and parallel computing systems." *XMTT, Inc. v. Intel Corp.*, No. 18-CV-1810-RGA, 2020 WL 2404825 (D. Del. May 12, 2020) (internal citation and quotation marks omitted) ("*XMTT I*"). XMTT contends that Intel has willfully infringed numerous claims of the asserted patents both literally and under the doctrine of equivalents.[1]

Intel has moved for summary judgment on all of XMTT's claims and also seeks the exclusion of certain testimony by two of XMTT's expert witnesses. XMTT has moved for partial summary judgment on certain issues and to preclude Intel's experts from testifying on various topics. In this opinion, the Court sets forth its construction of certain disputed claim terms. The Court also grants Intel's motion for summary judgment of noninfringement on all claims for the reasons stated below.

[1] XMTT contends that Intel infringes claims 1, 4, 13, 14, 16, 18, 19, 21, 22, 26, 31, and 33 of the '388 patent and claims 1, 4, 7, 15, 20, 23, 25, and 26 of the '879 patent.

Background

The Court takes the following facts from its prior orders and the parties' briefing. A more detailed recounting of the allegations can be found in the Court's July 22, 2022 decision on Intel's motion for supplemental claim construction. *See XMTT, Inc. v. Intel Corp.*, No. 18-CV-1810-MFK, 2022 WL 2904308 (D. Del. July 22, 2022) ("*XMTT II*").

A. The asserted patents and accused products

The two patents relate to computing and computer processing systems. Computing can occur in a "serial processing mode" or a "parallel processing mode," and "transitioning among processing modes is non-trivial and requires time and resources, as well as overall system organization." '388 patent at 1:52–54; '879 patent at 1:59–61. Both patents claim "[a] method of transitioning from a serial processing mode to a parallel processing mode in a computing system." '388 patent at 16:36–36; '879 patent at 16:20–21. The two patents also claim multiple apparatuses, each of which comprises a "serial processor" and a "plurality of parallel processors," among other components. According to the specifications, this "system architecture provides seamless transitions between parallel and serial processing modes, while maintaining memory coherence and providing sufficient performance for streaming applications." '388 patent at 1:64–67; '879 patent at 2:4–7.

Various Intel products that include computer processors are at issue in this case.[2] The patents state that "a 'processor' or 'process' includes any human, hardware

[2] XMTT's expert Dr. Thomas Conte states that the accused products include client processors in Intel's Amber Lake, Apollo Lake, Braswell, Broadwell, Coffee Lake, Comet Lake, Crystal Well, Gemini Lake, Haswell, Ice Lake, Ivy Bridge, Kaby Lake, Rocket Lake, Skylake, Tiger Lake, Valleyview, and Whiskey Lake product families.

and/or software system, mechanism or component that processes data, signals, or other information." '388 patent at 12:29–31; '879 patent at 12:45–47. The parties do not appear to dispute the meaning of this term. Each of the accused products comprises a central processing unit (CPU) with multiple cores, an integrated graphics processing unit (GPU), and various other components. The parties dispute whether the CPU and its cores are "serial processors" or "parallel processors."

B. The instant suit

XMTT filed this lawsuit against Intel on November 16, 2018. The case was previously assigned to Judge Richard Andrews. On April 30, 2020, Judge Andrews held a claim construction hearing to address five disputed terms of the asserted patents, and on May 12, 2020, he issued an order construing the five disputed claim terms. *XMTT I*, 2020 WL 2404825. The case was later reassigned to the undersigned District Judge.

Shortly after the Court's claim construction order, Intel petitioned to institute *inter partes* review of all the claims in the '388 patent. The Patent Trial and Appeal Board (PTAB, or Board) granted review, proposed its own construction of certain terms, and relied on those constructions in denying Intel's petition. *See Intel Corp. v. XMTT, Inc.*, No. IPR2020-00145, 2020 WL 2562752 (P.T.A.B. May 20, 2020). Intel appealed to the Federal Circuit, which affirmed the Board's decision on the basis of judicial estoppel.

While the appeal was pending, the parties filed a joint supplemental claim construction brief before this Court. The Federal Circuit issued its decision before the Court ruled on the parties' supplemental constructions, and Intel subsequently asked this Court to adopt the Board's constructions. Intel also proposed constructions of

several terms for the first time, including but not limited to "serial processor" and "parallel processor." XMTT opposed the proposed constructions, arguing that the terms' plain language was sufficient.[3] The Court agreed with XMTT and denied Intel's request for a supplemental claim construction order, finding that Intel "offer[ed] no . . . discussion of why it contends the plain language is insufficient." *XMTT II*, 2022 WL 2904308, at *7.

On December 22, 2022, both parties filed combined summary judgment and Daubert motions.

Discussion

Summary judgment is appropriate if the moving party "shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a). Because the parties have filed cross-motions for summary judgment, the Court "view[s] the facts contained in each motion in the light most favorable to the nonmoving party." *Columbia Gas Transmission, LLC v. 1.01 Acres*, 768 F.3d 300, 309 (3d Cir. 2014). "[A] grant of summary judgment of noninfringement is proper when no reasonable factfinder could find that the accused product contains every claim limitation or its equivalent." *Medgraph, Inc. v. Medtronic, Inc.*, 843 F.3d 942, 949 (Fed. Cir. 2016).

The patent infringement analysis has two steps. "The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Duncan*

[3] In reviewing the prosecution history, the Court noted that "XMTT has consistently argued that the terms need not be construed" and that "XMTT's primary argument has always been that construction is not necessary." *XMTT II*, 2022 WL 2904308, at *9, 13.

Parking Techs., Inc. v. IPS Group, Inc., 914 F.3d 1347, 1360 (Fed. Cir. 2019). These two steps are not always strictly sequential, however, and "[d]istrict courts may engage in a rolling claim construction, in which the court revisits and alters its interpretation of the claim terms as its understanding of the technology evolves." *Jack Guttman, Inc. v. Kopykake Enters., Inc.*, 302 F.3d 1353, 1361 (Fed. Cir. 2002).

A. Claim construction

Although the Court previously declined to construe the term "serial processor," claim construction is necessary at this stage because the parties now dispute the plain meaning of that term. "A determination that a claim term 'needs no construction' or has the 'plain and ordinary meaning' may be inadequate *when a term has more than one 'ordinary' meaning* or when *reliance on a term's 'ordinary' meaning does not resolve the parties' dispute*." *O2 Micro Int'l, Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (emphasis added). Courts "are not (and should not be) required to construe every limitation present in a patent's asserted claims[,]" and claim construction is not warranted when "th[e] disputed issue was the proper application of a claim term to an accused process rather than the scope of the term." *Id.* at 1363 (citing *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001)). When "the parties actively dispute[] the scope" of certain claim terms, however, it is legal error to "determin[e] only that the terms should be given their plain and ordinary meaning" and "[leave] this question of claim scope unanswered." *Eon Corp. IP Holdings LLC v. Silver Spring Networks, Inc.*, 815 F.3d 1314, 1319 (Fed. Cir. 2016).

XMTT contends that claim construction is unnecessary because the parties'

dispute is a "factual disagreement regarding the plain and ordinary meaning of unconstrued terms." Pl. XMTT's Br. in Opp. to Intel's Mot. for Summ J. ("XMTT Resp.") at 6. This argument is unpersuasive. Although XMTT recognizes that Intel defines a "serial processor" as a "processor that executes instructions one at a time, in a sequential manner," it seems to argue that serial processors "execute programs having a sequential, program order and retire instructions according to that sequential program order." *Id.* at 6, 15. XMTT relies on statements by its infringement expert, Dr. Thomas Conte, who asserts that Intel's "incorrect definition . . . would exclude essentially every known processor at the time of the invention and decades prior." XMTT Resp., Ex. 9, Reply Expert Report of Dr. Thomas M. Conte ("Conte Reply Report"), at ¶ 73. Given that the parties do not agree on what the term "serial processor" includes and instead each offer their own definition, this is a case in which "reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *O2 Micro*, 521 F.3d at 1362.

XMTT attempts to avoid claim construction by arguing that Intel's definition is an overly narrow *application* of the plain meaning of "serial processor." XMTT does not explain, however, how Intel's proposed definition—a "processor that executes instructions one at a time, in a sequential manner"—is an application of XMTT's own definition.[4] Instead, XMTT points to various parts of Dr. Conte's reply report in which he

[4] At oral argument held on February 8, 2023, XMTT was not entirely clear about the plain meaning of the term "serial processor." When asked if a "serial processor" is "a processor that executes programs having a sequential, program order and retires instructions according to that sequential program order"—the definition XMTT appeared to provide in its response to Intel's motion for summary judgment—counsel for XMTT initially disputed that definition. Upon further questioning, counsel told the Court that the definition is "fairly close" to that and was "generally the argument that Dr. Conte is making." The official transcript for that hearing has not yet been requested or prepared.

disputes Intel's experts' analysis. XMTT then cites two nonprecedential district court decisions for the proposition that disagreements between experts turns this question into a factual dispute for the jury. Neither of those decisions is persuasive; the Federal Circuit has issued precedential decisions holding otherwise in *O2 Micro* and *Eon Corp*. Similarly, Federal Circuit precedent precludes XMTT's argument that it is appropriate for the jury to decide whether a serial processor executes software programs or instructions and whether "execution" of a software instruction covers "retirement" of the instruction. *See Eon Corp*, 815 F.3d at 1319 (holding that "the crucial question [of] whether . . . the terms should not be construed so broadly as such that they covered" certain products is a "question of claim scope" for the court to decide). The Court therefore concludes that claim construction is necessary at this stage.

1. Legal standard

The construction of a patent is a question of law for the Court. *Markman v. Westview Instrs., Inc.*, 517 U.S. 370, 387-88 (1996). "[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004). During claim construction, a court is to construe the words of a claim in accordance with their "ordinary and customary meaning," namely "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005). Sometimes, the meaning of a term is not immediately apparent, and a court will need to look to other sources to determine "what a person of skill in the art would have understood disputed claim language to mean." *Innova*, 381 F.3d at 1116. These sources include "the words of the

claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *Id.*

Claim construction begins by considering the words of the claim. *Takeda Pharm. Co. v. Zydus Pharms. USA, Inc.*, 743 F.3d 1359, 1363 (Fed. Cir. 2014). "The claims, of course, do not stand alone." *Phillips*, 415 F.3d at 1315. They are part of a larger document, including the specification. *Id.* Consequently, claims "must be read in view of the specification, of which they are a part." *Id.* In some situations, the specification "may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1317. And in other situations, the specification may show a disclaimer of claim scope, which is likewise dispositive. *Id.* As a general rule, however, it is inappropriate to confine the claims to the specific embodiments of the invention described in the specification. *Id.* at 1323. That said, the distinction between using the specification to help interpret a claim and importing limitations from the specification into the claim "can be a difficult one to apply in practice." *Id.*

In certain circumstances, a court may also rely on evidence extrinsic to the claim, "which 'consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.'" *Id.* at 1317 (quoting *Markman*, 52 F.3d at 980). But extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Id.* (internal quotation marks omitted). As a general rule, it is only where the intrinsic evidence is ambiguous that a court may rely on extrinsic evidence to construe a claim term. *See,*

e.g., *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1360 (Fed. Cir. 2013).

2. "Serial processor"

a. *XMTT's proposed construction:*

i. "a processor that executes programs having a sequential, program order and retires instructions according to that sequential program order"

b. *Intel's proposed construction:*

i. "a processor that executes instructions one at a time, in a sequential manner"

c. *The Court's construction:*

i. "a processor that executes instructions one at a time, in a sequential manner"

This case turns on the meaning of the term "serial processor" in XMTT's two patents. The patents claim "a serial processor adapted to execute software instructions in a software program primarily in parallel." '388 patent at 13:52–53.[5] The parties proposed the above constructions to clarify what constitutes a "serial processor" in this context. The main points of disagreement are (1) whether a serial processor is any processor that can execute serial programs or only those processors that execute

[5] Although the '879 patent uses slightly different language, neither party contends that the two patents cover different serial processors. *See* '879 patent at 13:64–65 (claiming "a serial processor *to execute instructions* in a *computing program* primarily in serial") (emphasis added).

software instructions serially, and (2) whether "execution" encompasses a step the parties refer to as "retirement." The Court addresses each of these disputes in turn.

a. Programs or instructions

The construction the Court adopts—"a processor that executes instructions one at a time, in a sequential manner"—is more consistent with the patents' claim language and specifications than the construction proposed by XMTT. The parties do not dispute that a serial processor must be different from a parallel processor, as "different claim terms are presumed to have different meanings." *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008). Yet whereas the Court's construction is clear that serial processors are only those processors that execute software instructions sequentially, XMTT's construction would elide the distinction between serial and parallel processors as established by the claims and specifications. If a serial processor is—as XMTT contends—any processor that executes a serial program, then any individual thread control unit (TCU) would also be a serial processor because "all TCUs independently execute a serial program in parallel." '388 patent at 10:42–43; '879 patent at 10:63–64. The '879 patent states, however, that "each *parallel processor* . . . comprises *a thread control unit* to execute instructions in the program," '879 patent at 15:17–19 (emphasis added),[6] and counsel for XMTT explained at oral argument that TCUs are characteristic of the parallel processors in the accused

[6] The '388 patent uses similar language, claiming that "the plurality of parallel processors comprise a plurality of thread control units adapted to execute instructions in the software program." '388 patent at 14:63–65. The '388 patent also notes that "[e]ach parallel processor may include multiple thread control units (TCUs). These may be clustered together to perform parallel processing." *Id.* at 7:26–28.

products. It is therefore unclear what kind of processor—if any—could be a parallel processor if the Court were to adopt XMTT's proposed construction.[7] Such a construction cannot be appropriate given that courts must interpret claims "with an eye toward giving effect to all terms in the claim." *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006).[8]

The prosecution history also supports a narrower construction of the term than XMTT proposes. If the Court were to adopt XMTT's construction that a processor only needs to execute a serial program to be a "serial processor," then any processor that executes both serial and parallel programs could also be a serial processor. Yet XMTT

[7] At best, XMTT argues that it is not "collapsing the distinction between the claimed 'serial processor' and plurality of parallel processors'" because Dr. Conte asserts that the serial processors in the CPU have different functionality than the parallel processors in the GPU. XMTT Resp. at 17–18. Yet Dr. Conte's assertions regarding the functionality of these specific *Intel* products are not relevant on how the Court construes the general term "serial processor" in *XMTT's* patents. *See Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1310 n.10 (Fed. Cir. 2006) (Although a court can "consider the accused device when determining what aspect of the claim should be construed[,]" "[a] claim is construed in the light of the claim language . . . *not* in light of the accused device.") (internal citation and quotation marks omitted) (emphasis in original). Regardless of the accused products' functionality, under XMTT's proposed construction a TCU—which the patents describe as part of the parallel processor—would also be a serial processor because it executes a serial program.

[8] XMTT also contends that a processor is a "serial processor" if any individual "core"—which it does not define, but which appears to be a component of the processor—executes software instructions or programs serially. Yet the accused products comprise multiple cores, and the Intel products that XMTT concedes are "parallel processors" also comprise of multiple TCUs that execute serial programs. Construing a "serial processor" as any processor with components that execute instructions or programs serially would thus render the term "parallel processor" in the patents meaningless, as any such processor would be a serial processor because they contain TCUs. Because "the general assumption is that different terms have different meanings[,]" *Symantec Corp. v. Computer Assocs. Int'l, Inc.*, 522 F.3d 1279, 1289 (Fed. Cir. 2008), the Court cannot appropriately construe a "serial processor" as any processor with a "core" that executes instructions or programs in serial.

itself argued during *inter partes* review that "[a] processor that switches back and forth between serial and parallel processing depending on the instructions that are fed to it by a particular software program is *neither a serial processor or a parallel processor* in the context of the '388 patent" and that the '388 patent specification "provides specific examples of hardware and software differences between serial and parallel processors." Intel's Resp. Br. in Opp'n to XMTT's Summ. J. and Daubert Mot. ("Intel Resp."), Ex. 7, Patent Owner's Sur-Reply, at 5, 2 (emphasis added). XMTT also noted that the specification "describes the different ways in which the 'serial process' [is] *designed to execute instructions 'primarily in serial,'* versus the 'parallel processors' which are designed to execute instructions 'primarily in parallel,'" *id.* at 3 (emphasis added), and one of its experts stated in a supporting declaration that the '388 patent "uses a system in which the *serial processors are specialists designed to perform serial computing* and the parallel processors are specialists designed to perform parallel computing." *Id.*, Ex. 2, Decl. of Professor Murali Annavaram, at 32 (emphasis added). In light of these statements, the Court cannot appropriately adopt a construction of the term "serial processor" based on the type of software program the processor executes, as courts "must look at the ordinary meaning in the context of the written description and prosecution history." *Univ. of Mass. v. L'Oreal S.A.*, 36 F.4th 1374, 1379 (Fed. Cir. 2022) (internal citations and quotation marks omitted).

b. Execution and retirement

The parties also dispute whether a processor "retires" a software instruction when it executes that instruction. Neither party proposes a construction of the term "execute," but XMTT contends that execution also encompasses "fetching" and

"retiring" the instruction. In particular, XMTT seems to define "retirement" as "produc[ing] correct results according to a sequential program order." XMTT Resp. at 13. Intel argues that retirement is separate from execution. Because the parties do not agree about what the term "execute" encompasses, the Court cannot "[leave] this question of claim scope unanswered." *Eon Corp.*, 815 F.3d at 1319.

XMTT does not point to any intrinsic evidence supporting its position but instead relies on Dr. Conte's reports and deposition testimony. "When the intrinsic evidence is silent as to the plain meaning" of the term "execute, it is entirely appropriate for [the Court] to look to dictionaries or other extrinsic sources for context—to aid in arriving at the plain meaning of the term." *Helmsderfer*, 527 F.3d at 1382. Yet "[e]xpert testimony, in particular, is less reliable because it 'is generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence[,]'" and "conclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court." *SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1195 (Fed. Cir. 2013) (quoting *Phillips*, 415 F.3d at 1316). For this reason, expert testimony "may not be used to vary or contradict the claim language," and "opinion testimony on claim construction should be treated with the utmost caution, for it is no better than opinion testimony on the meaning of statutory terms." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584, 1585 (Fed. Cir. 1996).

The '388 and '879 patents both reference "execution" of software instructions on multiple occasions, but there is no discussion or mention of "retirement" at any point in the claims or specifications. XMTT argues that this is because execution was understood to encompass retirement, pointing to statements by Dr. Conte in his reports

that "[r]etirement is the stage where . . . the instruction completes execution" and "an instruction's 'results' happen in serial, in the correct program order, at retirement." XMTT Resp., Ex 1, Expert Report of Dr. Thomas M. Conte ("Conte Report") ¶ 180; Conte Reply Report ¶ 29. Dr. Conte also testified that "[t]he [micro-operations] are reordered, and then from the programmer's point of view, the original instructions are sequentially executed in the program order." Def. Intel's Opening Br. in Supp. of Mot. for Summ. J. ("Intel Opening Br."), Ex. 10, Transcript of Thomas M. Conte, Ph.D. (Conte Dep. Tr.) at 141:7–10. These statements seem to suggest that Dr. Conte considers execution to encompass retirement.

Yet Dr. Conte's other statements indicate otherwise. During his deposition, Dr. Conte explained that completing an instruction is "not the same thing as [retiring the instruction]" because "[i]t is the stage that happens before retirement" and that "[w]hen you are done calculating the result, that's when you complete the instruction." *Id.* at 153:24–154:1, 155:4–6. Dr. Conte also agreed that an instruction "is complete when it leaves the execution stage," which occurs before "the end of the state update stage, [when] the instruction is retired." *Id.* at 155:17–22; *see also id.* at 143:12–19 (agreeing that "Intel's CPU cores execute [micro-operations] in parallel and out of order *at the execution stage*, and *in the state update stage, reorder and retire* the micro-operations in order.") (emphasis added).

The documentary evidence cited by the parties' experts also suggests there is a distinction. Dr. Conte cited a "documentation for the [Out-of-Order] cluster" in his initial report to support his conclusion that execution includes retirement. Conte Report ¶ 179. That document states, however, that "[t]he Out-of-Order (OOO) cluster is responsible

for *dispatching [micro-operations] for execution out of program order* . . . and for marshaling them back into program order *for retirement*," that "*[a]fter execution*, [the micro-operations] write their results," and that "[t]he *executed* [micro-operations] are retired in the original program." *Id.* (emphasis added).[9] Rather than showing that retirement is a part of execution, this document appears to support the conclusion that a processor executes an instruction or micro-operation before retiring it. Another Intel document cited by Dr. Conte similarly includes a diagram indicating that "[instruction] fetch," "decode and resource allocation," and "execution units" are separate from "retirement/writeback." *Id.* ¶ 179. This is consistent with a document which—as Intel's expert Dr. Tor Aamodt notes—the '388 and '879 patents both cited, and that document shows "execute" and "instruction fetch" as separate stages. XMTT Resp., Ex. 2, Expert Report of Dr. Tor Aamodt ("Aamodt Report"), ¶ 221. The Court finds these documents—which, unlike expert reports and testimony, were not "generated at the time of and for the purpose of litigation," *SkinMedica,* 727 F.3d at 1195 (internal citation omitted)—more reliable than Dr. Conte's conflicting reports and deposition testimony.[10] Because "opinion testimony on claim construction should be treated with the utmost

[9] Intel contends that "micro-operations" are distinct from "instructions," but both Dr. Annavaram and Dr. Conte state otherwise. *See* Conte Dep. Tr. at 112:7–16; Intel Opening Br., Ex. 35, Parallel Computer Organization and Design, at 89.

[10] XMTT contends that Dr. Aamodt's infringement report also supports its position on this issue, but that is not the case. Dr. Aamodt states that "[i]f we take the term 'execute' to mean the computation of an instruction's result is produced from its inputs, the accused CPU cores do not execute instructions 'primarily in serial.'" Aamodt Report ¶ 221. Dr. Conte references this statement in asserting that an instruction's results happen at retirement, but as discussed previously, this contradicts Dr. Conte's testimony that "[w]hen you are done calculating the result, that's when you complete the instruction" and that completion occurs before the "state update stage" and retirement. Conte Dep. Tr. at 155:4–6, 17–22.

caution" even in the best cases, *Vitronics*, 90 F.3d at 1585, the Court adopts the construction better supported by the non-testimonial evidence and concludes that "execution" does not encompass "retirement."

For these reasons, the Court declines to adopt XMTT's construction of the term "serial processor" and instead construes the term as "a processor that executes instructions one at a time, in a sequential manner."

B. Infringement

The claims in both the '388 and '879 patents include the term "serial processor." As noted above, the Court has construed "serial processor" to be a processor that executes software instructions sequentially. Intel contends that it is entitled to summary judgment because no reasonable jury could find that the accused products—Intel's CPUs—are serial processors under this construction. "[A] grant of summary judgment of noninfringement is proper when no reasonable factfinder could find that the accused product contains every claim limitation or its equivalent." *Medgraph*, 843 F.3d at 949.

XMTT contends that there is a genuine factual dispute regarding whether Intel's CPUs are serial processors. It asserts that (1) a processor can be a serial processor based on the actions of a single core and that (2) retirement is part of execution. Neither argument precludes a grant of summary judgment because the Court has rejected both these contentions as a matter of claim construction. *See* sections A.2.a at 11 n.8, A.2.b, *supra*. XMTT does not dispute that the accused CPUs have multiple cores that execute instructions and perform "simultaneous multi-threading" or "Hyper-Threading," and both Dr. Conte and XMTT's founder Dr. Vishkin stated that those features indicate parallel processing. *See* Intel Opening Br., Ex. 33, Pl. PACT XPP

Schweiz AG's Concise Stat. of Material Facts ¶ 16 (citing Dr. Conte's report that stated "a *multi-core CPU is designed to execute software instructions at the same time* (in parallel) in more than one core" and "a software program can be broken down into independent blocks or 'threads' and executed across the multiple cores in order to allow fast, parallel processing") (emphasis in original); Conte Dep. Tr. at 126:22–127:1 (agreeing that "the Accused Products have instruction-level parallelism" at the "micro-operation" level); Intel Opening Br., Ex. 11, Transcript of Uzi Vishkin, at 149:6–9 (agreeing that "as an example simultaneous multi-threading is a technique for parallel processing").[11] Consequently, it is not genuinely disputed that neither the CPUs in the accused products nor their cores are processors that "that execute[] instructions one at a time, in a sequential manner."

Lastly, XMTT argues that even if the accused processors are not literally serial processors, they do the equivalent of executing in serial such that Intel may be liable under the doctrine of equivalents. Not so. Under Federal Circuit precedent, there can be no infringement under the doctrine of equivalents if the "theory of equivalence would vitiate a claim limitation." *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1160 (Fed. Cir. 1998). Courts have "refused to apply the doctrine in other cases where the accused device

[11] Aside from Dr. Conte's statements about execution and retirement, XMTT contends that there is a genuine factual dispute because of Dr. Conte's testimony that "Hyper-Threading" involves "executing each of [multiple unrelated threads] as a serial stream of instructions" and "us[ing] those to execute two processes on the same processor." Conte Dep. Tr. 188:20–189:5. Yet this statement does not dispute that the accused products executed multiple threads. To the extent that Dr. Conte is asserting—without further support or explanation—that executing multiple threads or instructions is serial processing if those threads or instructions are "unrelated," "[c]onclusory expert assertions cannot raise triable issues of material fact." *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 1001 (Fed. Cir 2008).

contained the antithesis of the claimed structure," *Planet Bingo, LLC v. GameTech Int'l, Inc.*, 472 F.3d 1338, 1345 (Fed. Cir. 2006), and "two elements likely are not insubstantially different when they are polar opposites." *Brilliant Instruments, Inc. v. GuideTech, LLC*, 707 F.3d 1342, 1347 (Fed. Cir. 2013). In this case, the accused products execute instructions in parallel because they are multi-core processors and each processor performs "simultaneous multi-threading." Executing multiple instructions at the same time is the antithesis of the serial processor claimed by the patents, which "executes instructions one at a time, in a sequential manner," and thus the doctrine of equivalents cannot apply here.

XMTT contends that the accused products are "insubstantially different" from the claimed serial processor because they retire instructions sequentially. This requires assuming that retirement includes execution, however, and the Court has already rejected that construction. *See* section A.2.b, *supra*. Because execution means "execution" and not "execution and retirement," there is no merit to XMTT's argument that the accused products execute instructions in the same "way" as the claimed serial processor because they retire instructions sequentially. XMTT's function-way-result analysis therefore fails to support a claim for infringement under the doctrine of equivalents, as it has at most shown a similarity in the "*result* achieved" but not the "*means* by which function is performed." *Lear Siegler, Inc. v. Sealy Mattress Co.*, 873 F.2d 1422, 1425 (Fed. Cir. 1989) (emphasis in original). Intel is thus entitled to summary judgment with respect to infringement of the '388 and '897 patent claims.

Conclusion

For the foregoing reasons, the Court grants Intel's motion for summary judgment

[dkt. no. 340] and denies all other motions [dkt. nos. 341, 343, 396] as moot.[12] The Court directs the Clerk to enter judgment in favor of the defendant and against the plaintiff.

Date: February 22, 2023

MATTHEW F. KENNELLY
United States District Judge

[12] On February 8, 2023, attorney John Desmarais filed a motion to appear pro hac vice on behalf of Intel [dkt. no. 396]. The Court denies this motion as moot.