Case No. 23-2007, Case No. 23-2095

United States Court of Appeals for the Federal Circuit

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC, STATE OF IDAHO,
Plaintiffs-Appellees

v.

LONGHORN IP, LLC,
Defendant-Appellant

Case No. 23-2007: Appeal from the United States District Court for the District of Idaho in No. 1:22-cv-00273-DCN, Judge David C. Nye.

KATANA SILICON TECHNOLOGIES LLC,
Plaintiff-Appellant

v.

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC, STATE OF IDAHO,
Defendants-Appellees

Case No. 23-2095: Appeal from the United States District Court for the District of Idaho in No. 1:22-cv-00282-DCN, Judge David C. Nye.

CORRECTED OPENING BRIEF OF APPELLANTS KATANA SILICON TECHNOLOGIES LLC AND LONGHORN IP, LLC

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February 22, 2024

EXEMPLARY PATENT CLAIMS

Claim 1 of RE38,806 patent

1. A semiconductor device including a stacked package structure and a chip size package structure, comprising:
an insulating substrate including a wiring layer having electrode sections;
a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first insulating adhesion layer; and
a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second insulating adhesion layer;
each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

Claim 1 of 6,352,879 patent

1. A method of manufacturing a semiconductor device comprising:
(a) forming a first adhesion layer on a back surface of a first wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;
(b) producing separate first semiconductor chips from said first wafer by dicing;
(c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer;
(d) forming a second adhesion layer on a back surface of a second wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;
(e) producing separate second semiconductor chips from said second wafer by dicing; and
(f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip.

Claim 11 of 6,731,013 patent

11. A semiconductor device comprising:
an insulating substrate;
a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;
a land section, provided on the insulating substrate, for an external connection terminal;
wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section;
a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and land section;
a semiconductor chip mounted on the insulating substrate;
a bonding wire section for making electrical connection between the terminal section and the semiconductor chip;
a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section; and
a conductive member, provided on the land section, for connecting the semiconductor chip to outside.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 2023-2007

Short Case Caption Micron Technology Inc. v. Longhorn IP, LLC

Filing Party/Entity Longhorn IP, LLC

Instructions:

1. Complete each section of the form and select none or N/A if appropriate.
2. Please enter only one item per box; attach additional pages as needed, and check the box to indicate such pages are attached.
3. In answering Sections 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance.
4. Please do not duplicate entries within Section 5.
5. Counsel must file an amended Certificate of Interest within seven days after any information on this form changes. Fed. Cir. R. 47.4(c).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 2/22/2024

Signature: /s/ Scott W. Breedlove

Name: Scott W. Breedlove

1. Represented Entities. Fed. Cir. R. 47.4(a)(1).	**2. Real Party in Interest.** Fed. Cir. R. 47.4(a)(2).	**3. Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3).
Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities. ☑ None/Not Applicable	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities. ☐ None/Not Applicable
Longhorn IP, LLC		Tanit Ventures Inc.

☐ Additional pages attached

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

☐ None/Not Applicable ☐ Additional pages attached

Nathan I. Cox, (formerly Carter Arnett PLLC)	Daniel L. Schmid (formerly Carter Arnett PLLC)	Keely E. Duke, Duke Evett, PLLC
Seth Lindner (formerly Carter Arnett PLLC)	E. Leon Carter, Carter Arnett PLLC	Bradley D. Liddle, Carter Arnett PLLC
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5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

☑ Yes (file separate notice; see below) ☐ No ☐ N/A (amicus/movant)

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). **Please do not duplicate information.** This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

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UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF INTEREST

Case Number 2023-2095

Short Case Caption Katana Silicon Technologies LLC v. Micron Technology Inc

Filing Party/Entity Katana Silicon Technologies LLC

Instructions:

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TABLE OF AUTHORITIES

Cases

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TABLE OF ABBREVIATIONS AND CONVENTIONS

Katana	Patent owner and Appellant Katana Silicon Technologies LLC in Case No. 23-2095
Longhorn	Appellant Longhorn IP LLC in Case No. 23-2007
’879 Patent	Asserted U.S. Patent No. 6,352,879 owned by Katana, Appx56–79
’013 Patent	Asserted U.S. Patent No. 6,731,013 owned by Katana, Appx80–114
’806 Patent	Asserted U.S. Patent No. RE38,806 owned by Katana, Appx31–55
Asserted Patents	The’879 Patent, ’013 Patent, and ’806 Patent
Micron	Appellees Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC
Order	Memorandum Decision and Order filed May 3, 2023, Appx1–30
BFA	Bad-faith assertion of patent infringement
Act	Title 48, Chapter 17 of the Idaho Code, entitled “Bad Faith Assertions of Patent Infringement”
BFA bond	A bond under a state’s BFA statute
	In quotations, all emphasis is added unless otherwise noted.

I. INTRODUCTION

In the underlying cases, the district court applied a state statute to order an $8 million bond as a precondition to Katana prosecuting its patent case against Micron. The Order addresses a bond motion Micron originally filed in a retaliatory lawsuit in Idaho state court against a Katana affiliate, *Longhorn*. The Order expressly precludes *Katana* from prosecuting its federal infringement case unless and until the $8 million bond is paid. The district court embraced Micron's presumed intent in seeking the bond that Katana would be "scared off" from enforcing its patent rights. Appx1175–1181 (Order Denying Motion to Stay Bond Proceeding) at Appx178. What evidence did the district court consider in determining that Idaho law should effectively preclude Katana from proceeding with its federal case? None. Instead, the district court in Boise decided that the Idaho Act required the massive bond based on mere *allegations* of a BFA leveled by home-town juggernaut Micron.

The Order imposes what appears to be the first BFA bond in American history, and it further appears to present this Court's first opportunity to consider the constitutionality of any state's BFA statute. Such statutes are now common, but the Idaho Act is an outlier in important ways. Indeed, with its uncapped bond provision and express targeting of federal complaints, the Act is arguably the most extreme BFA statute in the country. Appellants submit the Act and particularly its bond provision are unconstitutional and preempted, especially as applied in the Order.

Notably, this case is more egregious than prior preemption cases this Court has considered. There is no underlying antitrust violation or customer interference or other traditional tort here. And not only is there no clear and convincing evidence of bad faith as this Court's precedents would require, the Order cites no evidence at all—just (demonstrably untrustworthy) *allegations* of the disgruntled accused infringer. Yet on the basis of these allegations alone, the Order effectively punishes Katana under state law for petitioning a federal court for a federal remedy.

Given the magnitude of the bond, Micron's economic leverage over the much smaller patent owner, and the procedural posture of these cases, awaiting an appeal following a final judgment in the underlying cases against Katana and/or Longhorn is neither realistic nor just. Appellants submit, therefore, that immediate relief from this Court is both necessary and appropriate.

II. STATEMENT OF RELATED CASES

No other appeals in or from these actions has previously been before this or any other appellate court.

III. JURISDICTIONAL STATEMENT

This appeal is timely. The Order was filed on May 3, 2023, and each of Katana and Longhorn filed its respective notice of appeal on May 25, 2023.

A. Interlocutory Appeal

The Order imposes an unconstitutional bond calculated under Idaho state law by quadrupling estimated fees and costs Micron may incur in Katana's patent case. The chilling effect of the $8 million bond is manifest. And it was ordered below based not on evidence, but on Micron pleadings alone, assumed (wrongly) to be true. Appx28 (applying "a reasonable possibility" standard lower than "the higher 12(b)(6) standard"). Thus, Idaho's scheme would allow patent infringers in Idaho to erect an often insurmountable barrier to federal court for smaller patent owners falsely accused of bad faith. The Order in this case erected just such a barrier. This appeal is therefore ripe at least under 28 U.S.C. § 1292 and the *Cohen* (collateral order) doctrine.

1. This Court Has Jurisdiction Under Section 1292(a)(1) & (c)(1).

Katana has been effectively enjoined from enforcing its federal rights in federal court because of a state statute asserted in a bond motion—filed only in Micron's separate case against Longhorn, a separate company.[1] The Supreme Court

[1] The jurisdictional analysis as to Katana applies equally to Longhorn on the current record. Micron has argued that activities of Longhorn, a Katana affiliate and service provider, are attributable to Katana and that Katana's filing of a federal complaint is attributable to Longhorn. *See* Appx384–408 (Micron Memo. ISO Motion for Bond) at Appx401. Micron also says its BFA claim against Katana was a compulsory counterclaim in Katana's patent infringement suit. Appx150–175 (*Micron v. Longhorn* Complaint) at Appx154 n.2. The Order adopts Micron's argument as an assumption based on Micron's pleadings alone. *See* Appx3–4 & Appx21 (referring to "Longhorn, which allegedly controls Katana"; concluding *Katana's infringement*

recently reiterated that "where an order has the 'practical effect' of granting or denying an injunction, it should be treated as such for purposes of appellate jurisdiction." *Abbott v. Perez*, 138 S. Ct. 2305, 2310 (2018); *see also Matter of Establishment Inspection of Skil Corp.*, 846 F.2d 1127, 1130 (7th Cir. 1988) (holding that an order requiring a manufacturer to allow a government agency to inspect records or else pay $500 per day was literally an injunction for appealability purposes). In *Abbott v. Perez*, the Supreme Court stressed the "valuable purpose" of the "'practical effect' rule": "But if the availability of interlocutory review depended on the district court's use of the term 'injunction' or some other particular language, Congress's scheme could be frustrated." 138 S. Ct. at 2319–20.

If an interlocutory order is not an injunction but has the "practical effect" of one, appellate jurisdiction nevertheless exists under Section 1292 where the order "might have 'serious, perhaps irreparable, consequence'" and can be "'effectually challenged' only by immediate appeal." *Carson v. Am. Brands, Inc.*, 450 U.S. 79, 84 (1981); *see also Gulfstream Aerospace Corp. v. Mayacamas Corp.*, 485 U.S. 271,

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complaint in 2022 was a new assertion *by Longhorn* for purposes of the Act's limitations period). While Micron's position lacks merit (*see* Appx1182–1207 (Longhorn Response to Micron's Motion for Bond) at Appx1200–1202), the Order's assumption of that position means Longhorn and Katana are similarly situated for purposes of appellate jurisdiction. Moreover, because Katana and Longhorn, and the injunction and bond, are addressed "concurrently in a single order," they are in that sense "inextricably linked." *See Murata Mach. USA v. Daifuku Co.*, 830 F.3d 1357, 1361 (Fed. Cir. 2016).

287–88 (1988) ("Section 1292(a)(1) will, of course, continue to provide appellate jurisdiction over orders that grant or deny injunctions and orders that have the practical effect of granting or denying injunctions and have serious, perhaps irreparable, consequence." (cleaned up)).

a. The Order Is Injunctive.

The injunctive nature of the Order is not ambiguous: "Longhorn or Katana ***must*** post a bond of $8 million ***before*** the Katana case (1:22-cv-00282) may proceed further." Appx30. This anti-enforcement injunction was imposed on *Katana* based on a motion for bond filed in state court only against *Longhorn*, and it is not merely a stay or case management order as Micron has argued. The injunction has no stated end date and presents an unacceptable risk of irreparable harm to Katana, the patent owner. *Cf. Andrew v. Am. Import Ctr.*, 110 A.3d 626, 634 (D.C. 2015) ("[G]ranting a stay pending arbitration does have the 'practical effect' of enjoining the party opposing arbitration.") (as cited in *Abbott*, 138 S. Ct. at 2321 n.12). The district court itself, in ordering that Longhorn had to respond to Micron's bond motion without *any* discovery, recognized the presumptive intent of Micron seeking a bond of such coercive magnitude is that Katana "would be scared off" from enforcing its federal patent rights. Appx1178.

b. The Injunction and Bond Are Punitive and Chilling in Their Effect, Requiring Immediate Appeal.

Courts consistently recognize the chilling ("scared off") impact that even much lower bonds have on speech and on enforcement of rights—an impact often giving rise to constitutionality concerns, as it does here. *See, e.g.*, *Am. Target Advert., Inc. v. Giani*, 199 F.3d 1241, 1250 (10th Cir. 2000) ("The chilling impact of the bond upon protected speech outweighs any fraud protection it might provide. We therefore find that the bond/letter of credit provision of the Utah Act is unconstitutional on its face."); *Buchanan v. Sullivan*, No. 8:20-CV-301, 2021 WL 149052, at *4 (D. Neb. Jan. 15, 2021) ("The Court also finds that more than a minimal bond might chill private enforcement of the TCPA, counter to congressional intent."). And the larger and more indeterminate or speculative the bond, the greater the risk of chilling meritorious litigation. *See Azizian v. Federated Dep't Stores, Inc.*, 499 F.3d 950, 960 (9th Cir. 2007) ("[A] Rule 7 bond including the potentially large and indeterminate amounts awardable under Rule 38 [providing for an award of attorneys' fees as a sanction] is more likely to chill an appeal than a bond covering the other smaller, and more predictable, costs on appeal.").

A state could scarcely concoct a larger, more indeterminate bond formula than Idaho's. Its Act stands alone among the many BFA statutes in the country by purporting expressly to make "unlawful" the inclusion of certain assertions in a

federal "complaint." Act § 48-1703(1).[2] And it is one of less than a handful of state BFA statutes that provide for a bond to include quadruple the anticipated damages, costs, and attorney's fees, ***with no cap on the bond amount***. Act §§ 48-1707 & 48-1706(1)(b)-(d). *See infra* notes 6-7 and accompanying text.

Here, the bond itself is coercive and punitive—punishing Katana for filing its federal complaint—such that meaningful appellate review must be interlocutory. Micron itself has emphasized that "its [BFA] claims are centered on the Katana Complaint" (Appx1131–1157 (Opp. to Longhorn's Motion to Dismiss) at Appx1139), and in its lawsuit against Longhorn, Micron focused on the filing of that *Katana* complaint (Appx153 & n.1). Moreover, addressing *Erie* considerations, the district court reasoned that "the bond is not merely procedural—it is a substantive provision that discourages bad-faith patent assertion ***in and of itself***."[3] Appx27. The district court further confirmed the punitive, coercive purpose of the bond when it rejected Longhorn's request for limited discovery to respond to the bond motion on the grounds that any delay in ordering a bond "would be undercutting" the Act "in a

[2] A minority of the states with BFA statutes define "target" broadly enough to include persons who have been sued, but they do not appear expressly to regulate the contents of a (federal court) "complaint" as Idaho does. *See, e.g.*, N.C. Gen. Stat. § 75-142; Wash. Rev. Code § 19.350.010; Ind. Code § 24-11-2-5.

[3] What the district court missed is that the bond provision also discourages *good-faith* patent assertions in a federal complaint, in part because the court applied the provision based merely on the accused infringer's allegations, without considering any of the evidence contradicting those allegations.

manner that removes *much of the teeth* from the law." Appx1180. Thus, the bond is being used substantively as a state-law device with "teeth" to discourage enforcement of federal rights, not simply as a procedural tool to provide security for a possible damages award under the Act.

Micron no doubt counts on Katana to fold up its tent and go home rather than face the prospect of years of litigation in Micron's Idaho hometown on Micron's state-law BFA claim seeking quadruple damages, while Katana's affirmative federal-law claim seeking compensation for patent infringement is barred from proceeding absent an $8 million bond. This motivation is particularly apparent given the economic and size disparity between (a) accused infringer Micron—the self-described "Fortune 500 leader" that "spends billions of dollars each year" (No. 2023-2007, ECF No. 16 at 2)—and (b) patent owner Katana—the small company that Micron implies will "bend or break when struck" (*id.* at 4 n.3). Micron's too-apparent strategy is to leverage its economic power and the bond to force Katana to give up its federal rights. The constitutional implications of this risk buttress the irreparable nature of Katana's injury. *Cf. Elrod v. Burns,* 427 U.S. 347, 373–74 (1976) (affirming a preliminary injunction, holding that the "loss of First Amendment freedoms, for even minimal periods of time, unquestionably constitutes irreparable injury"); Fed. R. Civ. P. 23(f) advisory committee note to 1998 amendment (recognizing that an order granting class certification could "force a

defendant to settle rather than incur the costs of defending a class action and run the risk of potentially ruinous liability"). Even if the Order were not considered a literal injunction, interlocutory relief would still be required given this grave risk of irreparable harm and the chilling effect of the Order.

2. This Court Also Has Jurisdiction Under the Collateral Order Doctrine Applied to Bonds, as in Cohen.

Aside from Section 1292 appellate jurisdiction, this appeal is also timely under the collateral-order doctrine set forth in *Cohen v. Beneficial Indus. Loan Corp.*, 337 U.S. 541 (1949). *Cohen* itself involved a litigation bond as a precondition to bringing a suit. At issue here is the Idaho district court's power to order a bond at all, which is a classic issue for interlocutory appeal, especially given the magnitude of the bond. *See Donlon Indus., Inc. v. Forte*, 402 F.2d 935, 936 (2d Cir. 1968) (reciting "familiar law" that interlocutory orders granting applications for security are appealable "when the appeal challenges the court's power"); *see also In re U.S. for Use & Benefit of St. Paul A. M. E. Church Hous. Corp.*, 541 F.2d 463, 464 (4th Cir. 1976) ("An order requiring or refusing to require the posting of security during the pendency of the litigation is 'collateral' and is appealable under the doctrine of *Cohen*."). And as in *Cohen*, the "order of the District Court did not make any step toward final disposition of the merits of the case and will not be merged in final judgment. When that time comes, it will be too late effectively to review the present order." 337 U.S. at 546. Micron has argued the Order is not "completely separate

from the merits" as *Cohen* requires because the bond requirement considers the ultimate merits question of bad faith. No. 2023-2007, ECF No. 16 at 15. But the Order was based purely on Micron's *allegations*, and the Supreme Court has rejected reasoning like Micron's in that circumstance. *See Mitchell v. Forsyth*, 472 U.S. 511, 528–29 (1985) ("[T]he Court has recognized that a question of immunity is separate from the merits of the underlying action for purposes of the *Cohen* test ***even though a reviewing court must consider the plaintiff's factual allegations*** in resolving the immunity issue."). Moreover, the Order here takes no more "step toward final disposition of the merits" than did the order in *Cohen*.

"Here it is the right to security [(a bond)] that presents a serious and unsettled question," as opposed to merely "an exercise of discretion as to the amount of security." *Cohen*, 337 U.S. at 547.[4] This Court is being asked to decide as a matter of first impression whether prosecuting a federal patent-infringement claim can be

[4] Some courts hold that bond orders (accompanying preliminary injunctions, for example) are not subject to interlocutory appeal where they involve merely "an exercise of discretion as to the amount of security." *Donlon*, 402 F.2d at 936 (Friendly, C.J.). *Donlon* reasoned that a court's "power" to require a bond, in contrast with matters of discretion about the exact amount of the bond, "is an issue of law, and an appellate decision will settle the matter not simply for the case in hand but for many others—as was notably true with the important issue in *Cohen*." *Id.* at 937. But even where the issue is only one of discretion concerning merely the amount of the bond, interlocutory appeals are permissible when "the bond is both higher than necessary and beyond the plaintiff's financial capacity, and thus inflicts irreparable harm without justification. In such a case the bond order meets the criteria for a collateral order." *Habitat Educ. Ctr. v. U.S. Forest Serv.*, 607 F.3d 453, 456 (7th Cir. 2010) (citations omitted).

conditioned on first posting a massive state-law bond, particularly when the need for the bond is based on nothing more than allegations. The punitive aspect of the bond requirement will have already done its irreparable damage if Appellants had to survive, without being forced into an adverse settlement or bankruptcy, and wait for a final judgment on the merits before they could one day appeal the bond. These circumstances are precisely the sort that *Cohen*'s collateral-order doctrine is designed to address.

Micron has argued that Katana can wait to get a final judgment on the BFA claim and then "appeal at that point" (No. 2023-2007, ECF No. 16 at 13), but this ignores the import of a punitive, coercive bond. Micron's argument that "the bond is not conclusive" likewise rings hollow. *Id*. at 14. The bond conclusively erects a massive barrier to enforcing federal rights. The harm from that barrier is precisely what gives rise to the interlocutory appeal. Perhaps $8 million is a small amount for Micron, but it would likely close the courthouse doors on the majority of patent owners in the United States damaged by Idaho companies' infringement.

For this reason, and because the appeal questions the district court's power to order the bond, the same reasoning and holding of *Cohen* should apply to allow interlocutory appeal of the Order in this case.

3. The Court May Also Exercise Pendent Jurisdiction.

Finally, at the Court's discretion, related issues may also be included in the appeal based on pendent jurisdiction. *Procter & Gamble Co. v. Kraft Foods Glob., Inc.*, 549 F.3d 842, 846 (Fed. Cir. 2008) ("When this court reviews a properly appealable interlocutory order, 'other interlocutory orders, which ordinarily would be nonappealable standing alone, may be reviewed.'"). Where the lower court decides additional issues along with an appealable issue in a single interlocutory order, the appellate court may conclude "those decisions are inextricably linked" and exercise its discretion to consider the additional issues. *Murata*, 830 F.3d at 1361. Thus, Appellants also seek relief from the Order's denial of their motions to dismiss.

B. Alternative Relief Under 28 U.S.C. § 1651

Alternatively, this Court has mandamus jurisdiction under the All Writs Act, 28 U.S.C. § 1651, and because (a) the underlying Katana case is a patent case, (b) the underlying Longhorn case also arises under federal patent law, and (c) the district court precluded Katana's patent case based on Micron's motion filed only in the Longhorn case and addressed Katana and Longhorn concurrently in a single order. 28 U.S.C. § 1295(a)(1); *In re Princo Corp.*, 478 F.3d 1345, 1351–52 (Fed. Cir. 2007) (confirming this Court's exclusive jurisdiction over writs of mandamus where jurisdiction in the district court is based in whole or in part on 28 U.S.C. § 1338, even where the writ substantively does not implicate patent law).

Mandamus is "available to correct a clear abuse of discretion." *In re Apple Inc.*, 979 F.3d 1332, 1336 (Fed. Cir. 2020). In general, three conditions must be satisfied for a writ to issue: "(1) the petitioner must demonstrate a clear and indisputable right to issuance of the writ; (2) the petitioner must have no other adequate method of attaining the desired relief; and (3) the court must be satisfied that the writ is appropriate under the circumstances." *Id*. (citing *Cheney v. United States Dist. Ct.*, 542 U.S. 367, 380–81 (2004)). Given "the unique relationship of this issue to patent law," Federal Circuit law governs. *In re Deutsche Bank Tr. Co. Americas*, 605 F.3d 1373, 1378 (Fed. Cir. 2010) (concluding Federal Circuit law governed "the determination of whether a protective order should include a patent prosecution bar"). Each condition for mandamus is met here.

It is "clear and undisputable" that the district court's order was unconstitutional and otherwise erroneous as a matter of law. And an error on a question of law or application of the law to the facts qualifies as an abuse of discretion. *In re Shared Memory Graphics LLC*, 659 F.3d 1336, 1342 (Fed. Cir. 2011) ("*SMG*") (granting mandamus where the district court misconstrued a joint defense agreement and thereby erroneously granted a motion to disqualify trial counsel). The Order leveraged the state Act to punish patent owner Katana for asserting its federal patent rights in federal court and to erect a substantial barrier to Katana's ability to prosecute its infringement case. And it did so with no evidence

of bad faith at all, much less the clear and convincing evidence of objective and subjective bad faith required to overcome the bar on state-law liability for communications or petitioning activity related to patent infringement. *Globetrotter Software, Inc. v. Elan Comput. Grp., Inc.*, 362 F.3d 1367, 1374–75 (Fed. Cir. 2004). Thus, the district court's error is clear from both the bond provision itself and federal preemption jurisprudence.

Appellants lack "adequate alternative means to obtain the relief sought." *In re Princo*, 478 F.3d at 1353. Katana and Longhorn have been ordered to post not some de minimis bond, but a bond quadruple Micron's estimated patent-litigation-defense fees and costs—a bond understood by the district court to serve a "similar purpose to the damages provisions" and to provide "much of the teeth" of the Act to further "prompt resolution" of the patent infringement claims because Katana would be "scared off" from the case. Appx1178–1180. In other words, the idea is to force Katana to abandon its patent infringement claims. In these circumstances, waiting to appeal a final judgment is inadequate. *See SMG*, 659 F.3d at 1340–42 (granting mandamus, when appeal was unavailable under the collateral-order doctrine, where the district court erred as a matter of law in disqualifying patent owner SMG's counsel-of-choice, and reasoning that the patent owner would be "adversely affected if it is required to wait until after a final adverse judgment to have this issue addressed"); *cf. Sumitomo Copper Litig. v. Credit Lyonnais Rouse, Ltd.*, 262 F.3d

134, 140 (2nd Cir. 2001) (acknowledging that "class certification will effectively terminate the litigation because it will force [defendants] to settle the case rather than risk trial").

Finally, the requested writ is "appropriate under the circumstances." *In re Apple Inc.*, 979 F.3d at 1336. This case would not be the first time that mandamus was warranted concerning an issue of first impression. *See In re Deutsche Bank*, 605 F.3d at 1377, 1382 (noting that "we have granted mandamus review of discovery orders when the petition presented an important issue of first impression," and granting the mandamus petition where the district court improperly evaluated a proposed prosecution bar for a protective order).

IV. STATEMENT OF THE ISSUES

Whether the district court erred by declining to dismiss Micron's BFA claims against Katana and Longhorn and by ordering that Katana's patent infringement claims against Micron cannot proceed until Katana or Longhorn posts an $8 million bond where (i) the Idaho Act and its bond provision on their face and as applied are preempted by federal law, and (ii) Micron's factual allegations failed to state a plausible claim of the minimum objective bad faith required by this Court's preemption decisions.

Whether the district court clearly abused its discretion in granting Micron's motion filed against Longhorn for a multi-million-dollar bond under state law

(i) based primarily on Katana's filing of a patent infringement complaint in federal court, (ii) considering only Micron's allegations assumed to be true under a "reasonable possibility" standard, and (iii) wholly disregarding the contravening evidence and facts filed and argued by Longhorn.

Whether the district court clearly abused its discretion in ordering, based on a Micron motion filed against Longhorn alone, that Katana may not prosecute its patent infringement case against Micron in federal court until Longhorn or Katana posts an $8 million bond pursuant to an Idaho state law purporting to regulate patent infringement complaints filed in federal court.

V. STATEMENT OF THE CASE

A. Katana Identified Micron as an Infringer in 2018 and Initiated License Negotiations.

Katana owns, among other things, certain patents protecting inventions developed by Sharp Corporation in the late 1990s to help shrink semiconductor devices. Longhorn is a sister company that specializes in providing licensing services to its clients, including Katana, and has technical expertise related to semiconductors. Appx1208–1211 (Dec'l of Dr. Soogeun Lee ISO Longhorn's Response to Motion for Bond); Appx1212–1219 (Dec'l of Khaled Fekih-Romdhane ISO Longhorn's Response to Motion for Bond). In 2018, relying on forensic electron-microscope imaging of Micron products, they identified Micron products including flash NAND and DRAM devices infringing Katana's three Asserted

Patents.[5] Appx1216–1218. Through counsel, Katana wrote in the summer of 2018 to notify Micron of the identified infringement, inform Micron of Katana's licensing service agreement with Longhorn, and request a meeting. Appx1216, Appx944–946 (Aug. 22, 2018 First Notice Letter to Micron), Appx999–1001 (Sept. 18, 2018 Second Notice Letter to Micron). At the subsequent meeting in November 2018, Katana met with Micron and presented the seven infringement charts (presentation slide decks) that it had provided to Micron before the meeting. Appx1218–1219; Appx1220-1321 (Initial Presentations to Micron). Following responses from Micron, Katana delivered two additional rebuttal slide decks to Micron in February 2019 highlighting the technical shortcomings in Micron's responses. Appx1219; Appx1329-1379 (Rebuttal Presentations to Micron).

Rather than negotiate in good faith, Micron personnel largely scoffed at the alleged infringement and repeatedly referred back to interim victories Micron had won in patent litigation against Lone Star Silicon Innovations (a different affiliate and client of Longhorn that owned unrelated patents obtained from AMD), which Micron settled in 2019. *See* Appx1219; Appx1322–1328 (Email Chain Regarding Settlement).

[5] Some of these forensic images are excerpted in Katana's Complaint (Appx2340–2380). *See, e.g.*, Appx2349–2351, Appx2360–2363, Appx2370–2374.

B. Katana Sued Micron for Patent Infringement in 2022, and Micron Then Sued Longhorn in Idaho State Court in Retaliation, Relying on the Idaho BFA Statute.

Eventually, Katana had to either forgo its patent rights or file a complaint for patent infringement against Micron; Katana did the latter on March 4, 2022, in the Austin Division of the Western District of Texas. Appx2340.

In addition to answering Katana's complaint, Micron multiplied the proceedings. For its seventh counterclaim to Katana's complaint, Micron asserted its BFA counterclaim under the Idaho Act, alleging that "Katana's claims and demands made in its Complaint . . . violate Idaho Code § 48-1703"—emphasizing in bold-italics the Act's proscription of certain patent infringement assertions in "a complaint." Appx2469–2530 (Micron's Answer and Counterclaims) at Appx2526, ¶ 105. Just one month later, on July 5, 2022, Micron sued Longhorn in Idaho state court, asserting the identical BFA theory against Longhorn as an alleged "alter ego" of Katana, Appx158, even though Micron acknowledges the BFA counterclaim was compulsory in the Katana case, Appx154 n.2. As "Exhibit 1" to Micron's *state-court* complaint, it attached Katana's federal-court patent-infringement complaint (Appx153 n.1); and in its requested relief, Micron sought a "bond posted by Longhorn" to include "Micron's costs to litigate Katana's infringement claims" (Appx175).

1. The Idaho BFA Statute Regulates Federal Patent Litigation.

More than 30 states have passed BFA statutes since 2013, but Idaho's Act is unique in its breadth and remedial scope. To date, neither this Court nor the Supreme Court has addressed the constitutionality of *any* state's BFA statute.

Delving deep into federal matters, the Idaho Act's "Legislative Findings and Intent" section states that the Idaho "legislature seeks to facilitate the efficient and prompt resolution of patent infringement claims." Act § 48-1701(2). It defines "Target" to include "an Idaho person . . . against whom a lawsuit has been filed alleging patent infringement." *Id*. §48-1702(3)(b). Then it provides, "(1) It is unlawful for a person to make a bad faith assertion of patent infringement in . . . a complaint . . . ." *Id*. §48-1703(1). Idaho's BFA statute appears to be the only one in the country that expressly regulates a federal "complaint" in this way.

Rather than following federal law in presuming patent infringement assertions are made in good faith, the Idaho Act lists factors purported to show bad faith and a few factors a court "may consider" as evidence that an assertion was *not* made in *bad* faith. These factors used to prove the negative include factors that are in no way required by federal patent law, including:

- "The person makes a substantial investment in the use of the patent or in the production or sale of a product or item covered by the patent"; and
- "The person has . . . [s]uccessfully enforced the patent, or a substantially similar patent, through litigation."

Act §§ 48-1703(3)(b) & (c)(ii). The Act's remedies include equitable relief, damages, costs, and fees, including attorney's fees, and exemplary damages "in an amount equal to fifty thousand dollars ($50,000) or three (3) times the total of damages, costs and fees, *whichever is greater*." *Id*. § 48-1706(1)(d). Finally, the Act's bond provision states:

> Upon motion by a target and a finding by the court that a target has established a reasonable likelihood that a person has made a bad faith assertion of patent infringement in violation of this chapter, the court shall require the person to post a bond in an amount equal to a good faith estimate of the target's costs to litigate the claim and amounts reasonably likely to be recovered under this chapter, conditioned upon payment of any amounts finally determined to be due to the target. A hearing shall be held if either party so requests. The court may waive the bond requirement if it finds the person has available assets equal to the amount of the proposed bond or for other good cause shown.

Id. § 48-1707. Idaho's Act is one of only four state BFA statutes that provide for a bond that may include quadruple the anticipated damages, costs, and attorney's fees, ***with no cap on the bond amount***.[6] Eleven other states have a BFA bond provision but cap it, almost exclusively at $250,000.[7]

[6] *See* Mont. Code Ann. § 30-13-154; Miss. Code Ann. § 75-24-355, -357; Tenn. Code Ann. § 29-10-103, -104.

[7] *See, e.g.*, Ga. Code Ann. § 10-1-772; Vt. Stat. Ann. tit. 9, § 4198; Me. Rev. Stat. tit. 14, § 8701; S.D. Codified Laws § 37-36-5; N.C. Gen. Stat. § 75-144; N.H. Rev. Stat. Ann. § 359-M:3; Utah Code Ann. § 78B-6-1905; N.D. Cent. Code § 51-36-05; 6 R.I. Gen. Laws § 6-41.1-5; Ind. Code § 24-11-4-1; Mich. Comp. Laws § 446.169.

2. The District Court Allowed Longhorn No Discovery in Response to Micron's State-Law Motion for a $15 Million Bond.

Micron filed its motion seeking a $15-million bond in the state-court case only. Micron's proposed bond represented its "estimated cost of defending against Longhorn's asserted three patents (including IPRs) . . . plus treble damages in three times that amount as permitted by" the Idaho Act. Appx316-319 (Micron's Motion to Post Bond) at Appx318 ¶ 4. Longhorn then removed Micron's case to federal court. Appx133–140 (Notice of Removal) at Appx133. Meanwhile, Katana did not oppose Micron's motion to transfer its patent infringement case to Idaho. Appx 2747–2748 (Nonopposition to Motion for Transfer).

Katana and Longhorn each filed a motion to dismiss Micron's BFA claim/counterclaim, arguing the claim was time-barred, the Act was preempted on its face and as applied, and Micron's allegations failed to state a plausible claim of "bad faith" under Rule 12(b)(6). Appx2770–2772 (Katana's Motion to Dismiss Micron's Seventh Counterclaim); Appx353–355 (Longhorn's FRCP 12(b)(6) Motion to Dismiss). On July 21, 2022, Micron filed its memorandum in support of its bond motion, attaching three declarations and 36 additional exhibits. On July 28, Longhorn moved to stay the bond proceedings pending resolution of its dismissal motion or, in the alternative, to enter a schedule "allowing a brief discovery period before Longhorn is required to file its response brief." Appx1115–1117 (Longhorn's Motion to Stay). Longhorn asked to depose Micron's declarants and pointed out that

a brief stay would not prejudice Micron. Appx1167–1174 (Longhorn's Reply ISO Motion to Stay) at Appx1168–1170. On August 8, however, the district court denied the stay and denied Longhorn any discovery or even additional time to respond to Micron's $15 million bond motion. Appx1175–1181.

In denying the requested stay, the only potential prejudice cited by the district court was Micron's claim that "it is incurring significant legal costs that it would not incur if Longhorn was required to post a bond." Appx1178. The court then offered this telling analysis: "Presumably, Micron's claim is based on the idea that *Longhorn would be scared off from this case (and the related Katana case) if Longhorn was required to post a significant bond.*" *Id.* Far from rejecting Micron's idea, the district court embraced it: "This may be so, and in that situation, Micron would experience serious prejudice if the bond was stayed." *Id.* That, the court reasoned, "cuts in favor of denying the Motion for Stay." *Id*. In other words, the district court sided with Micron's desire to have the bond scare off Katana from enforcing its federal patent rights (with no discovery). The court invoked the apparent will of the Idaho Legislature in support of this state device to regulate federal litigation: "Presumably, the bond was intended to play a role in facilitating 'the efficient and prompt resolution of patent infringement claims.' [Act] §48-1701(2)." Appx1180. Thus, the Order states, even the modest requested stay to allow for a brief discovery period

"would be undercutting" the Act "in a manner that removes *much of the teeth* from the law." *Id*.

Longhorn had to file its response to the bond motion just three days later, which it did, along with two declarations and 13 additional exhibits. Appx1182-1408. Longhorn's evidence included a declaration (Appx1208–1211) from Dr. Soogeun Lee, a Ph.D. semiconductor expert at Longhorn who was involved in identifying and analyzing Micron's products in comparison to the Katana patents and helped to create the seven infringement slide decks presented to Micron at the meeting in November 2018 (Appx1220–1321). Dr. Lee's declaration also identified numerous research and conference papers by Micron personnel that contradicted a non-infringement argument related to "resin" that Micron proffered in its bond motion. Appx1380–1408. Longhorn's evidence also included a declaration from Khaled Fekih-Romdhane, a named inventor on patents related to integrated circuit and semiconductor chip technologies who co-founded Longhorn after many years working for semiconductor manufacturers and then for accomplished patent-licensing firms. He confirmed the corporate structure and relationship between Longhorn and distinct affiliated clients, including Katana. Appx1212–1219. He also explained how Longhorn obtained the forensic images of the accused Micron products and described attempts to negotiate with Micron on behalf of Katana. Appx1218–1219.

Just three days before Longhorn filed this evidence, the court had said in denying discovery: "Any holes that Longhorn finds in Micron's Motion for Bond *and exhibits* that Longhorn desired to ask about in discovery can be used by Longhorn *as evidence* that it is not acting in bad faith." Appx1181. Yet when it came time to rule on the bond motion, the district court considered none of the evidence in determining a bond was required. Appx27-28.

C. In Addition to Denying Appellants' Motions to Dismiss, the District Court Also Ordered the $8-Million Bond Based Solely on Micron's Pleadings, Assumed (Wrongly) To Be True.

Relying solely on Micron's pleadings, and assuming them to be true for purposes of the dismissal motions, the Order stated: "The bottom line is that Micron's complaint pleads enough facts to allow a finding under the statutory factors that Longhorn and Katana acted in bad faith. This is enough affirmative evidence, if accepted as true, to overcome the presumption of good faith." Appx26. In denying the motions to dismiss, the court cited only two allegations to determine that "Micron has pleaded sufficient facts to support a conclusion that Longhorn and Katana's claims are objectively meritless": (1) "Micron pleads that the asserted patents are invalid. First, according to Micron's complaint, the asserted patents have expired"; and (2) "Micron further alleges that these patents are invalid" based on prior art. Appx24. As for the first allegation, contrary to the district court's apparent understanding, expiration is not the same as invalidity; and Katana has never sought

post-expiration damages. *See generally* Appx2340–2380 (*Katana v. Micron* Complaint). Regarding the second allegation, invalidity theories based on prior art are ubiquitous in patent litigation. And the court's only specific prior-art discussion was to recount Micron's allegation that, "as early as 1998, Intel Corporation had developed a semiconductor package with the same key elements as the subject matter of the '879 patent." Appx24. Yet the Order includes no discussion of (a) the fact that the '879 patent itself has a 1998 priority date, (b) the federal-law presumption of patent validity, (c) how the Intel package compares to the specific elements of any '879 patent claim, or (d) how the invalidity argument could be so strong as to demonstrate bad faith by clear-and-convincing evidence.

Next, in granting the bond motion filed against Longhorn only, the district court continued to rely exclusively on the pleadings and disregarded the evidence, determining that a bond was "required":

> Unlike the 12(b)(6) standard, which requires facial plausibility, the Act requires *merely* "a reasonable possibility." Thus, the Court must determine whether there is a reasonable possibility that Longhorn and Katana asserted infringement in bad faith.
>
> Because the higher 12(b)(6) standard has been satisfied, the lower statutory standard is also necessarily satisfied. ***The above analysis on the motion to dismiss serves also to show that, under the Act, a bond is required.***

Appx28. The Order proceeded to consider only one piece of evidence filed by Micron, an AIPLA "report on the cost of defending patent suits," but only for purposes of calculating the *amount* of the bond, apparently based on the cost of

litigating a three-patent suit "from pre-trial through to appeal." Appx28-29. The Order failed to address Longhorn's argument that the "estimate" is overblown for a patent assertion that's supposed to be objectively meritless—and presumably vulnerable to summary judgment and the like—as alleged. Appx1206. Nor did the Order provide any analysis for quadrupling the estimate to include "exemplary damages."

The Order then concluded by denying both Katana's and Longhorn's motions to dismiss and granting Micron's bond motion, ordering: "Longhorn or Katana must post a bond of $8 million before the Katana case (1:22-cv-00282) may proceed further." Appx30. The Order stated that it would be "entered in both cases" but did not explain why Katana would be included in the bond requirement or barred from enforcing its patents when no bond motion was ever filed in its case. *Id*.

The district court failing to consider any evidence and instead taking the accused infringer's allegations at face value were crucial mistakes, especially since those allegations were often conclusory and contradicted by the evidence. For example, in denying the Appellants' motions to dismiss, the court cited only the two deficient allegations discussed above to determine that Micron had pleaded objective meritlessness.[8] Other examples are also revealing. Regarding the more subjective

[8] This is just one example of deficient pleading but clearly an important one since this Court's preemption caselaw imposes the "objectively baseless" ***requirement***, even if the state law doesn't require it. *Globetrotter*, 362 F.3d at 1374–75.

aspects of bad faith, the district court credited Micron's demonstrably false allegations about litigation brought by Lone Star Silicon Innovations, LLC, a different Longhorn affiliate that owned a wholly unrelated portfolio of patents. The court recited Micron's allegations about Lone Star to conclude Micron had pleaded enough facts to indicate "Longhorn and Katana" have filed lawsuits based on a "similar claim" that was meritless. Appx25. Yet no facts were alleged, or exist, to support that Lone Star's claims were "similar," much less that they were filed by "Longhorn and Katana"; and Micron's allegations about the litigation were false and misleading, as Longhorn demonstrated in its response to the bond motion (Appx1190-1192), which the district court did not address. Specifically, Micron alleged that it had obtained a "full dismissal" of Lone Star's case from Judge Alsup, "who criticized Lone Star for having incorrectly stated that it was the sole owner of the asserted patents and having engaged in a 'litigation gimmick.'" Appx159, ¶ 32. In fact, Judge Alsup merely granted a dismissal without prejudice (Appx657–667 (*In re Lone Star Silicon Innovations LLC* Order Granting Motion to Dismiss) at Appx667), which was then vacated by this Court as it criticized Judge Alsup's "litigation gimmick" analysis in *Lone Star Silicon Innovations LLC v. Nanya Tech. Corp.*, 925 F.3d 1225, 1229–34, 1237–38 (Fed. Cir. 2019)—an opinion that is conspicuously absent from both Micron's pleadings and the Order, even though the opinion recognized Lone Star's innocence and criticized Judge Alsup's decision for

ignoring the applicable rule: "It makes little sense here to ignore this rule, even if we could, because the licensee ***[Lone Star] brought suit thinking it was the patentee and turned out to be wrong.***" *Id.* at 1237.

For a more technical example, the Order credits Micron's allegation that "the asserted '806 patent covers a semiconductor device sealed with a resin, which the allegedly infringing Micron product does not contain, being sealed instead with a 'thermoplastic encapsulant,'" and that this was a "critical difference." Appx22-23. Again, though, because the district court simply took the accused infringer's assertion at face value and failed to consider the evidence, the Order overlooked evidence that Micron's products do in fact use resins. Longhorn filed evidence from Micron publications that (1) Micron used epoxy molding compound ("EMC") as a package encapsulant in Micron's NAND and DRAM memory (the accused Micron product is a NAND memory) and (2) "epoxy resin" forms one of the three main parts of EMC. Appx1210-1211, ¶¶ 6-9; Appx1380-1385; Appx1386-1388. Contemporaneous industry usage also connects "thermoplastic encapsulants" and "resin," exemplified by a DuPont brochure from the late 1990s discussing "thermoplastic encapsulation resins." Appx1211, ¶ 10; Appx1389-1408. The district court considered none of this.

Each of Katana and Longhorn noticed an appeal in its respective case on May 25: Case No. 23-2095 and Case No. 23-2007 respectively, now consolidated. Micron

filed a motion to dismiss the appeals, which the parties briefed. This Court denied the motion on December 15, 2023, advising the parties to address the Court's jurisdiction in the merits briefing and directing Appellants to raise in their opening brief any argument they wish to raise under Section 1651. ECF Nos. 16, 21-23.

VI. SUMMARY OF THE ARGUMENT

This appeal concerns what appears to be the first BFA bond in American history. The $8-million Idaho state-law bond precludes a patent owner, Katana, from prosecuting its federal claims for patent infringement. And it does so based on mere *allegations* of bad faith by the accused infringer, home-town juggernaut Micron, in its separate case filed originally in Idaho state court against Longhorn, a Katana affiliate and service provider. The massive bond was purportedly an "estimate" including "exemplary damages"; and it was found to be required based on no *evidence* whatsoever, much less clear and convincing evidence.

Appellants maintain the Idaho Act and bond are unconstitutional and preempted as applied. Importantly, this case is far more egregious than prior preemption cases this Court has considered. Idaho's Act expressly targets federal litigation and badly distorts the balance of rights in patent cases, displacing Congress's chosen calculus of litigation incentives and disincentives. In this case, there are no allegations that Appellants have committed an antitrust violation or interfered with Micron's customers or the like. Indeed, the supposed wrongful

conduct is the patent owner filing its complaint in federal court to recover damages for Micron's past infringement. Period. Thus, the bond is not calculated based on potential lost profits from some Micron customer relationship. No, the bond is simply a quadrupling of Micron's estimated costs to defend the patent case. A state statute, then, is being used to replace federal law's governance of a federal case.

The bond itself is punitive, punishing Katana for filing its federal complaint—without the minimum evidentiary showing required to avoid federal preemption. Micron itself has confirmed that "its [BFA] claims are centered on the Katana Complaint" (Appx1131–1157 (Opposition to Longhorn's Motion to Dismiss) at Appx1139); and, in its lawsuit against Longhorn filed in state court, Micron focused on the Katana complaint, attaching that federal complaint as "Exhibit 1" (Appx153 n.1). Moreover, the district court after removal, in rejecting an *Erie* challenge, reasoned that "the bond is not merely procedural—it is a substantive provision that discourages bad-faith patent assertion ***in and of itself***." Appx27 (also concluding the "bond provision thus serves a similar purpose to the damages provisions"). And previously, the court had rejected Longhorn's request for limited discovery to respond to the bond motion on the grounds that any delay in ordering a bond "would be undercutting" the Act "in a manner that removes *much of the teeth* from the law." Appx1180. Thus, the bond is apparently being used substantively as a state-law

device with "teeth" to discourage certain federal filings, not simply as a procedural tool to provide security for a possible damages award under the Act.

What the district court missed is that the bond provision also discourages *good-faith* patent assertions in a federal complaint, in part because the court applied the provision to require a bond based merely on the accused infringer's allegations. The court identified no evidence, much less clear and convincing evidence, making the required showing of bad faith that could avoid federal preemption. After all, federal law recognizes a presumption that the assertion of a duly granted patent is made in good faith. *Virtue v. Creamery Package Mfg. Co*., 227 U.S. 8, 37–38 (1913). And "this presumption is overcome only by affirmative ***evidence*** of bad faith." *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1369 (Fed. Cir. 1998). Yet the district court did not even purport to consider evidence in deciding a bond was required, instead restricting its analysis to Micron's allegations under a "lower statutory standard" than even Rule 12(b)(6) requires. Appx28.

The option for Katana to post the bond is largely illusory given the magnitude of the bond, as the district court seemed to anticipate. In denying Longhorn any discovery, the court specifically acknowledged (and credited) Micron's intent that "Longhorn [*sic*: Katana]" would be "scared off" from enforcing its patent rights if required to post "a significant bond." Appx1178. Indeed, courts consistently

recognize the chilling impact—often implicating constitutionality concerns—that even much lower bonds have on speech and on enforcement of federal rights.

For these reasons, the court erred in permitting the BFA claim to proceed and abused its discretion in ordering a substantial bond and precluding Katana's infringement suit from otherwise proceeding. Moreover, given the magnitude of the bond, Micron's economic leverage over the much smaller patent owner, and the procedural posture of these cases, awaiting an appeal following a final judgment in the underlying cases against Katana and/or Longhorn is neither realistic nor just.

VII. ARGUMENT

A. Standard of Review

This Court reviews decisions to dismiss complaints under Rule 12(b)(6) de novo. *Zafer Constr. Co. v. United States*, 40 F.4th 1365, 1367 (Fed. Cir. 2022); *see also Burgert v. Lokelani Bernice Pauahi Bishop Tr.*, 200 F.3d 661, 663 (9th Cir. 2000); *United States v. Hampshire*, 95 F.3d 999, 1001 (10th Cir. 1996) ("We review de novo challenges to the constitutionality of a statute.").

Decisions to issue an injunction or to require a bond are generally reviewed for abuse of discretion. *LEGO A/S v. ZURU Inc.*, 799 F. App'x 823, 827 (Fed. Cir. 2020) ("[T]his Court reviews a district court's decision granting a motion for preliminary injunction under an abuse of discretion standard. An abuse of discretion has occurred when the court made a clear error of judgment in weighing relevant

factors or exercised its discretion based upon an error of law or clearly erroneous factual findings.") (cleaned up); *Diouf v. Mukasey*, 542 F.3d 1222, 1234 (9th Cir. 2008) (holding an injunction was an abuse of discretion where it relied on an erroneous premise); *Negrete v. Allianz Life Ins. Co. of N. Am.,* 523 F.3d 1091, 1096 (9th Cir. 2008) (explaining that a district court abuses its discretion if it enters preliminary injunctive relief because of a misapprehension of the law governing the underlying issues in the litigation); *cf. Gen. Elec. Co. v. Joiner*, 522 U.S. 136, 141 (1997) ("We have held that abuse of discretion is the proper standard of review of a district court's evidentiary rulings."). An error on a question of law or application of the law to the facts qualifies as an abuse of discretion. *SMG*, 659 F.3d at 1342 (granting mandamus where the district court misconstrued a joint defense agreement and thereby erroneously granted a motion to disqualify trial counsel).

B. The District Court Erred in Entering the Order.

Micron has no legitimate basis to use state law to punish Katana's petitioning activity in federal court in its effort to enforce its patents against accused infringer Micron. The district court should have dismissed Micron's BFA claim because it fails to state a plausible claim that could satisfy this Court's requirements for the sort of "bad faith" that may avoid preemption. Moreover, the Act on its face creates a statutory scheme that would go so far as to regulate patent litigation itself in a manner

that would undermine federal statutes and rules, would create nationwide non-uniformity in patent cases, and is preempted.

1. Micron's BFA Claim Is Preempted for Failing to State a Plausible Claim of Objective Baselessness.

Micron fails to state a plausible BFA claim that could survive preemption. "A plaintiff claiming that a patent holder has engaged in wrongful conduct by asserting claims of patent infringement must establish that the claims of infringement were objectively baseless." *Globetrotter*, 362 F.3d at 1377. Rather than suggesting objectively baseless claims, Micron's allegations reflect at most Micron's purported disagreements with Katana's infringement analysis and claim construction. These do not amount to plausible allegations of objective baselessness. *See Landmark Tech., LLC v. Azure Farms, Inc*., No. 3:18-CV-1568, 2020 WL 1430088, at *5 (D. Or. Mar. 24, 2020) (holding counterclaim based on Oregon's Anti-Bad Faith Assertion Statute preempted "as pleaded because Defendant has failed to allege facts demonstrating the objective baselessness of Plaintiff's claim"); *Puritan Med. Prods. Co. v. Copan Italia S.p.A*., 188 A.3d 853, 862–63 (Me. 2018) (similar with respect to Maine's statute).

Micron's allegations fail to state a plausible claim that "no reasonable litigant could realistically expect success on the merits" of Katana's infringement claims. *See 800 Adept, Inc. v. Murex Secs., Ltd.*, 539 F.3d 1354, 1370 (Fed. Cir. 2008). In

the district court, Micron listed **six bullet points** purporting to support objective bad faith. Appx1150-1151. None of them satisfies *Iqbal*.

First, Micron criticized one clause in one paragraph of Katana's 40-page Complaint. Pointing out the obvious fact that all three patents had expired by the time Katana's Complaint was filed, Micron found one place where the Complaint erroneously used the phrase "continue to infringe" with reference to Micron products. But fairly read, Katana's Complaint was about past infringement only. Katana did not attempt to seek relief for any ongoing infringement, Appx2378-2379, and Micron did not allege otherwise. Even so, Micron's lead argument was that this stray erroneous phrase—included only in the jurisdictional section of the Complaint—showed "objective bad faith." Appx1150.

Second, Micron asserted objective bad faith because "Longhorn did not allege patent marking in either its pre-suit correspondence or the Katana Complaint, even though pre-suit damages would be severely circumscribed without marking." Appx1150-1151. First of all, Micron's assertion is not plausible because it is disproven by the Katana Complaint itself, which does allege patent marking in its paragraphs 122-123. Appx2378. In any event, "severely circumscribed" damages, whatever Micron may have meant by that, would not indicate that no reasonable litigant could realistically expect success on the merits of Katana's infringement claims.

In its third bullet, Micron relied on its conclusory assertion "that Longhorn's claims regarding the asserted patents are exceptionally weak." Appx1151. But this naked assertion carries no weight under *Iqbal*—particularly not when plausible allegations of objective bad faith, which Micron would have the burden of proving by clear and convincing evidence at trial, are required to avoid federal preemption.

In its fourth, fifth, and sixth bullets, Micron addressed one technical point from each of the three patents-in-suit. Concerning the '806 patent, Micron repeated its argument about the claim element "sealed with a resin," arguing Katana's Complaint "erroneously identified portions of Micron's products as a 'resin' that are not actually 'resin.'" *Id.* Yet Micron's Complaint itself conceded that "Micron's accused products are instead sealed using thermoplastic encapsulants," which do "contain small amounts of resins." Appx166-167, ¶ 66. Micron's argument falls short of meeting the high standard for objective bad faith. *See C.R. Bard*, 157 F.3d at 1369 (explaining "sham litigation requires more than a failed legal theory").

Addressing the '879 patent in its fifth bullet, Micron identified an issue that at best relates to disputed claim construction. Specifically, Micron pointed to claim language in claim 1 "that Longhorn improperly reads inconsistently across the claim," it argued. Appx1151. Putting aside that Micron's argument fails as a matter of law, Micron alleged no facts to make its argument or its allegation plausible. *See*

id. And Micron's theory would again fail under the high federal standard articulated in *C.R. Bard* to avoid preemption.

The same is true about Micron's sixth bullet arguing about the '013 patent. The cited paragraph from Micron's Complaint purported to find a misidentification of a claim element in the forensic images of the Micron product, but such a dispute does not plausibly give rise to a claim of sham litigation. *See id.* (citing Compl. ¶ 81 (Appx170)); *see also Golan v. Pingel Enter., Inc.*, 310 F.3d 1360, 1371 (Fed. Cir. 2002) ("[P]atentees . . . are allowed to make representations that turn out to be inaccurate provided they make them in good faith.").

The district court ignored these arguments from Micron in assessing objective bad faith, instead crediting allegations of invalidity. Specifically, the court cited only two allegations to determine that "Micron has pleaded sufficient facts to support a conclusion that Longhorn and Katana's claims are objectively meritless": (1) "Micron pleads that the asserted patents are invalid. First, according to Micron's complaint, the asserted patents have expired,"[9] Appx24; and (2) "Micron further alleges that these patents are invalid" based on prior art. *Id.* But invalidity allegations based on prior art are ubiquitous in patent litigation. And the court's only specific prior-art discussion was to recount Micron's allegation that, "as early as 1998, Intel

[9] It appears the district court did not appreciate the distinction between expiration and invalidity.

Corporation had developed a semiconductor package with the same key elements as the subject matter of the '879 patent." *Id.* Yet the Order includes no discussion of (a) the federal-law presumption of patent validity, (b) the fact that the '879 patent itself has a 1998 priority date, (c) how the Intel package compares to the specific elements of any '879 patent claim, or (d) how the invalidity argument could be so strong as to demonstrate bad faith by clear-and-convincing evidence.

In short, Micron's allegations of bad faith are supported by nothing more than the typical kind of disputes common to American patent litigation. In contrast, the district court cases Micron relied on reflect application of other states' statutes to egregious factual allegations easily distinguishable from Micron's allegations. Appx1144-1145. And these cases merely underscore that Micron's allegations fall far short of meeting the federal standard. *See NAPCO, Inc. v. Landmark Tech. A, LLC*, 555 F. Supp. 3d 189, 214 (M.D.N.C. 2021) ("Landmark engaged in a pattern of meritless litigation against various entities and has attempted to force quick settlements, based on the in terrorem effect of its demands, without any intent of litigating its claims."); *Triple7Vaping.com, LLC v. Shipping & Transit LLC*, No. 16-CV-80855, 2017 WL 5239874, at *7 (S.D. Fla. Feb. 6, 2017) (holding that Triple7 had sufficiently alleged both objective and subjective bad faith based in part on Triple7's allegation that "S&T's patent assertion is part of a repeated pattern of filing frivolous, cookie-cutter lawsuits and immediately seeking settlement well below the

cost of litigation"). The Complaint in Katana's lawsuit, in contrast, addresses specific claim elements applied to forensic images of certain Micron semiconductor products and bears no resemblance to any prior case finding a plausible claim of a bad faith assertion.

2. Idaho's Act Is Facially Preempted Because It Would Displace Congress's Chosen Calculus of Patent Litigation Incentives and Lead to Stark Nationwide Non-Uniformity.

Of the dozens of BFA statutes passed by states in the last ten years, Idaho's Act goes the furthest. It is unique in its clear intent to regulate litigation in federal court and is among only a few other state BFA statutes with the combination of a bond and uncapped quadruple damages. It also ignores, and would even distort, the presumption under federal law that patent infringement assertions are made in good faith. Ultimately, even after importing into the Act this federal presumption and the requirement to show both objective and subjective bad faith by clear and convincing evidence—which are not otherwise part of the Act—Idaho's statute would effectively displace Congress's chosen calculus of patent litigation incentives for a subset of patent cases in this country.

The Act's "Legislative Findings and Intent" section states that the Idaho legislature seeks to "***facilitate*** the efficient and prompt resolution of patent infringement claims." Act § 48-1701(2). Then it provides, "(1) It is unlawful for a person to make a bad faith assertion of patent infringement in . . . a complaint . . . ."

Act §48-1703(1). Idaho's BFA statute appears to be the only one in the country that expressly regulates a federal "complaint" in this way.

The Idaho statute's findings state that "[p]atent holders have every right to enforce their patents when they are valid and infringed." Act § 48-1701(1)(b). While undoubtedly true, the phrasing highlights a deficiency in the statutory scheme, because a patent holder should not be required to wait for its patent infringement case to be successful to be assured that it will not be subjected to the harsh remedies of a state statute regulating the federal case itself. This Court has emphasized that "a principal purpose of the patent system is to provide innovators with a property right upon which investment and other commercial commitments can be made." *C.R. Bard*, 157 F.3d at 1369. Thus, absent the criteria for truly sham litigation, "the patentee must have the right of enforcement of a duly granted patent, unencumbered by punitive consequences should the patent's validity or infringement not survive litigation"; and "sham litigation requires more than a failed legal theory." *Id*. This is exactly the reason federal law "recognizes a presumption that the assertion of a duly granted patent is made in good faith." *Id.* Stating no such presumption, Idaho's Act lists numerous factors that the court may consider "as evidence that a person has made a bad faith assertion of patent infringement," and these include activity that is acceptable under federal law. *See, e.g.*, Act § 48-1703(2)(b), (c), (i).

Instead of a presumption of good faith, the Idaho statute lists three particular factors that a court "may consider" as "evidence that a person has not made a bad faith assertion of patent infringement." Act § 48-1703(3). In this way, the statutory scheme practically suggests a presumption of bad faith. And of the three "not bad faith" factors, not one of them is required by federal law. Moreover, the second factor discriminates against individual inventors and other persons who do not necessarily "use" the invention or make or sell "a product or item covered by the patent." Act § 48-1703(3)(b). Federal law does not permit such discrimination. The Patent Act states: "A patentee shall have remedy by civil action for infringement of his patent." 35 U.S.C. § 281. And the term "patentee" comprises "not only the patentee to whom the patent was issued but also the successors in title to the patentee." 35 U.S.C. § 100(d); *see also Thermolife Int'l LLC v. GNC Corp.*, 922 F.3d 1347, 1363 (Fed. Cir. 2019) (recognizing "the patent statute does not restrict enforceable patent rights to those who practice the patent"). It would be bad federal policy—and impair the patent marketplace and the incentives to inventors to promote the progress of science—to allow Idaho to subject patent owners to greater risk in patent enforcement simply because they do not make covered products.

As the Supreme Court recognized a century ago, "Patents would be of little value if infringers of them could not be . . . proceeded against in the courts." *Virtue*, 227 U.S at 37–38; *see also* 35 U.S.C. § 281 ("A patentee shall have remedy by civil

action for infringement of his patent."). While Idaho's Act does not expressly preclude federal court suits for patent infringement, as a practical matter its excessively punitive scheme, including the bond provision, risks doing just that for patentees with limited resources. Katana's plight in the face of Micron's efforts to leverage the coercive power of the Act would be only the beginning if the Act could stand.

The Idaho statute goes too far in giving accused infringers mechanisms to effectively block patent owners, especially smaller ones, from seeking redress in federal court. When it comes to patent litigation, federal law already protects against bad-faith assertions, carefully balancing the rights of patentees and accused infringers. *See, e.g.*, 35 U.S.C. § 285 (providing that "[t]he court in exceptional cases may award reasonable attorney fees to the prevailing party" in patent cases); Fed. R. Civ. P. 11(b), (c) (providing courts the ability to sanction parties who bring federal claims "for any improper purpose, such as to harass, cause unnecessary delay, or needlessly increase the cost of litigation"). The more substantial problem historically has been willful patent infringers, which, as here, often have vastly more resources than the patentee. Thus, federal law allows for the possibility of enhanced damages up to treble damages, 35 U.S.C. § 284, generally reserved for "egregious cases typified by willful misconduct." *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93, 109–10 (2016). But Idaho's Act badly distorts the balance of rights in patent

litigation expressly, displacing Congress's "chosen calculus of litigation incentives and disincentives." *Bldg. Innovation Indus., L.L.C. v. Onken*, 473 F. Supp. 2d 978, 986–88 (D. Ariz. 2007) (holding that 35 U.S.C. § 285 impliedly preempted the application of a state fee-shifting statute, and explaining that besides ousting the federal statute, enforcing various state laws on fees in patent-related cases "would also undermine Congress's goal of nationwide uniformity in patent law").

Idaho's Act does nothing to protect patentees from bad-faith infringement but practically presumes bad-faith assertion. On its face, the Act regulates federal petitioning activity (even offering injunctive relief) and creates the *threat* of a punitive bond and substantial liability, including quadruple damages, for activity that is permitted and even incentivized by federal patent laws—i.e., a patent owner (yes, even a small patent owner that isn't selling products) petitioning a federal court in good faith seeking a remedy for a large corporation's patent infringement. This threat risks chilling speech and blocking the federal courthouse doors, particularly for smaller patent owners.

Idaho's Act thereby interferes with federal law, and "any state law . . . which interferes with or is contrary to federal law, must yield." *Free v. Bland*, 369 U.S. 663, 666 (1962). Federal law impliedly preempts state laws that pose an obstacle to the "full purposes and objectives" of Congress. *See Hines v. Davidowitz*, 312 U.S. 52, 67 (1941); *see also Boggs v. Boggs*, 520 U.S. 833, 844 (1997) (explaining that

"[s]tates are not free to change ERISA's structure and balance" and holding that application of state law was preempted where it would "undermine the purpose" of ERISA's mandated survivor's annuity); *Felder v. Casey*, 487 U.S. 131, 138 (1988) (recognizing implied preemption when the state statute "conflicts in both its purpose and effects with the remedial objectives of [42 U.S.C.] § 1983").

Because the Act impedes the vindication of a federal right, it is impliedly preempted. Appellants submit Idaho's Act simply cannot exist alongside U.S. patent laws in our federal system and is preempted in light of the United States Constitution's prohibition on certain laws abridging "the right of the people . . . to petition the Government for a redress of grievances" (First Amendment), *see, e.g.*, *Gen–Probe, Inc. v. Amoco Corp.*, 926 F. Supp. 948, 956 (S.D. Cal. 1996) (agreeing with "the majority of courts who have considered the issue . . . that *Noerr* immunity bars any claim, federal or state, common law or statutory, that has as its gravamen constitutionally-protected petitioning activity"), as well as the Supremacy Clause (Art. IV, para. 2) and the Patent Clause (Art. I, Sec. 8, Clause 8).

C. The District Court Abused Its Discretion by Applying State Law to Order a Punitive, Coercive Bond as a Precondition to Katana Enforcing Its Patents in Federal Court.

Federal law presumes a duly granted patent is valid and its assertion is made in good faith. *Virtue*, 227 U.S. at 37–38. Further, the federal Patent Act provides, "A patentee shall have remedy by civil action for infringement of his patent." 35 U.S.C.

§ 281. And the Federal Rules of Civil Procedure "impose comprehensive, not minimum, pleading requirements." *Klocke v. Watson*, 936 F.3d 240, 247 (5th Cir. 2019). They also provide a mechanism to address federal complaints allegedly filed in bad faith. *See* Fed. R. Civ. P. 11. Thus, if Micron had legitimate concerns about Katana's patent infringement complaint, federal law is well-established and capable to govern them in appropriate balance with the remedial purpose of the Patent Act.

Yet Micron—attaching Katana's federal complaint as "Exhibit 1" to an Idaho state-court lawsuit—turned to Idaho's Act to effectively replace the federal scheme with a one-sided state-law scheme that "conflicts with the Federal Rules by setting up an additional hurdle a plaintiff must jump over to get to trial." *See Abbas v. Foreign Pol'y Grp., LLC*, 783 F.3d 1328, 1334 (D.C. Cir. 2015). Indeed, the hurdle is practically insurmountable given the manner the bond provision was erroneously applied in the Order.

The Order leveraged the *state* Act to punish patent owner Katana for asserting its *federal* patent rights in *federal* court and to erect a substantial barrier to Katana's ability to prosecute its infringement case. And it did so with no evidence, much less the clear and convincing evidence of objective and subjective bad faith required to overcome the bar on state-law liability for communications or petitioning activity related to patent infringement. Thus, the district court's error is clear from both the bond provision itself and federal preemption jurisprudence.

1. The district court applied the Act's bond provision wrongly and unconstitutionally.

Under the Act, no bond should be ordered absent a motion by the target of the patent assertion and "a finding" by the court that a target has established "a reasonable likelihood" that a person has made a bad faith assertion of patent infringement. Act § 48-1707. Yet in this case only, the district court applied a "reasonable *possibility*" standard and, instead of making a "finding" based on evidence, simply assumed all of the accused infringer's allegations were true. Appx27-28.

As written, the Act's bond provision cannot pass muster; but as applied in the Order, it fell woefully short. The court's approach to Micron's bond motion cannot even be squared with the same district court's analysis the last time the issue came up in Idaho. *See Ice Castles v. LaBelle Lake Ice Palace, LLC*, No. 4:18-cv-00571, 2021 WL 3085479, at *6-7 (D. Idaho July 21, 2021) (considering, for example, the evidence at "Dkt. 96-7," stating "the Court cannot wholesale accept [the accused infringer's] interpretation of the facts," and finding bad faith had not been established). Several years earlier, a federal court in Georgia interpreted identical language in the bond provision of the Georgia BFA statute—requiring a finding by the court that "a target has established a reasonable likelihood" of a BFA. *Farmer v. Alpha Techs., Inc.*, No. 1:14-CV-2958, 2015 WL 13777260, at *3 (N.D. Ga. Nov. 18, 2015), *report and recommendation adopted*, No. 1:14-CV-2958, 2015 WL

13777898 (N.D. Ga. Dec. 9, 2015). And likewise in that case, the court considered the evidence and did not rely solely on the accused infringer's pleadings, ultimately concluding a "reasonable likelihood" had not been established. *Id*. Indeed, until the Order in this case, it appears no court in the country had ever ordered a BFA bond at all, much less a massive bond based solely on the accused infringer's pleadings.

The district court therefore erred as a matter of law in applying the Act's bond provision. Preemption jurisprudence did not permit the court to use state law to punish Katana (or Longhorn) for Katana filing its patent infringement complaint in federal court absent evidence—clear and convincing evidence—of bad faith. This Court has emphasized that, absent affirmative evidence of bad faith, "the patentee must have the right of enforcement of a duly granted patent, unencumbered by punitive consequences should the patent's validity or infringement not survive litigation." *C.R. Bard*, 157 F.3d at 1369. This Court has further explained that the requirement for ***objective*** baselessness "rests on both federal preemption and the First Amendment." *Globetrotter*, 362 F.3d at 1377; *see also Virtue*, 227 U.S. at 37–38 ("Patents would be of little value if infringers of them could not be notified of the consequences of infringement, or proceeded against in the courts. Such action, considered by itself, cannot be said to be illegal."). The Order, however, has *already* imposed "punitive consequences" on the patentee, Katana, before it has even had a

chance to exercise its "right of enforcement"—merely because of reckless accusations by the accused infringer.

Indeed, the Order imposes a massive state-law obstacle to enforcement by conditioning such enforcement on payment of an $8-million bond. The coercive, chilling effect of this bond is neither accidental, *see supra* at 22-23, nor constitutional. *Cf. Am. Target Advert.*, 199 F.3d at 1250 ("The chilling impact of the bond upon protected speech outweighs any fraud protection it might provide. We therefore find that the bond/letter of credit provision of the Utah Act is unconstitutional on its face.").[10] The Supreme Court in *Felder v. Casey* considered an exhaustion requirement of Wisconsin's notice-of-claim statute requiring "a dispute resolution system [that] may have much to commend it," but the Supreme Court explained that is a judgment for Congress to make. 487 U.S. at 149. It observed further that state rules may not "impose unnecessary burdens upon rights of recovery authorized by federal laws." *Id*. at 150. As applied in the Order, Idaho's Act poses a formidable obstacle (including "unnecessary ~~burdens") to the most bas~~ic remedial

[10] *See also Azizian*, 499 F.3d at 960 ("[A] Rule 7 bond including the potentially large and indeterminate amounts awardable under Rule 38 [providing for an award of attorneys' fees as a sanction] is more likely to chill an appeal than a bond covering the other smaller, and more predictable, costs on appeal."); *Melaleuca, Inc. v. Hansen*, No. CV07-212-E-EJL, 2008 WL 2788470, at *7 (D. Idaho July 18, 2008) (declining to require Plaintiff to post a bond to cover Defendants' fees and costs in a federal Can-Spam case where Plaintiff had shown "at least some evidence" because "requiring Plaintiff to post a bond when they have brought a claim supported by evidence, may chill private enforcement of Can-Spam").

objective of the Patent Act—to give a patent owner a "remedy by civil action for infringement of his patent." 35 U.S.C. § 281. The Order is therefore preempted.

2. The bond is unconstitutional for the additional reason that the Act is preempted as applied to Micron's theory of the case.

As discussed above, the Act badly distorts the balance of rights in federal patent litigation. The distortion is more pronounced here as Micron admits its BFA claim is "centered on the Katana Complaint." Appx1139; *see also* Appx2526–2528 (alleging Katana's "conduct in filing its Complaint here is unlawful under Idaho Code § 48-1703" and further seeking "injunctive relief" against such conduct and a bond including "Micron's costs to litigate Katana's infringement claims"). The Act does nothing to protect a patentee from bad-faith infringement but practically presumes bad-faith assertion and creates the threat of quadruple damages (including liability for ***quadruple*** the accused infringer's fees and costs), an injunction, and an outsized, uncapped bond in favor of the accused infringer—potentially based solely on critiquing a patent owner's federal complaint. This threat risks chilling speech and, particularly for a smaller patent owner, blocking the federal courthouse doors—or, in the case of Katana, kicking it out of those doors right after it entered.

Because it specifically targets a federal "complaint," the Act as a whole would in effect replace much of the federal scheme for handling allegations of meritless patent litigation like Micron's. Aside from 35 U.S.C. § 285 and Rule 11, other federal rules provide avenues to an early dismissal or summary judgment for

defective allegations or meritless claims. Micron's novel approach, in contrast, was to attach Katana's federal complaint as "Exhibit 1" to a state-court complaint that invokes Idaho's Act and to press for a bond calculated by quadrupling estimated fees for Micron to prosecute its own IPRs and defend the infringement case.

The district court dismissed all preemption concerns on the theory that Micron's mere allegations sufficed to satisfy the federal requirement for bad faith; that Idaho's Act is "not inconsistent" with Congress's "express policies"; and that the question of "sham litigation" requires a "fact-intensive reasonableness determination [that] is impractical to consider at the motion-to-dismiss stage." Appx18-19. Yet the court's Order failed to consider that, "in order to *assert* a claim that a patent holder has engaged in wrongful conduct by asserting claims of patent infringement, the plaintiff must *establish* that the claims of infringement were objectively baseless." *SSI Techs., LLC v. Dongguan Zhengyang Elec. Mech. LTD.*, 59 F.4th 1328, 1337 (Fed. Cir. 2023) (cleaned up). Indeed, the Order does not address even the allegations of objective baselessness except in 12 lines of text near the end, recounting Micron's conclusory allegations of invalidity because, for example, "according to Micron's complaint, the asserted patents have expired"—appearing to equate expiration with invalidity. Appx24.

In its discussion of the bond, the district court did not address preemption at all. And its only consideration of constitutionality related to the doctrine that,

"[w]hen sitting in diversity—as this Court is in the Longhorn case—federal courts apply state substantive law and federal procedural law." Appx27 (citing *Hanna v. Plumer*, 380 U.S. 460, 465 (1965)). The court went on to find the state-law bond "is not merely procedural—it is a substantive provision that discourages bad-faith patent assertion in and of itself." Appx27. Indeed, the court even stated that the "bond provision thus serves a similar purpose to the damages provisions." *Id.* Yet it ordered the bond without consideration of any evidence for or against bad faith. *See C.R. Bard*, 157 F.3d at 1369 (noting the federal presumption that patent assertions are made in good faith and explaining "this presumption is overcome only by affirmative evidence of bad faith"). Failing to consider or identify any bad-faith evidence, the state-law bond is just as unconstitutional as would be a state-law damages award with no supporting *evidence* of bad faith.

Moreover, given that Micron's BFA claim is "centered on the Katana complaint" (Appx1139) and that the "damages" it seeks are calculated as a multiple of the fees it expects to incur in defending Katana's federal infringement claim, the Act is preempted as applied even based on federal procedure alone. *See Shady Grove Orthopedic Assocs., P.A. v. Allstate Ins. Co.*, 559 U.S. 393, 398–406 (2010) (holding a federal procedural rule concerning class action eligibility preempted a state statute's provision barring class actions for certain claims even though the claim at

issue was governed by state substantive law, because the state provision "attempts to answer the same question" as the federal rule).

Here, Micron's BFA claim against both Katana and Longhorn is not about any underlying tortious misconduct. Instead, Micron's claim is little more than an accusation that Katana's infringement complaint itself was filed in bad faith and will cost Micron to defend. The question, then, would be: What is Micron's remedy? Federal Rule 11 provides the answer, but Micron claims the Act provides the answer, courtesy of the state legislature. Thus, Micron did not follow the procedures required by Rule 11. Indeed, Micron did not even move to dismiss Katana's infringement claims under Rule 12. Instead, Micron relied on Idaho's Act.[11] Since the federal rules don't provide for the patent owner to post a bond or for a sanction quadruple the accused infringer's fees and expenses to defend the patent case, Micron turned to state law. But "the state law cannot apply in federal court" because the Act as applied attempts to answer the same question as the federal rules but "imposes additional requirements" beyond those in the rules. *Klocke*, 936 F.3d at 245; *see also Shady Grove*, 559 U.S. at 399; *Abbas*, 783 F.3d at 1334.

[11] Indeed, Micron relies heavily on a bond motion it filed ***in state court*** against a Katana affiliate to stop Katana's federal case from proceeding.

D. Absent Appellate Relief, the Court Should Order Mandamus Relief Because the Bond Precondition Was Clearly Erroneous and No Other Relief Would Be Adequate.

Mandamus is "available to correct a clear abuse of discretion." *In re Apple Inc.*, 979 F.3d at 1336. For the reasons discussed in Section III(B), *supra*, all conditions for a writ to issue have been satisfied.

VIII. CONCLUSION

For all of these reasons, Appellants respectfully request the Court to vacate the district court's Order and hold that the Act is preempted. In the alternative, Appellants request a writ of mandamus vacating the Order and remanding with instructions for the district court to require no bond and to permit Katana's patent infringement case to proceed without the posting of a bond.

February 22, 2024

Respectfully submitted,

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ADDENDUM

Document Name
Memorandum Decision and Order
USRE38806E
US6,352,879
US6,731,013

UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF IDAHO

KATANA SILICON TECHNOLOGIES LLC, Plaintiff, v. MICRON TECHNOLOGY, INC, et al., Defendants.	Case No. 1:22-cv-00282-DCN Case No. 1:22-cv-00273-DCN **MEMORANDUM DECISION AND ORDER**
MICRON TECHNOLOGY, INC., et al., Plaintiffs, v. LONGHORN IP, LLC, Defendants.	

I. INTRODUCTION

Before the Court are three motions from two connected actions: Micron's Motion for Bond (Longhorn Dkt. 3), Longhorn's Motion to Dismiss (Longhorn Dkt. 7), and Katana's Motion to Dismiss (Katana Dkt. 27). On January 10, 2023, the Court held oral argument and took the motions under advisement. Upon review, and for the reasons below, the Court DENIES Longhorn and Katana's Motions to Dismiss and GRANTS Micron's Motion for Bond.

II. BACKGROUND

1. The Act

The Idaho Bad Faith Assertions of Patent Infringement Act (the "Act") is designed

to discourage patent trolls. It makes it "unlawful for a person to make a bad faith assertion of patent infringement in a demand letter, a complaint, or any other communication." Idaho Code § 48-1703(1). It also creates a private cause of action for those targeted by bad-faith demand letters, empowering courts to grant equitable relief, costs and fees, and significant punitive damages. Idaho Code § 48-1706.

The Act contains a bond provision:

> Upon motion by a target and a finding by the court that a target has established a reasonable likelihood that a person has made a bad faith assertion of patent infringement in violation of this chapter, *the court shall require the person to post a bond* in an amount equal to a good faith estimate of the target's costs to litigate the claim and amounts reasonably likely to be recovered under this chapter, conditioned upon payment of any amounts finally determined to be due to the target . . . .

Idaho Code § 48-1707 (emphasis added).

2. The Parties

Micron Technology, Inc.[1] ("Micron") is a major manufacturer of semiconductors headquartered in Boise, Idaho. Longhorn IP, LLC ("Longhorn") is a patent licensing company headquartered in Texas. It does not create products or offer services. Instead, it makes money by asserting a portfolio of patents against companies that do. Through a network of affiliates,[2] it acquires and enforces patents on, among other things, semiconductors. One of its many affiliates is Katana Silicon Technologies, LLC ("Katana"), which owns patents covering semiconductor manufacturing.

[1] Two Micron subsidiaries are also parties: Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC.

[2] Micron alleges that this affiliate structure allows Longhorn to aggressively pursue judgments against other companies while remaining judgment-proof itself.

[redacted]

3. The Katana Case

On March 4, 2022, Katana sued Micron for patent infringement in the U.S. District Court for the Western District of Texas (the "Katana case"). Katana alleged certain Micron products infringed on three of its patents: No. RE38,806 (the "'806 patent"), No. 6,352,879 (the "'879 patent,"), and No.6,731,013 (the "'013 patent"). The '806 patent and the '879 patent cover miniaturized devices that allow for many semiconductor chips to be contained in a small space. These patents expired on December 30, 2018. The '013 patent covers a special wiring substrate for semiconductor devices that relieves connection failure between the semiconductor chip and the terminal section. It expired on July 5, 2021.

Micron, which had previously been sued by a different Longhorn affiliate, perceived Katana's suit to be a bad-faith assertion of patent infringement. It filed an Answer (Katana Dkt. 13) asserting a counterclaim under the Act and seeking equitable relief, costs and fees, and damages. Katana countered with a motion to dismiss Micron's counterclaim, arguing that the Act is preempted because the federal government, not the states, regulates patents. Katana Dkt 27. Micron then asked the U.S. District Court for the Western District of Texas to transfer the Katana case to the District of Idaho and the court agreed. Once the case was in Idaho, the State of Idaho exercised its right to intervene and defend the Act, filing a memorandum in opposition to Katana's Motion to Dismiss. Katana Dkt. 43.

4. The Longhorn Case

The same day Micron filed its Answer and counterclaim in Texas, it sued Longhorn, which allegedly controls Katana, in Idaho state court (the "Longhorn case"). The Longhorn

[redacted]

case alleges that the patent infringement asserted in the Katana case violated the Act. Under Section 48-1707, Micron asked the court to impose a $15 million bond on Longhorn and Katana, asserting that this amount was a good faith estimate of its costs to litigate the claim and the amount reasonably likely to be recovered. *See* Longhorn Dkt. 1-6, at 2–3. Longhorn removed the case here and then moved to dismiss, raising the same constitutional arguments it did in the Katana case. Once again, the State intervened to defend the Act.

Both the Katana and Longhorn cases are now before the Court.

III. LEGAL STANDARD

A. Motion to Dismiss

Federal Rule of Civil Procedure 8 requires a complaint to "contain sufficient factual matter, accepted as true, to 'state a claim to relief that is plausible on its face.'" *Ashcroft v. Iqbal*, 556 U.S. 662, 678 (2009) (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 570 (2007)). The *Iqbal/Twombly* "facial plausibility" standard is met when a complaint contains "factual content that allows the court to draw the reasonable inference that the defendant is liable for the misconduct alleged." *Id.*, citing *Twombly*, 550 U.S. at 556. Accordingly, to avoid dismissal for failure to state a claim, a complaint must provide sufficient factual allegations to show that there is "more than a sheer possibility that a defendant has acted unlawfully." *Id.*

A court "need not assume the truth of legal conclusions cast in the form of factual allegations." *U.S. ex rel. Chunie v. Ringrose*, 788 F.2d 638, 643 n.2 (9th Cir. 1986). Rule 8 "demands more than an unadorned, the defendant-unlawfully-harmed-me accusation." *Iqbal,* 556 U.S. at 678. If a complaint fails to state a plausible claim, "'[a] district court

should grant leave to amend even if no request to amend the pleading was made, unless it determines that the pleading could not possibly be cured by the allegation of other facts.'" *Lopez v. Smith*, 203 F.3d 1122, 1130 (9th Cir. 2000) (cleaned up).

B. Motion for Bond

The Act gives courts nine factors to consider in determining whether a patent is asserted in bad faith:

> (a) [A] person sends a demand letter to a target without first conducting an analysis comparing the claims in the patent to the target's products, services or technology.
> (b) The demand letter does not contain the following information:
> (i) The patent number;
> (ii) The name and address of the patent owner or owners and assignee or assignees, if any; and
> (iii) The factual allegations concerning the specific areas in which the target's products, services and technology infringe the patent or are covered by the claims in the patent.
> (c) The demand letter does not identify specific areas in which the products, services and technology are covered by the claims in the patent.
> (d) The demand letter demands payment of a license fee or response within an unreasonably short period of time.
> (e) The person offers to license the patent for an amount that is not reasonably based on the value of a license to the patent.
> (f) The person asserting a claim or allegation of patent infringement acts in subjective bad faith, or a reasonable actor in the person's position would know or reasonably should know that such assertion is meritless.
> (g) The claim or assertion of patent infringement is deceptive.
> (h) The person or its subsidiaries or affiliates have previously filed or threatened to file one (1) or more lawsuits alleging patent infringement based on the same or similar claim, the person attempted to enforce the claim of patent infringement in litigation and a court found the claim to be meritless.
> (i) Any other factor the court finds relevant.

Section 48-1703. The Act provides another four factors a court may consider in

determining a patent is *not* asserted in bad faith:

> (a) The person engages in a good faith effort to establish that the target has infringed the patent and to negotiate an appropriate remedy.
> (b) The person makes a substantial investment in the use of the patent or in the production or sale of a product or item covered by the patent.
> (c) The person has:
> (i) Demonstrated good faith in previous efforts to enforce the patent, or a substantially similar patent; or
> (ii) Successfully enforced the patent, or a substantially similar patent, through litigation.
> (d) Any other factor the court finds relevant.

Id.

IV. ANALYSIS

The motions at issue raise three major questions. First, is the Act preempted by federal law? Second, has the applicable statute of limitations run? Finally, has Micron pleaded enough facts to state a plausible claim under the Act, and on those facts, is a bond warranted?

A. Federal Preemption

Longhorn and Katana argue that the Act "cannot exist alongside U.S. patent laws in our federal system" and so is preempted under the Supremacy Clause. Longhorn Dkt. 7-1, at 15. The Supremacy Clause dictates that federal law is "the supreme Law of the Land." U.S. Const. art. VI, cl. 2. Thus, federal law preempts incompatible state laws. *See Oneok, Inc. v. Learjet, Inc.*, 575 U.S. 373, 376 (2015). Preemption comes in three forms: express preemption, field preemption, and conflict preemption. *Ass'n des Éleveurs de Canards et d'Oies du Quebec v. Bonta*, 33 F.4th 1107, 1113–14 (9th Cir. 2022). Field and conflict

preemption are types of implied preemption. *Id.* at 1114.

1. Express Preemption

Congress may expressly preempt a state law by passing targeted federal legislation. *Id.* Here, no party has submitted—and the Court has not found—any federal statute expressly preempting the Act. Further, the Federal Circuit has held that federal patent law does not generally preempt state unfair competition law, which the Act could be read to be. *Hunter Douglas, Inc. v. Harmonic Design, Inc.*, 153 F.3d 1318, 1332–33 (Fed. Cir. 1998), overruled on other grounds by *Midwest Indus., Inc. v. Karavan Trailers, Inc.*, 175 F.3d 1356 (Fed. Cir. 1999). For these reasons, the Court finds that the Act is not expressly preempted.

2. Implied Preemption

Federal statutes may impliedly preempt state ones. *See Crosby v. Nat'l Foreign Trade Council*, 530 U.S. 363, 372 (2000). The Supreme Court, however, has sometimes applied a presumption against implied preemption. *See Wyeth v. Levine*, 555 U.S. 555, 565 (2009). In *Wyeth*, the Court applied the presumption and upheld a state law regulating drug labelling, despite noting that the Federal government had historically regulated this field. *Id.* (establishing an "assumption that the historic police powers of the States were not to be superseded by the Federal Act unless that was the clear and manifest purpose of Congress."). *But see Buckman Co. v. Plaintiffs' Legal Comm.*, 531 U.S. 341 (2001) (refusing to apply the presumption to a fraud case against a federal agency because the relationship between federal agencies and regulated parties is "inherently federal in character"); *Arizona v. Inter Tribal Council of Arizona, Inc.*, 570 U.S. 1, 14 (2013)

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(declining to apply the presumption to a state law governing voter-registration officials because state regulation of congressional elections "has always existed subject to the express qualification that it terminates according to federal law").

Patent law is quintessentially federal. *See Bonito Boats, Inc. v. Thunder Craft Boats, Inc.*, 489 U.S. 141, 156 (1989). States have no authority to issue patents or protect intellectual property in similar ways. *Id.* But they do have authority to protect businesses and regulate unfair competition. *See Hunter Douglas*, 153 F.3d at 1332–33.

This case pits the federal government's exclusive right to issue and regulate patent protections against Idaho's police power to protect its businesses from harassment. Though the question is close, the Court finds that the fundamentally federal nature of patents weighs against applying the presumption. Thus, because of the inherently federal subject matter at issue here, the Court will address the implied preemption arguments without applying any presumption.

Implied preemption can be divided into two general categories: field preemption and conflict preemption. *Association des Eleveurs de Canards*, 33 F.4th at 1114. The Court will address each one in turn.

a. Field Preemption

Field preemption occurs "when the scope of a federal statute indicates that Congress intended federal law to occupy a field exclusively." *Kurns v. R.R. Friction Prod. Corp.*, 565 U.S. 625, 630 (2012) (cleaned up). Here, the federal government occupies the field of patent issuance. *See Bonito Boats*, 489 U.S. at 156 (1989). Still, state law is not displaced just because it relates to intellectual property. *Id*. "[T]he states are free to regulate the use

of . . . intellectual property in any manner not inconsistent with federal law." *Id.* (quoting *Aronson v. Quick Point Pencil Co.*, 440 U.S. 257, 262 (1979)). "The case for federal preemption is particularly weak where Congress has indicated its awareness of the operation of state law in a field of federal interest, and has nonetheless decided to stand by both concepts and to tolerate whatever tension there [is] between them." *Wyeth*, 555 U.S. at 575 (quoting *Bonito Boats*, 489 U.S. at 166–167).

Here, more than half of the states[3] have adopted statutes outlawing bad-faith patent assertion. These state laws do not establish quasi-patent protections. Instead, they allow damages against those who abuse the federal patent system. Congress, by contrast, has neither passed legislation outlawing bad faith patent assertion nor established a standard for finding bad faith.[4]

By choosing not to legislate on the issue of bad-faith patent assertion, Congress has created a policy vacuum. Many states have stepped into that vacuum to protect local businesses from shakedowns at the hands of patent trolls. Considering there are more than 30 state acts prohibiting bad faith patent assertion, it is reasonable to assume that Congress knows about these acts and that its continued silence constitutes acquiescence. *See Wyeth*, 555 U.S. at 575. Thus, the Court finds that field preemption does not render the Act

[3] *Guide to State Patent Legislation*, Patent Progress, (May 1, 2019), https://web.archive.org/web/20190911174618/https://www.patentprogress.org/patent-progress-legislation-guides/patent-progresss-guide-state-patent-legislation/ (identifying thirty-three states with bad faith patent assertions statutes) (accessed via the Wayback Machine as the site appeared on Sep. 11, 2019).

[4] The federal standard for finding bad faith is the product of caselaw, not legislation. *See Globetrotter Software, Inc. v. Elan Comput. Grp., Inc.*, 362 F.3d 1367, 1375–77 (Fed. Cir. 2004) (holding that bad faith has both an objective and subjective component).

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unconstitutional.

b. Conflict Preemption

"[C]onflict preemption arises when state law conflicts with a federal statute." *Ass'n des Éleveurs de Canards*, 33 F.4th at 1114. Conflict preemption has at least two subcategories of its own: impossibility preemption and obstacle preemption. *See id.*

i. Impossibility Preemption

Impossibility preemption occurs "where it is impossible for a private party to comply with both state and federal law." *Crosby*, 530 U.S. at 372. Here, Longhorn and Katana argue that the Act conflicts with federal law in at least two ways. Both arguments involve the way courts apply allegedly competing standards, not the way private parties comply with them. The Court will nevertheless consider whether the Act makes it impossible for courts to apply both state and federal standards.

First, Longhorn and Katana argue the Act contradicts Federal law because it improperly substitutes a set of decision-making factors for the federal standard—a simple presumption of good faith. Federal law dictates that "[a] patent shall be presumed valid." 35 U.S.C.A. § 282; *see also C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1369 (Fed. Cir. 1998) ("the assertion of a duly granted patent is [presumed to be] made in good faith."). "This presumption is overcome only by affirmative evidence of bad faith." *C.R. Bard, Inc.*, 157 F.3d at 1369. The Act, on the other hand, supplies courts with a series of factors to consider in determining whether a patent is being asserted in bad faith. The list is open ended: it includes the catch-all "[a]ny other factor the court finds relevant." Idaho Code §§ 48-1703(2)(i); 48-1703(3)(d).

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The Act does not make compliance with federal law impossible. In fact, it plays in close harmony with the federal standard. By providing examples of evidence that might overcome the presumption of good faith, the state legislature has not supplanted that presumption. If anything, the Act facilitates the application of the federal standard by illustrating what kinds of behavior could constitute bad faith. The list of factors, which includes "any other factor the court finds relevant," leaves courts free to consider and follow federal guidance. Idaho Code §§ 48-1703(2)(i); 48-1703(3)(d).

It is true that the Act contains factors a court may consider "as evidence that a person has *not* made a bad faith assertion of patent infringement." Idaho Code § 48-1703(3)(3) (emphasis added). The inclusion of these factors, however, does not negate the presumption of good faith, nor does the Act require courts to make an affirmative finding of good faith before a patent may be enforced. The Act is concerned only with bad faith patent assertion, not general patent enforcement, and the language of Section 48-1703 is remarkably permissive. It offers factors that courts *may* consider, including—twice—a sweeping catch-all that invites courts to consider whatever other factors they find relevant. *See* Idaho Code §§ 48-1703(2)(i); 48-1703(3)(d). How, (and whether), a court applies the factors is left to the judge's discretion.

Because a court must follow federal law, the factors in Section 48-1703 are best viewed as a supplement to the federal standard, not an obstacle to it. Courts must apply the factors in a manner consistent with the federal presumption of good faith, and nothing in the Act prevents them from doing so. For these reasons, the Court finds that the factors in Section 48-1703 are compatible with federal law and do not engage

impossibility preemption.

Second, Longhorn and Katana argue the Act impermissibly allows courts to find that patents are being asserted in bad faith without specifically finding evidence of both objective and subjective bad faith, as Federal law requires. State laws creating liability for asserting a patent "are preempted by federal patent laws, unless the claimant can show that the patent holder acted in bad faith." *Energy Heating, LLC v. Heat On-The-Fly, LLC*, 889 F.3d 1291, 1304 (Fed. Cir. 2018). Bad faith requires a showing that the claims of infringement are both objectively baseless and asserted in subjective bad faith. *Globetrotter Software, Inc. v. Elan Comput. Grp., Inc.*, 362 F.3d 1367, 1375–77 (Fed. Cir. 2004).

Here, in a single factor, the Act provides that courts may consider whether "[t]he person asserting a claim or allegation of patent infringement acts in subjective bad faith, or a reasonable actor in the person's position would know or reasonably should know that such assertion is meritless." Idaho Code § 48-1703(2)(f)).

Unlike the Federal standard, which requires a specific finding of both objective and subjective bad faith, the Act's factor could be read to permit consideration of only one or the other. The problem is the difference between "and" and "or." This inconsistency in conjunctions might create an issue, were it not for the catch-all clauses in Section 48-1703, which allow courts to consider any other factor they find relevant. *See* Idaho Code §§ 48-1703(2)(i); 48-1703(3)(d). Courts applying the Act must consider the federal standard—requiring both objective and subjective findings—as a relevant factor, and the Act allows them to do so. The Act and federal law are not mutually exclusive, and so impossibility preemption does not apply.

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ii. Obstacle Preemption

Obstacle preemption occurs where state law "stands as an obstacle to the accomplishment and execution of the full purposes and objectives of Congress." *Crosby*, 530 U.S. at 373. "[S]tate regulation of intellectual property must yield to the extent that it clashes with the balance struck by Congress in our patent laws." *Bonito Boats,* 489 U.S. at 152. In *Bonito Boats*, a Florida statute barred people from duplicating a proprietary molding process used for making boat hulls, or selling duplicated hulls, effectively granting this unpatented molding process greater protection than it would have received under federal patent laws. *Id.* at 144–45. The Supreme Court held that this state law improperly upset the balance of interests Congress struck in its patent laws, and so was preempted. *Id.* at 152. The Court held that, when it is clear how patent laws strike the balance between "the desire to freely exploit the full potential of our inventive resources and the need to create an incentive to deploy those resources," the states may not second guess Congress' judgment by passing more stringent intellectual property protections. *See id.*

Similarly, at least one federal court has found that a state may not disrupt the "congressionally chosen calculus of litigation incentives and disincentives" by providing for attorneys' fees in patent cases other than those available under federal law. *Bldg. Innovation Indus., LLC v. Onken*, 473 F. Supp.2d 978, 986–88 (D. Ariz. 2007).

The Federal Patent Act ("Patent Act") is Congress' primary effort to balance what *Bonito Boats* called "the desire to freely exploit the full potential of our inventive resources" against "the need to create an incentive to deploy those resources." 489 U.S. at 152. To discourage patent infringement, the Patent Act sets a floor for the damages a

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successful patentee can receive: nothing less "than a reasonable royalty for the use made of the invention by the infringer, together with interest and costs as fixed by the court." 35 U.S.C.A. § 284. It also sets a ceiling: "the court may increase the damages up to three times the amount found or assessed." *Id.*

The Patent Act discourages egregious abuse of the patent system. It provides that courts may, "in exceptional cases," award reasonable attorney fees to a prevailing party. 35 U.S.C. § 285. This provision, which Congress added in 1945, "enabled courts to address unfairness or bad faith in the conduct of the losing party." *Octane Fitness, LLC v. ICON Health & Fitness, Inc.*, 572 U.S. 545, 548 (2014) (cleaned up); *see also Pennsylvania Crusher Co. v. Bethlehem Steel Co.*, 193 F.2d 445, 451 (3rd Cir. 1951) (listing "vexatious or unjustified litigation" as adequate justification for awarding attorneys' fees). Congress recodified the provision in 1952, adopting its current language, but the change did not substantively alter its meaning. *See Octane Fitness*, 572 U.S. at 549. In *Octane Fitness*, the Supreme Court expanded the applicability of this provision, holding that "something less than bad faith" could warrant fee shifting. *Id.* at 555.

Here, the Act strikes a similar balance to the one struck by Congress. It expresses a strong policy against patent infringement:

> (b) . . . Patent holders have every right to enforce their patents when they are valid and infringed, to solicit interest from prospective licensees and to initiate patent enforcement litigation as necessary to protect intellectual property.
>
> (c) The legislature does not wish to interfere with the good faith enforcement of patents or good faith patent litigation. The legislature also recognizes that Idaho is preempted from passing any law that conflicts with federal patent law.

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Idaho Code § 48-1701(b)–(c). Though it does not set a floor, it does set a ceiling for the damages a successful party may be entitled to if it proves a patent has been asserted in bad faith. A court may grant a successful plaintiff his actual costs and damages, plus exemplary damages of fifty thousand dollars or three times the total of his damages, costs and fees, whichever is greater. Idaho Code § 48-1706(1).

Longhorn and Katana complain that the Act unfairly chills patentees' ability to enforce their rights: "[b]y regulating federal lawsuits and allowing for quadruple damages, an up-front bond, and injunctive relief, [the Act] strikes a lopsided balance of the rights of patentees and apparent infringers and poses an obstacle to the 'full purposes and objectives' of federal patent laws." Longhorn Dkt. 71, at 19. The Court disagrees.

The Act does not stand as an obstacle to the policy goals Congress expressed in the Patent Act. Both the state Act and the federal Patent Act have the end goal of protecting valid patents without enabling bad-faith or vexatious litigation.

The fee-shifting provision in the Patent Act—which the Supreme Court recently expanded and emphasized in *Octane Fitness*, is especially relevant. Through that provision, Congress intended to allow courts to penalize abusive or bad-faith patent litigation—the identical aim the Idaho Legislature had in passing the Act. Remarkably, the fee-shifting provision in the Patent Act requires a lower evidentiary threshold than the threshold in the Act. Compare 35 U.S.C. § 285 (allowing fee-shifting in "exceptional cases") with Idaho Code Section 48-1703 (allowing damages when a court finds affirmative evidence of bad faith); *Octane Fitness*, 572 U.S. at 555 (holding that the federal Patent Act requires

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"something less than bad faith") with *Globetrotter Software,* 362 F.3d at 1375–77 (holding that state laws creating liability for patent assertion require a showing that the claims of infringement are both objectively baseless and asserted in subjective bad faith). The Act has the same essential purposes as the Patent Act and goes no further than its federal counterpart in pursuing them. There is no conflict of purpose or objective here.

Longhorn and Katana nevertheless assert that there is a conflict of method and execution. They argue that the Act threatens to upset at least one federal policy balance by allowing higher damages for successful defendants than the Patent Act allows successful plaintiffs. The Federal Patent Act allows a court to give successful plaintiffs treble damages. Functionally, the state Act allows a court to grant successful defendants quadruple damages. This disparity allows the inference that the Idaho legislature views bad-faith patent assertion as a bigger problem than Congress does and has attempted to alter the "congressionally chosen calculus of litigation incentives" accordingly. *Onken*, 473 F. Supp.2d at 987.

Bonito Boats held this type of alteration would be inappropriate in the context of a state law providing quasi-patent protections. And *Onken* suggests it would be inappropriate in the context of a state law creating new fee shifting provisions separate from those already in the federal Patent Act. Neither decision, however, fits neatly with the facts here.

Besides addressing mirror-opposite state activity (in *Bonito Boats,* Florida was trying to protect IP owners from infringement by businesses; here, Idaho is trying to protect businesses from harassment by IP owners), *Bonito Boats* forbade states from upsetting Congress' solution to the problem of how to motivate creators without stifling creativity.

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Unlike that high-level, strategic compromise, this case implicates a more tactical compromise: should the risks and potential rewards of litigation favor IP owners or businesses?

Congress has not directly addressed this issue in the context of bonds and damages. *Onken* expressly addresses this tactical compromise, but only in the context of attorneys' fees, which are already provided for by the Patent Act. By contrast, there is no federal statute on bad faith assertion of patent infringement. The distinction is important because fee shifting alone does not address the entire calculus of litigation incentives: it may not be an effective deterrent against patent trolls who have compartmentalized their liability and assets to avoid the potential negative consequences of litigation.[5] Damages and bonds are a developing part of the calculus, which Congress has yet to weigh in on. As discussed, this is an area where Congress has been content to let states do the legislating—and courts asked to review those state acts have upheld their constitutionality. *See NAPCO, Inc. v. Landmark Tech. A, LLC*, 555 F. Supp. 3d 189, 212 (M.D.N.C. 2021) (upholding a North Carolina bad-faith patent assertion statute providing for quadruple damages); *Landmark Tech., LLC v. Azure Farms, Inc.*, 2020 WL 1430088, at *5 (D. Or. Mar. 24, 2020)

[5] At least one state legislature has made such a finding:

> In lawsuits involving abusive patent assertions, an accused infringer prevailing on the merits may be awarded costs and, less frequently, fees. These awards do not serve as a deterrent to abusive patent assertion entities who have limited liability, as these companies may hold no cash or other assets. North Carolina has a strong interest in making sure that prevailing North Carolina companies sued by abusive patent assertion[] entities can recover what is awarded to them.

N.C. Gen. Stat. § 75-141(9).

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(upholding a similar Oregon statute); *Washington v. Landmark Tech. A, LLC*, No. 2:21-cv-00728-RSM (ECF No. 35), slip op. at 12 (W.D. Wash. Oct. 28, 2022) (upholding a similar Washington statute).

The Act does not intrude on Congress' exclusive right to grant patents. Nor does it alter any policy line that Congress has expressly drawn. Without more guidance from Congress, the Court will not strike down the Act just because of the difference between triple and quadruple damages. Because the Act is not inconsistent with Congress' express policies, the Court finds that it is not an obstacle to them. *See Aronson*, 440 U.S. at 262 (upholding a contract that had the effect of a patent because it was not inconsistent with express congressional policy).

3. The Noerr-Pennington Doctrine

Longhorn and Katana argue that, by making it unlawful to assert bad-faith patent infringement in a complaint, the Act impermissibly interferes with the ability to sue in federal court. The *Noerr–Pennington doctrine* immunizes defendants against antitrust liability for engaging in conduct aimed at influencing decision-making by the government, including litigation. *Octane Fitness*, 572 U.S. at 555–56. Courts have applied the *Noerr-Pennington* doctrine to bar "any claim, federal or state, common law or statutory, that has as its gravamen constitutionally-protected petitioning activity." *Gen-Probe, Inc. v. Amoco Corp.*, 926 F. Supp. 948, 955 (S.D. Cal. 1996) (collecting cases and finding that *Noerr* immunity is "constitutional and rooted in the First Amendment right to petition").

The *Noerr-Pennington* doctrine, however, does not protect defendants engaged in "sham litigation." *Pro. Real Est. Invs., Inc. v. Columbia Pictures Indus., Inc.*, 508 U.S. 49,

51 (1993). Sham litigation is "objectively baseless in the sense that no reasonable litigant could realistically expect success on the merits." *Globetrotter Software*, 362 F.3d at 1376. "In other words, the plaintiff must have brought baseless claims in . . . [subjective] bad faith." *Octane Fitness*, 572 U.S. at 556. The fundamental question is one of reasonableness. *See Globetrotter Software*, 362 F.3d at 1376.

Because application of the *Noerr-Pennington* Doctrine requires a fact-intensive reasonableness determination, it is impractical to consider at the motion-to-dismiss stage. *Washington v. Landmark Tech. A, LLC*, No. 2:21-cv-00728-RSM (ECF No. 35), slip op. at 12 (W.D. Wash. Oct. 28, 2022) (declining to decide whether Washington's bad faith patent assertion statute violated the *Noerr–Pennington* doctrine at the motion-to-dismiss stage); *see also NAPCO, Inc.*, 555 F. Supp. 3d at 215 (declining to find *Noerr-Pennington* immunity on a motion to dismiss because "reasonableness is a question of fact").

Here, the Court is asked to determine whether the Act unconstitutionally interferes with Longhorn and Katana's First Amendment right to petition the government for redress of grievances, which requires it to determine whether they are engaged in sham litigation. Both questions are fact intensive and premature at the motion-to-dismiss stage. The Court may take up these arguments upon the completion of discovery, but it will not dismiss any complaints on *Noerr-Pennington* grounds before then.

B. Time Bars

Longhorn and Katana argue that Micron's claims under the Act have been barred since 2021. The Act, in creating a private cause of action, also creates a limitations period:

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> No private action may be brought under the provisions of this chapter more than three (3) years after the cause of action accrues. A cause of action shall be deemed to have accrued when the party bringing an action under the provisions of the chapter knows, or in the exercise of reasonable care should have known, about the violation of the provisions of this chapter. *Each bad faith assertion of patent infringement constitutes a separate violation of this chapter*.

Idaho Code § 48-1706(3) (emphasis added). The Act prohibits bad-faith assertions of patent infringement "in a demand letter, a complaint, or any other communication." Idaho Code § 48-1703(1).

Here, Micron knew about Katana and Longhorn's intent to assert their patents as early as 2018, when Katana sent demand letters and met with Micron at its Boise headquarters. Katana filed its complaint on March 4, 2022, some three years after first threatening to do so. Micron made its first claim under the Act on June 6, 2022.

It is undisputed that, for purposes of the statute of limitations, a cause of action accrued in 2018 when Micron first knew of Longhorn and Katana's intent to assert their patents. The issue is whether the Katana complaint constituted a new "assertion" of the Katana patents, or merely another step in an ongoing assertion that began in 2018. The Katana complaint, Longhorn argues, was an escalation of an existing assertion, not a new assertion that triggered a new limitations period. Micron counters that each demand letter and complaint constituted an independent assertion that triggered a distinct limitation period.[6]

[6] Micron also argues that Longhorn and Katana's actions constituted a continuing tort such that the statute of limitations should be tolled. The Court does not decide this question here because, at this stage of the proceedings, it is moot.

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Micron is within the statute of limitations. The Act lists complaints as unlawful acts distinct from demand letters. *See* Idaho Code § 48-1703(1)) (making it "unlawful for a person to make a bad faith assertion of patent infringement *in a demand letter, a complaint, or any other communication*.") (emphasis added). Because a demand letter usually precedes a complaint, this language is redundant if a complaint that follows a demand letter does not constitute a separate assertion. Further, "[e]ach bad faith assertion of patent infringement constitutes a separate violation." Idaho Code § 48-1706(3). This provision suggests that, in commencing patent litigation against a target, a person may commit a separate violation at each step or escalation of the process, rather than committing one extended violation that begins with the demand letter and ends three years later, no matter what escalatory tactics are employed in between.

Finally, Longhorn's reading of the limitations provision would allow bad actors to defeat the Act through gamesmanship: if a patent troll can escape the Act by waiting three years between sending a demand letter and commencing litigation, the limitations provision swallows the Act. For these reasons, the Court finds that by sending a complaint, Longhorn and Katana made a new assertion that triggered a new limitations period, which has not yet run.

C. Adequacy of the Pleadings

Longhorn and Katana argue that Micron has failed to plead a plausible claim for bad-faith patent assertion and that the Court must therefore dismiss Micron's complaint in the Longhorn case and counterclaim in the Katana case under Rules 8 and 12(b)(6).

To escape dismissal under Rule 12(b)(6), a complaint must "contain sufficient

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factual matter, accepted as true, to state a claim to relief that is plausible on its face." *Iqbal*, 556 U.S. at 678 (cleaned up). This "facial plausibility" standard is met when a complaint contains "factual content that allows the court to draw the reasonable inference that the defendant is liable for the misconduct alleged." *Id.*, citing *Twombly*, 550 U.S. at 556. Thus, the issue here is whether Micron's complaint contains enough factual content to state a facially plausible claim that Longhorn and Katana are liable under the Act. The Court presumes that Longhorn and Katana have asserted their patents in good faith, though this presumption may be overcome by affirmative evidence. 35 U.S.C.A. § 282; *C.R. Bard, Inc.*, 157 F.3d at 1369.

1. Factors for Bad Faith

The Act allows a court to make a determination of bad faith using factors including the analysis that led to sending a demand letter, Idaho Code Section 48-1703(2)(a), the nature of the demand letter and the information it contained, Section 48-1703(2)(b)–(c), the sum of money sought in the demand letter, Section 48-1703(2)(d)–(e), the subjective and objective good faith of the patentee, Section 48-1703(2)(f), the patentee's history of assertion, and any deception present in the assertion. Idaho Code § 48-1703(2)(g)–(h).

a. Section 48-1703(2)(a)

Under Section 48-1703(2)(a), Micron has pleaded enough facts to support a conclusion that Katana sent a demand letter without first conducting an adequate analysis comparing its patents to Micron's products. Micron's complaint distinguishes the subject matter of the Katana patents from that of the allegedly infringing Micron products. For example, the asserted '806 patent covers a semiconductor device sealed with a resin, which

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the allegedly infringing Micron product does not contain, being sealed instead with a "thermoplastic encapsulant." Micron asserts that, had Longhorn and Katana properly compared the patents against the allegedly infringing products, it would have discovered such a critical difference.

b. Section 48-1703(2)(b)–(c)

There is no information in the pleadings about whether the demand letters contained the patent number, name and address of the patent owner, or the specific areas in which Micron's products infringed on covered claims. Without this information, the factors in Section 48-1703(2)(b)–(c) do not weigh either for or against bad faith.

c. Section 48-1703(2)(d)–(e)

The pleadings do not mention the sum of money that Longhorn and Katana sought from Micron in the demand letters. Thus, the factors in Section 48-1703(2)(d)–(e) are not probative either.

d. Section 48-1703(2)(f)

Micron has pleaded sufficient facts to support a conclusion that Longhorn and Katana acted in subjective bad faith. In its initial demand letter, Katana "in what can only be characterized as a thinly-veiled threat . . . pointed out that its . . . patents had been asserted against other companies." Dkt. 1-4, at 12. When the parties later met at Micron's Boise headquarters, "Longhorn communicated that the amounts demanded would increase as time passed because Longhorn was only just beginning its campaign of seeking licensing fees from companies based on the Katana portfolio. In [the Longhorn's principal]'s words, they were offering Micron an 'early bird special.'" Dkt. 1-4, at 14–15. Later, Longhorn's

representative suggested that Micron look over the patents in the portfolio of another Longhorn affiliate, Carthage Silicon Innovations, LLC. Micron took this suggestion to mean that Longhorn intended to pursue every available avenue to assert patent infringement claims against Micron, no matter which affiliate held the patents or how applicable those patents were.

Further, Micron has pleaded sufficient facts to support a conclusion that Longhorn and Katana's claims are objectively meritless. Micron pleads that the asserted patents are invalid. First, according to Micron's complaint, the asserted patents have expired. The '879 and '806 patents expired on December 30, 2018, and the '013 patent expired on July 5, 2021.

Micron further alleges that these patents are invalid "because the technology claimed in [them] was known, discussed in literature, described in other patents, and used in multiple commercially available products, all prior to the priority dates of the Katana patents." Dkt. 1-4, at 15. Micron's complaint takes pains to list, for each asserted patent, preexisting inventions and literature describing the same innovations that Longhorn and Katana claim their patents cover. For example, as early as 1998, Intel Corporation had developed a semiconductor package with the same key elements as the subject matter of the '879 patent. Thus, Micron has adequately pleaded that Longhorn and Katana have acted in objective and subjective bad faith.

e. Section 48-1703(2)(g)

Micron has pleaded enough facts to support a conclusion that Longhorn and Katana's assertion of patent infringement is deceptive. Micron's complaint says that

[redacted]

"Longhorn purports to assert claims of ongoing, current infringement for expired patents"—in other words, that it engages in deception. Micron's complaint further alleges that Katana is a mere puppet of Longhorn, which drives the bad-faith patent assertion through its affiliates. Though Longhorn otherwise portrays itself as a completely separate entity, it lists its affiliates' patent portfolios on its website in a manner suggesting it considers those patents to be its own assets. The sole manager and member of Longhorn is also the sole member and manager of each of its affiliates. Longhorn is represented by the same counsel as Katana and appears to have identical interests. Katana informed Micron that, to escape liability, it would need to secure licenses from two other Longhorn affiliates: Hamilcar Barca IP, LLC, and Trenchant Blade Technologies, LLC. On these facts, it is plausible that Longhorn and Katana have portrayed both their patents and themselves deceptively.

f. Section 48-1703(2)(h)

Micron has pleaded enough facts to indicate that Longhorn and Katana have filed or threatened to file lawsuits based on a similar claim that was meritless. Micron claims to have a history with one of Longhorn's affiliates, Lone Star Silicon Solutions, LLC, ("Lone Star") who sued Micron for patent infringement in 2016. In that case, the Patent Trial and Appeal Board ruled the disputed patents were invalid—the covered inventions were not patentable because "the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention of the patents." Dkt. 1-4, at 10. Judge Alsup, of the Northern District of California, dismissed the district court litigation and "criticized Lone Star for having incorrectly stated that it was the sole owner of the asserted

[redacted]

patents and having engaged in a 'litigation gimmick.'" Dkt 1-4, at 10. Micron agreed to pay Lone Star a sum in exchange for a promise not to appeal.

In its Complaint, Micron alleges that Longhorn is a non-practicing entity with a pattern of asserting patents in bad faith through a network of affiliates. Longhorn and Katana do not use their patents in commerce. Their only business is litigation. Longhorn and Katana may have made a substantial investment in purchasing the patents, but it was not an investment in research or development.

2. Factors Against Finding Bad Faith

As factors to consider in finding that the patentee *is not acting in bad faith*, the Act lists the patentee's good-faith efforts to negotiate an appropriate remedy, Idaho Code Section 48-1703(3)(a), the patentee's investment in the use of the patent or use of it in manufacturing, Section 48-1703(3)(b), the patentee's history of successfully enforcing the patent in good faith, Section 48-1703(3)(c), and any other factor the court finds relevant. Idaho Code § 48-1703(3)(d). Because patents are already presumed to be asserted in good faith, the Court does not consider these factors to be probative and will not analyze them. *See infra* section A2(b)(*i*) (discussing the federal presumption of good faith and its interplay with the factors in Idaho Code Section 48-1703(3)(a)–(d)).

The bottom line is that Micron's complaint pleads enough facts to allow a finding under the statutory factors that Longhorn and Katana acted in bad faith. This is enough affirmative evidence, if accepted as true, to overcome the presumption of good faith. Thus, Micron has stated a claim under the Act and dismissal is inappropriate. For all the reasons above, Longhorn and Katana's motions to dismiss are DENIED.

[redacted]

1. Bond

As an initial matter, the Court is constitutionally empowered to impose a bond. When sitting in diversity—as this Court is in the Longhorn case—federal courts apply state substantive law and federal procedural law. *Hanna v. Plumer*, 380 U.S. 460, 465 (1965). In *Ice Castles, LLC, v. LaBelle Lake Ice Palace, LLC*, 2021 WL 3085479, at *3 (D. Idaho July 21, 2021), the Court declined to wade into the "vexing question" of whether the Act's bond provision was substantive or procedural. After a review of similar statutes from other states, however, the Court is satisfied that the bond is not merely procedural—it is a substantive provision that discourages bad-faith patent assertion in and of itself.

North Carolina's equivalent statute, for instance, provides for both damages and a bond because patent trolls "may hold no cash or other assets" to pay a damages award and the state "has a strong interest in making sure that prevailing . . . companies sued by abusive patent assertion[] entities can recover what is awarded to them." N.C. Gen. Stat. § 75-141(9). The bond provision thus serves a similar purpose to the damages provisions and furthers the purpose of the statute. Though the Act does not explicitly list such a finding, the Court is persuaded that the same rationale applies. Further, if the Court were to find that the provision was procedural, it would create a forum shopping problem: plaintiffs would favor the state courts where the bond provision was available, while defendants would favor the federal courts. *See Sonner v. Premier Nutrition Corp.*, 971 F.3d 834, 839 (9th Cir. 2020) (holding that, in distinguishing substantive and procedural laws, courts must be cognizant of *Erie*'s dual aims: "discouragement of forum-shopping and avoidance of inequitable administration of the laws"). Because the bond provision is substantive, it is

[redacted]

within the power of the Court to impose a bond.

The Act provides the standard for imposing a bond. Idaho Code § 48-1707. If, using the Section 48-1703 factors, a court determines there is a reasonable likelihood that a patent is being asserted in bad faith, it must require the party asserting the patent to "post a bond in an amount equal to a good faith estimate of the target's costs to litigate the claim and amounts reasonably likely to be recovered" under the Act. *Id.*

Unlike the 12(b)(6) standard, which requires facial plausibility, the Act requires merely "a reasonable possibility." Thus, the Court must determine whether there is a reasonable possibility that Longhorn and Katana asserted infringement in bad faith.

Because the higher 12(b)(6) standard has been satisfied, the lower statutory standard is also necessarily satisfied. The above analysis on the motion to dismiss serves also to show that, under the Act, a bond is required.

Micron asserts that the Court should require a bond of $15 million. It reached this number by using the American Intellectual Property Law Association's report on the cost of defending patent suits. This report estimates that the cost to litigate against a non-practicing entity over one patent from motion practice through to appeal is $4,558,000, assuming that more than $25 million is at stake. Dkt. 15-37, at 17. Micron acknowledges that Longhorn has not yet made a specific demand for damages. Nevertheless, Micron relies on this $25-million-plus estimate from the report to calculate that the cost of defending a three-patent case is $3.75 million. That amount, plus treble damages, brings its estimate to $15 million.

There is no reason to find that this estimate is made in bad faith. The Act, however,

[redacted]

does not obligate the Court to reflexively accept a party's good faith estimate—in fact, it does not specify who, between the parties and the Court, is responsible for making such an estimate. *See* Idaho Code § 48-1707 (providing for a bond "in an amount equal to a good faith estimate of the target's costs to litigate the claim and amounts reasonably likely to be recovered . . .").

The Court accepts Micron's estimate as it relates to litigation over a single patent. That is, a conservative estimate of litigating a single-patent suit from pre-trial through to appeal is $1.25 million. The Court rejects, however, the assumption that, by tripling that sum, one can accurately predict the cost of litigating a three-patent suit. Although patent litigation does become more expensive the more patents are at issue, there are significant efficiencies inherent in bundling disputed patents together into a single suit. For instance, depositions need only be taken once—not three times—and pleadings likewise need only be filed once. Thus, for purposes of this suit, the Court finds that the additional two patents could be reasonably expected to increase Micron's cost of litigation by a total of $.75 million. Two million dollars, therefore, is a good-faith estimate of Micron's costs to litigate the claims and an amount reasonably likely to be recovered under the Act. That sum, plus treble damages, yields an $8 million bond. The Court will impose a bond in that amount. Micron's Motion for Bond is GRANTED.

V. CONCLUSION

The Court finds that the Act is not preempted by federal law, that its limitations period has not run, and that Micron has adequately pleaded a claim under it. Accordingly, the Court will DENY Longhorn and Katana's Motions to Dismiss and GRANT Micron's

[redacted]

Motion for Bond.

IV. ORDER

1. Longhorn's Motion to Dismiss (Case 1:22-cv-00273, Dkt. 7) is DENIED.
2. Katana's Motion to Dismiss (Case 1:22-cv-00282, Dkt. 27) is DENIED.
3. Micron's Motion for Bond (Case 1:22-cv-00273, Dkt. 3) is GRANTED.
    a. Longhorn or Katana must post a bond of $8 million before the Katana case (1:22-cv-00282) may proceed further.
4. This order will be entered in both cases.

DATED: May 3, 2023

David C. Nye
Chief U.S. District Court Judge

[redacted]

US00RE38806E

(19) **United States**
(12) **Reissued Patent**
Fukui et al.

(10) **Patent Number: US RE38,806 E**
(45) **Date of Reissued Patent: Oct. 4, 2005**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Yasuki Fukui**, Tenri (JP); **Yoshiki Sota**, Nara (JP); **Yuji Matsune**, Tenri (JP); **Atsuya Narai**, Yamatokoriyama (JP)

(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka (JP)

(21) Appl. No.: **10/428,013**

(22) Filed: **May 2, 2003**

Related U.S. Patent Documents

Reissue of:
(64) Patent No.: **6,229,217**
Issued: **May 8, 2001**
Appl. No.: **09/604,079**
Filed: **Jun. 27, 2000**

U.S. Applications:
(63) Continuation of application No. 09/223,272, filed on Dec. 30, 1998, now Pat. No. 6,100,594.

(30) **Foreign Application Priority Data**

Jan. 14, 1998 (JP) 10-5221

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52
(52) **U.S. Cl.** **257/777**; 257/685; 257/686
(58) **Field of Search** 257/777, 685, 257/686, 723, 724, 778; 438/108, 109, 110, 107

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,077,724 A * 6/2000 Chen 438/107

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Primary Examiner—S. V. Clark
(74) *Attorney, Agent, or Firm*—Nixon & Vanderhye, P.C.

(57) **ABSTRACT**

A first semiconductor chip is produced by affixing a thermo-compression sheet to the back surface of a wafer having a circuit formed on its front surface. The first semiconductor chip is mounted on a circuit board including an insulating substrate and a wiring layer provided on the insulating substrate so that the back surface of the first semiconductor chip faces the circuit board. A second semiconductor chip produced in the same manner as the first semiconductor chip is mounted on the first semiconductor chip with its back surface facing the first semiconductor chip. Each of the first and second semiconductor chips is wire-bonded to the wiring layer with a wire. The first and second semiconductor chips and the wire are sealed with a sealing resin. The wiring layer is connected to external connection terminals through via holes provided in the insulating substrate.

33 Claims, 15 Drawing Sheets

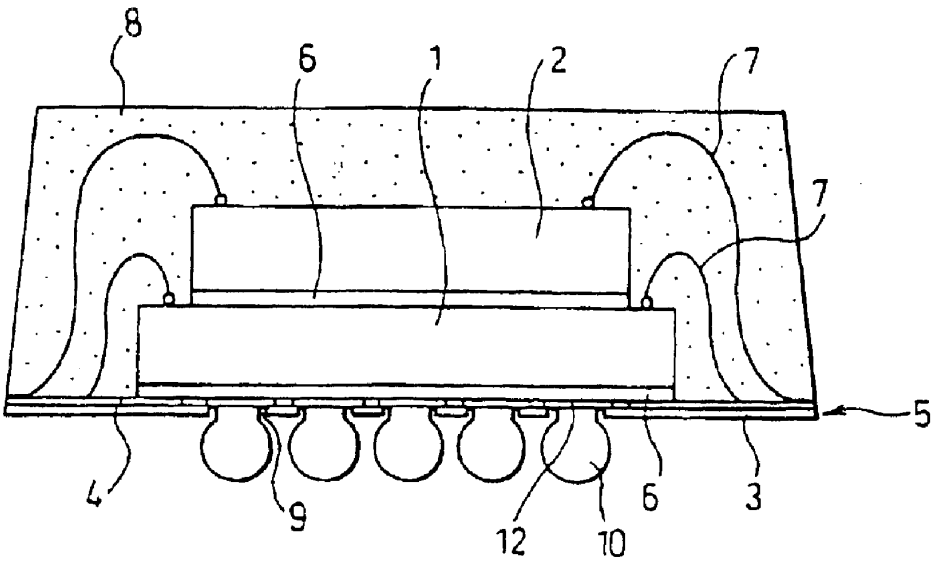


FIG.1

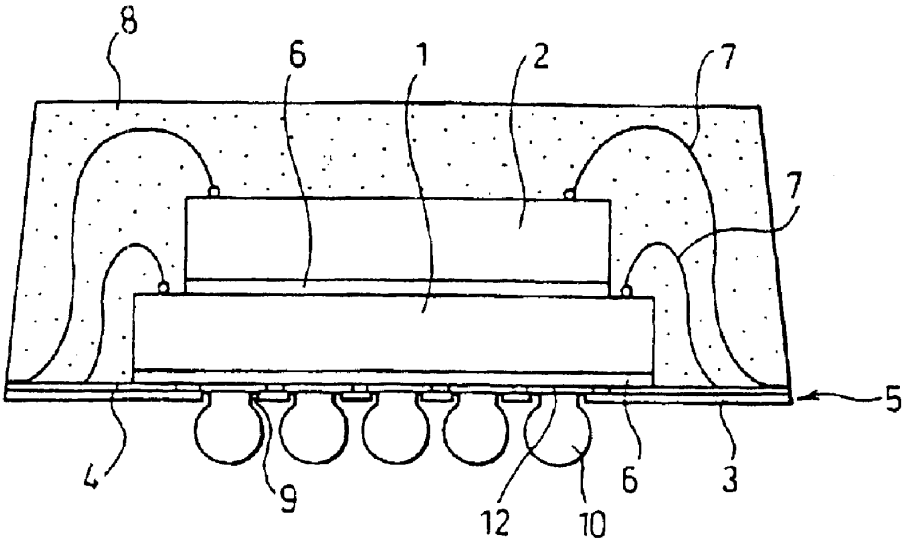


FIG. 2(a)

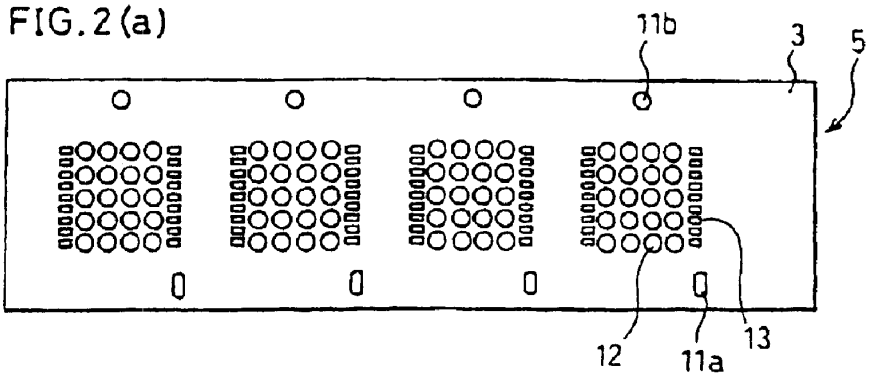


FIG. 2(b)

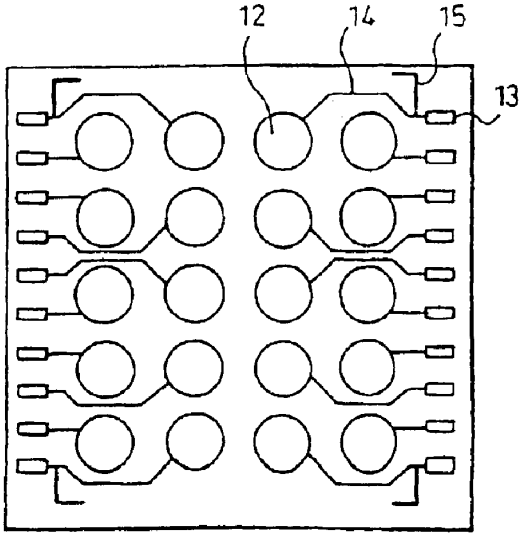


FIG.3(a)

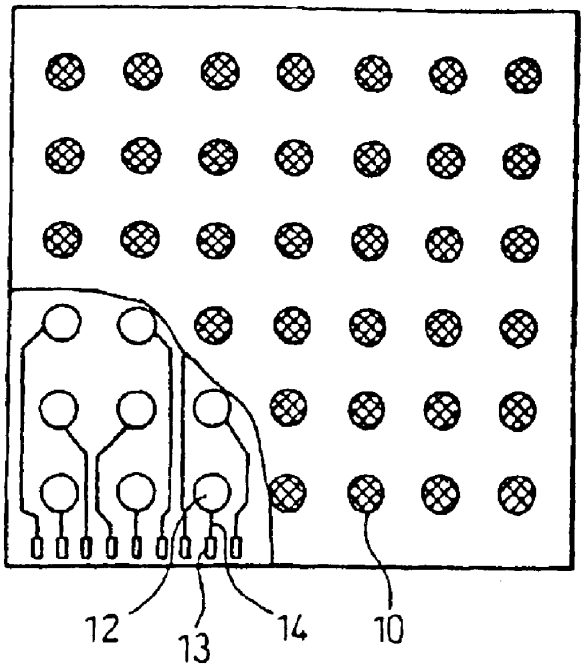


FIG.3(b)

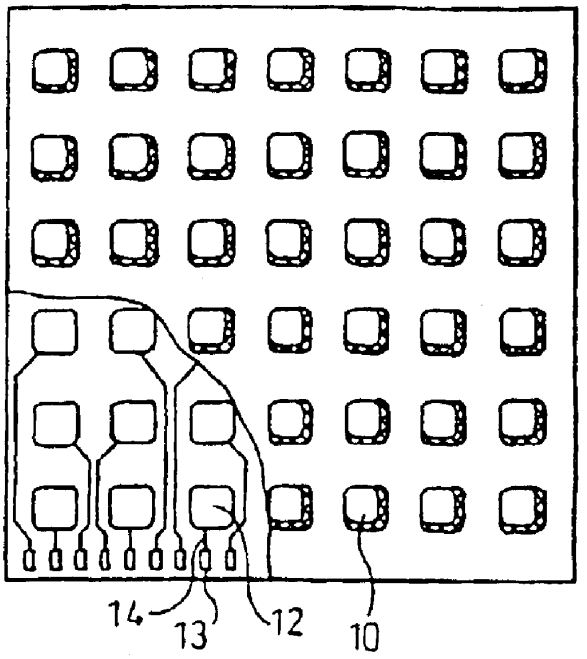


FIG. 4

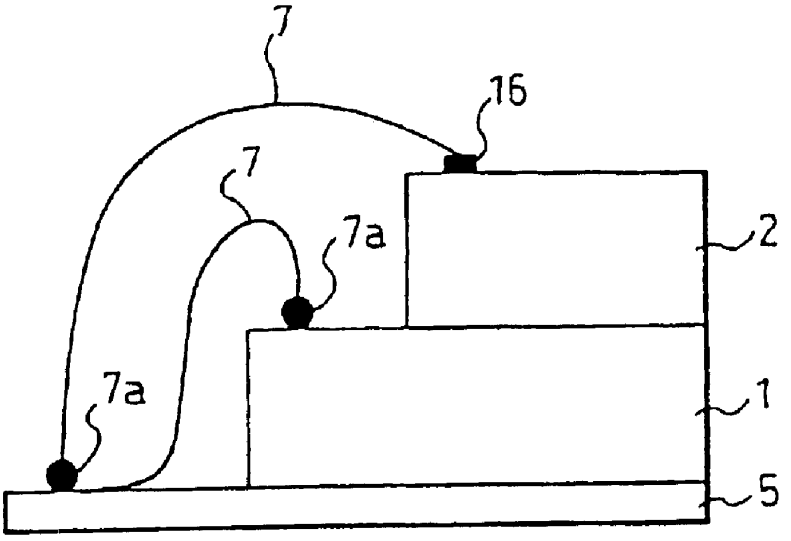


FIG.5(a)

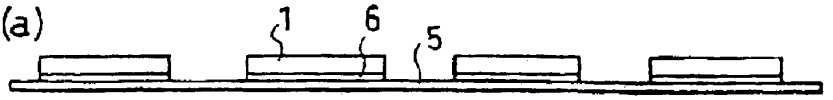


FIG.5(b)

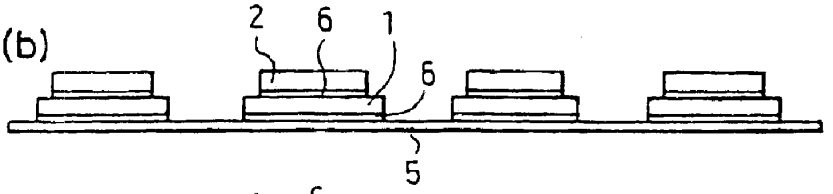


FIG.5(c)

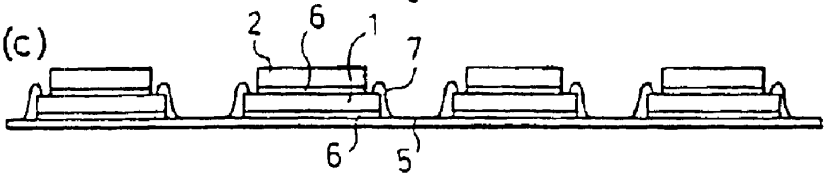


FIG.5(d)

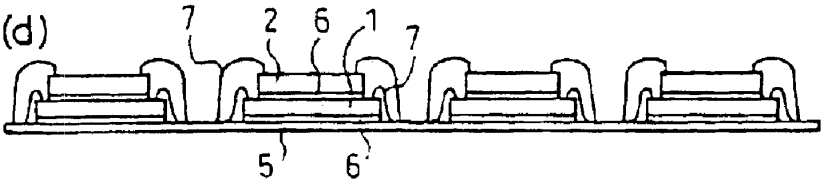


FIG.5(e)

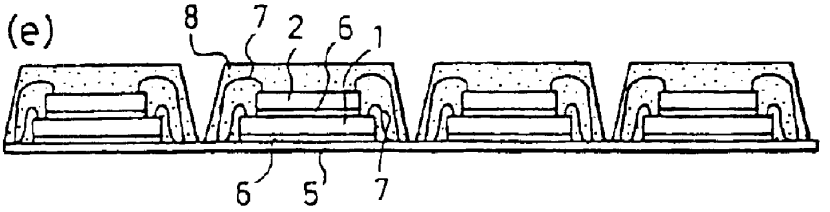


FIG.5(f)

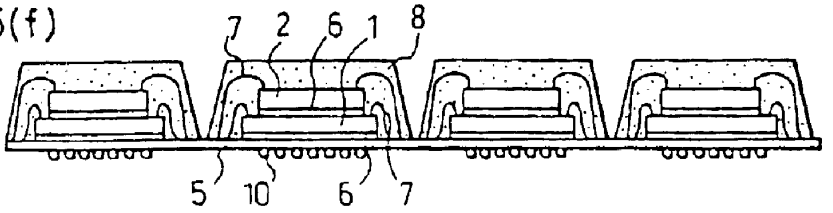


FIG.5(g)

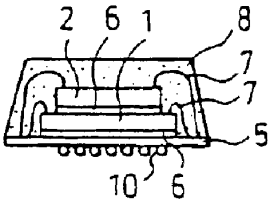


FIG.6 (a)

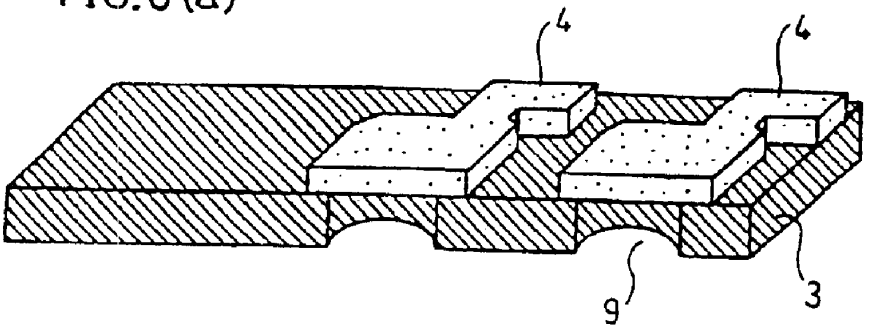


FIG.6 (b)

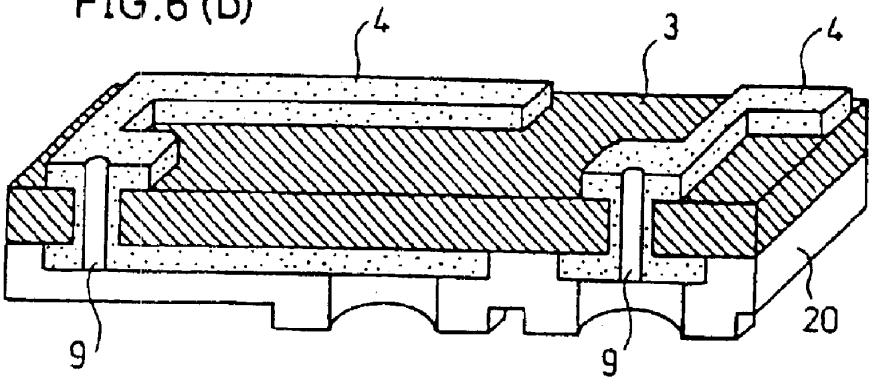


FIG.7(a)

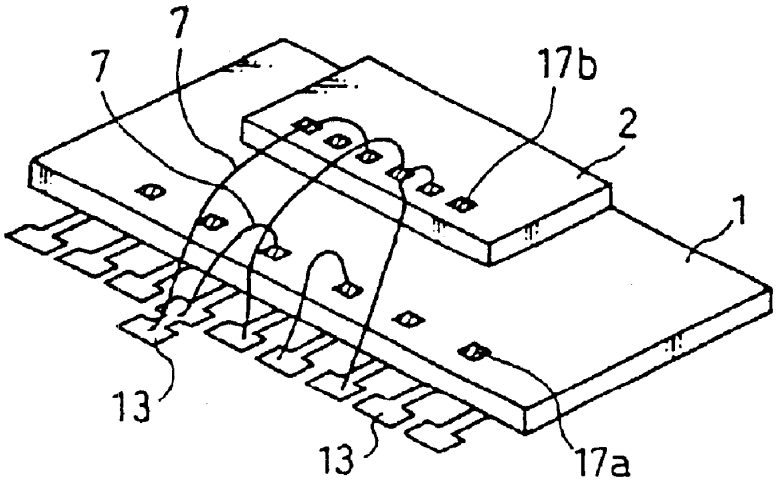


FIG.7(b)

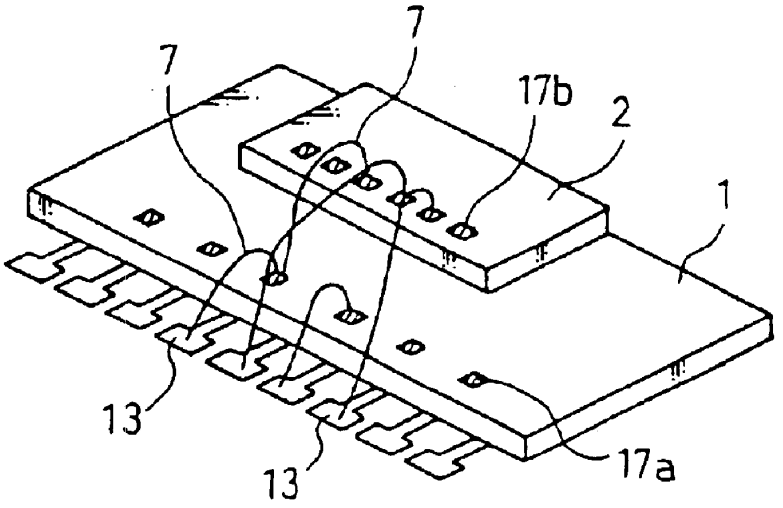


FIG. 8 (a)

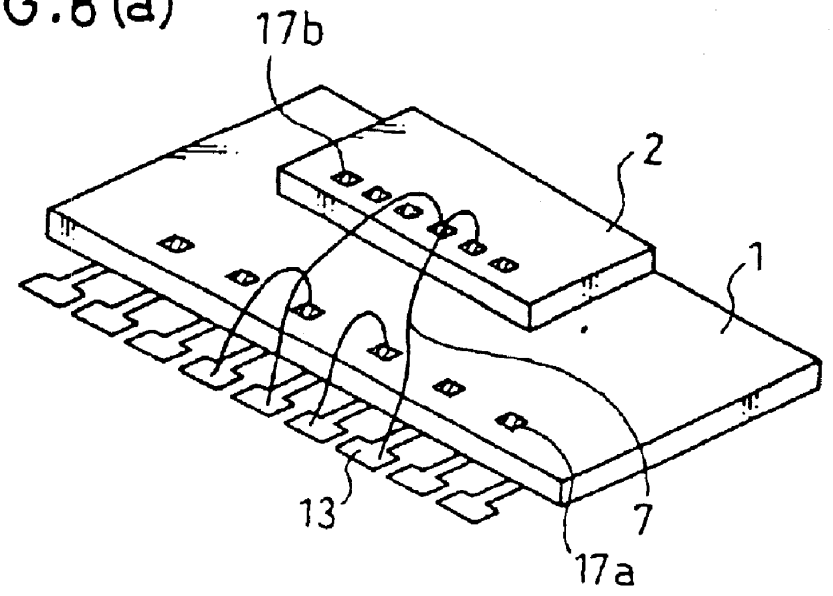


FIG. 8 (b)

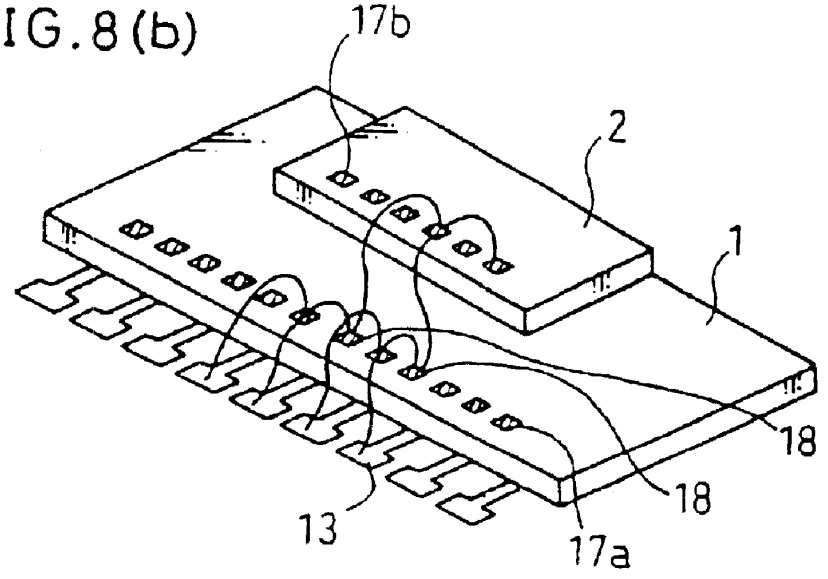


FIG. 9(a)

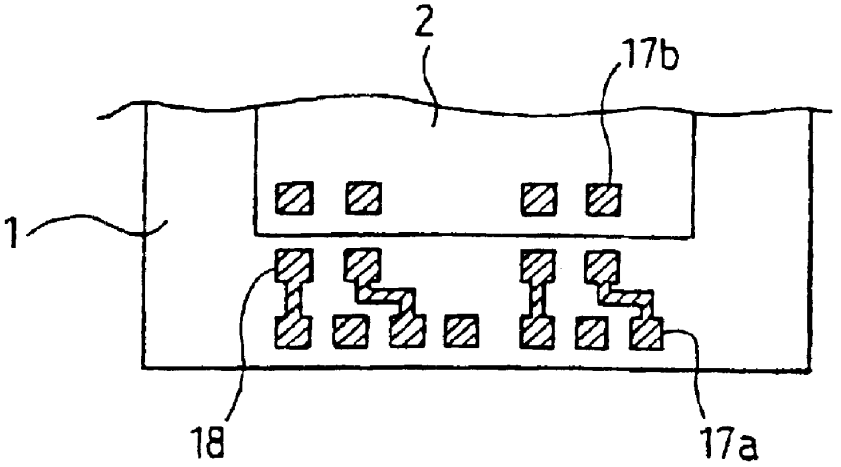


FIG. 9(b)

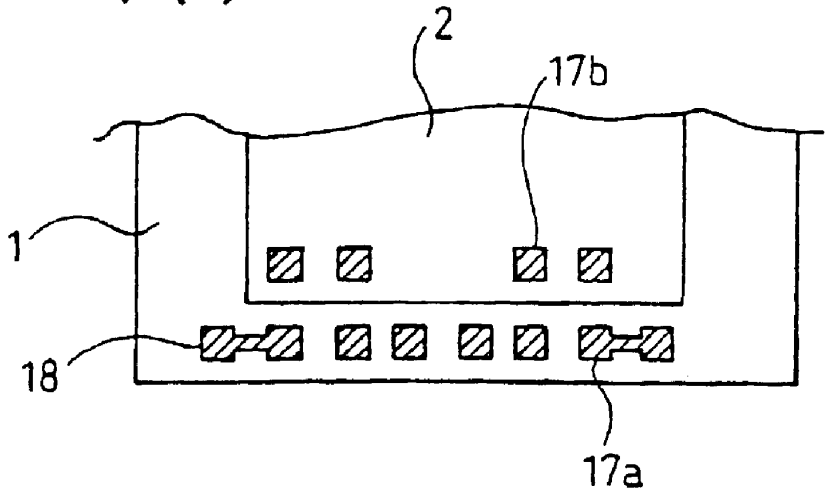


FIG.10

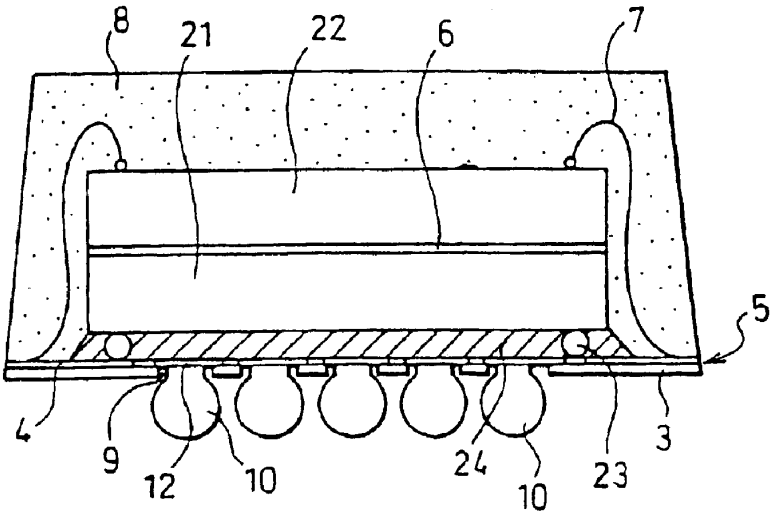


FIG.11(a)

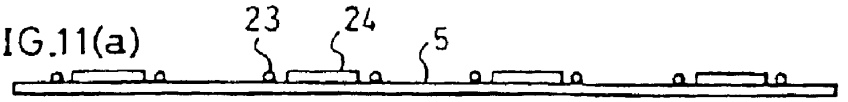


FIG.11(b)

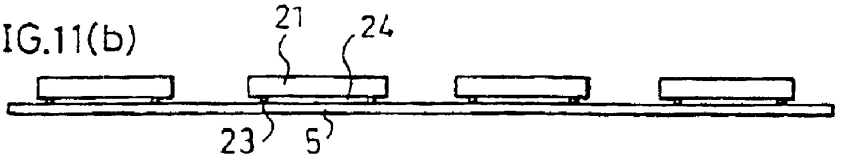


FIG.11(c)

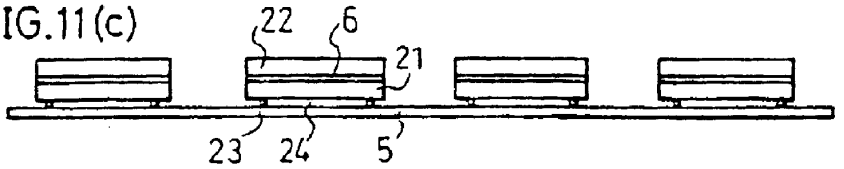


FIG.11(d)

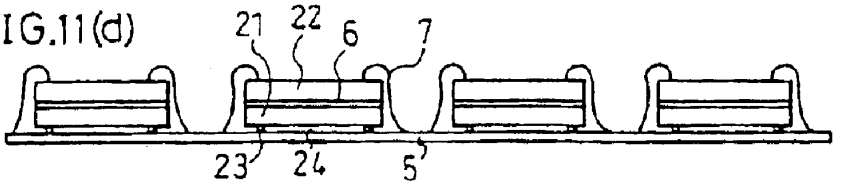


FIG.11(e)

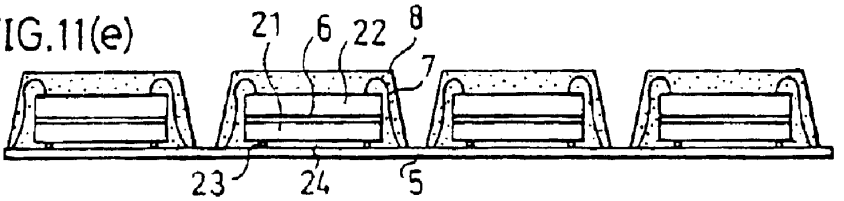


FIG.11(f)

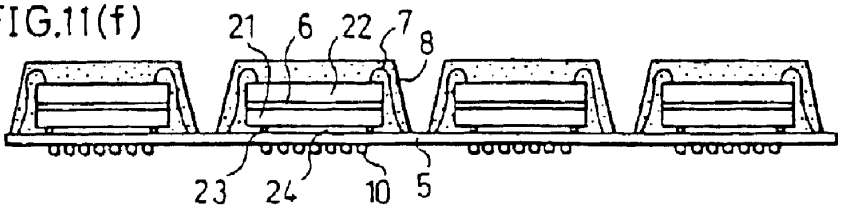


FIG.11(g)

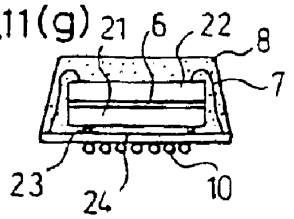


FIG.12(a)

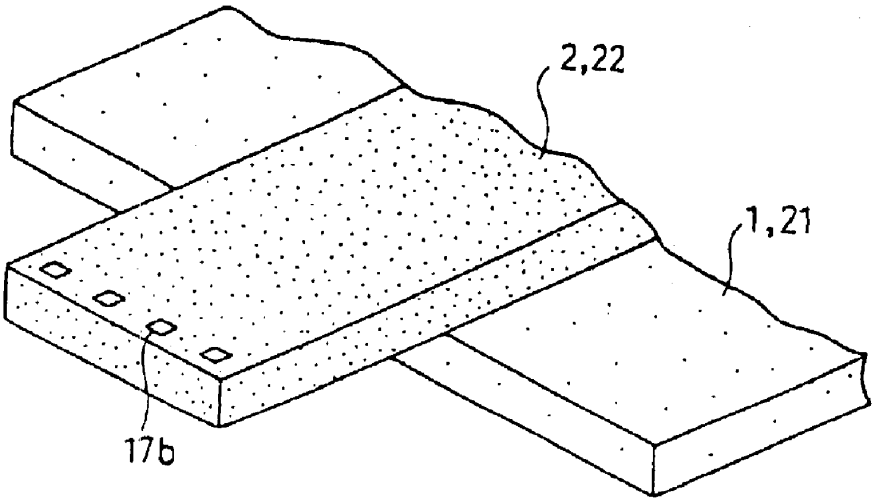


FIG.12(b)

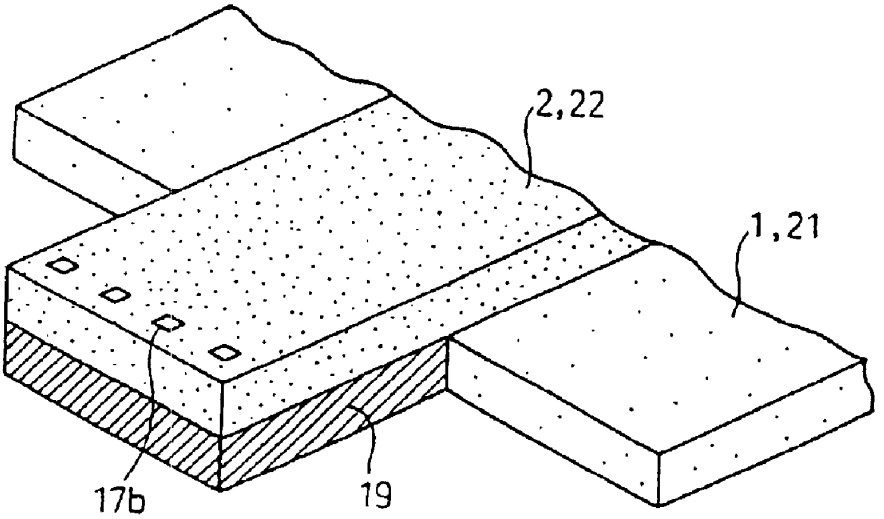


FIG. 13(a)

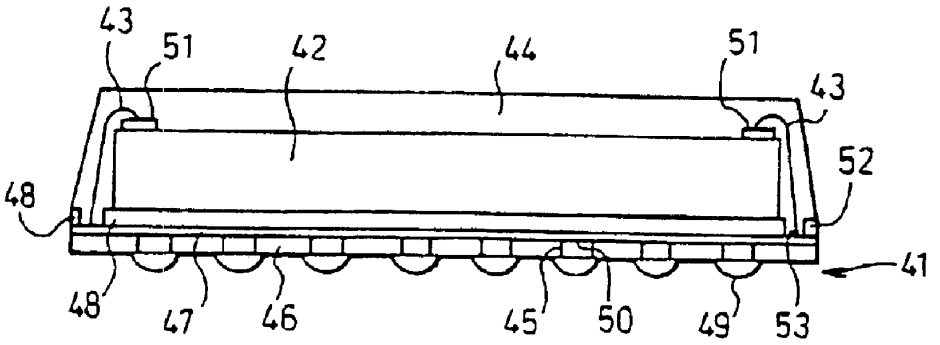


FIG. 13(b)

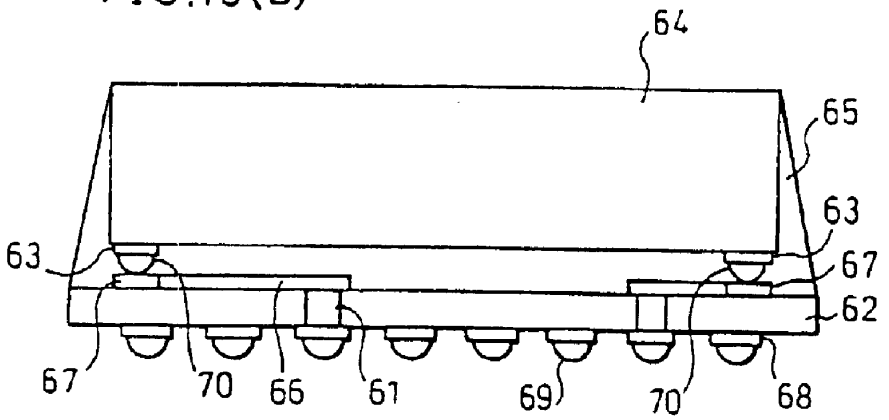


FIG.14(a)

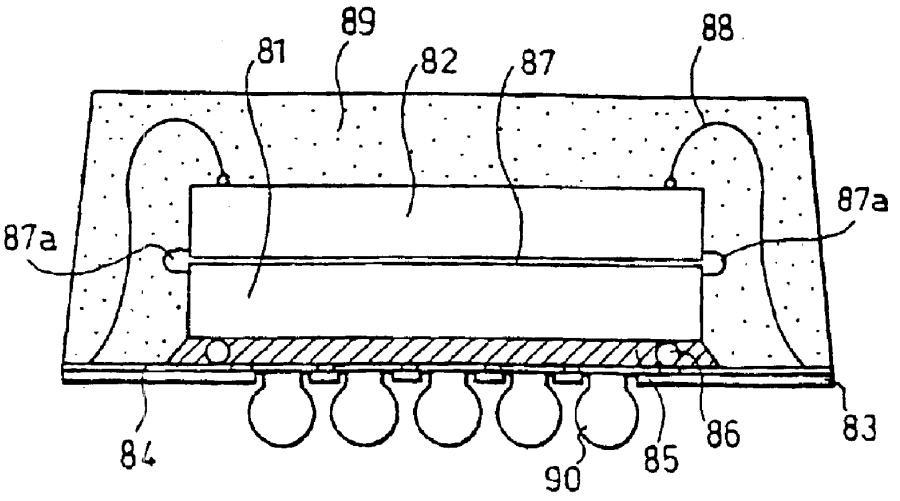


FIG.14(b)

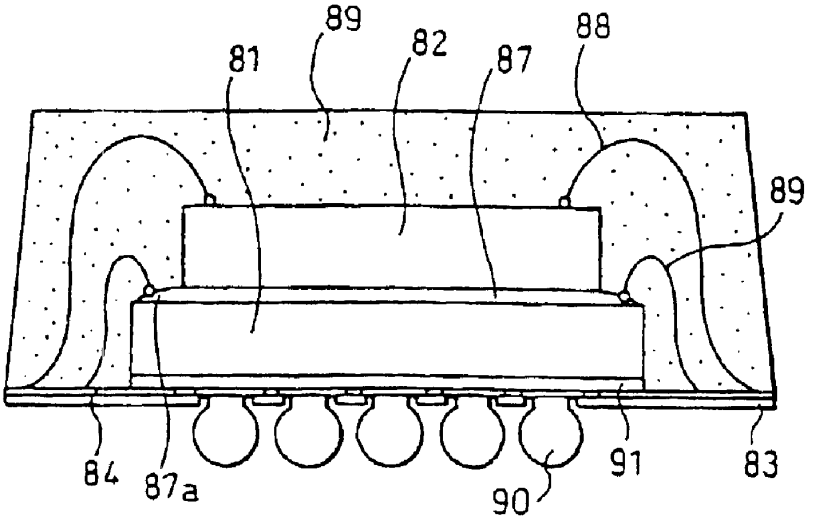
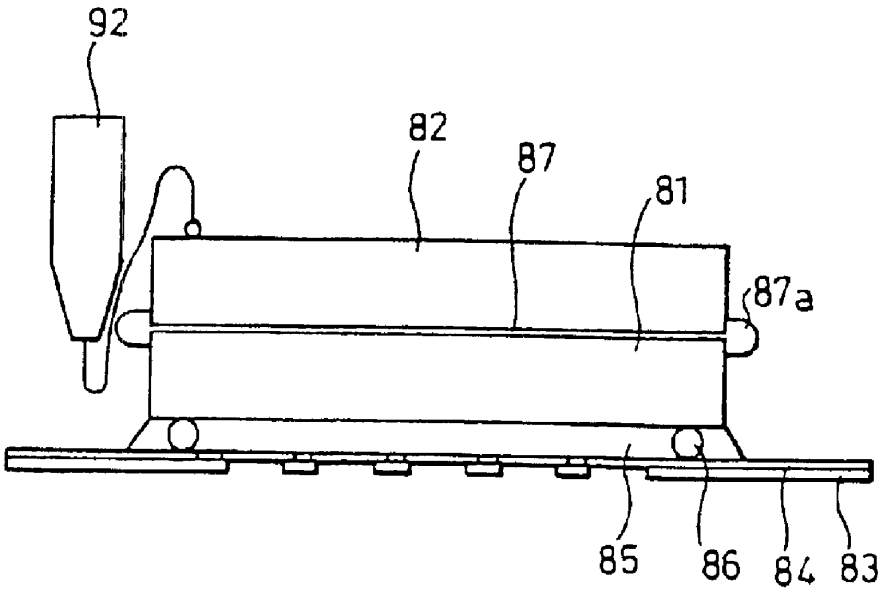


FIG.15



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This is a continuation of application Ser. No. 09/223,272, filed Dec. 30, 1998, now U.S. Pat. No. 6,100,594, the entire content of which is hereby incorporated by reference in this application.

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacturing the same, and more particularly relates to a semiconductor device having a structure substantially miniaturized to a chip size, i.e., a CSP (Chip Size Package) structure, and a method of manufacturing such a semiconductor device.

BACKGROUND OF THE INVENTION

Miniaturization of a semiconductor device is in progress so as to achieve a high-density semiconductor device for use on a printed circuit board. Recently, a semiconductor device substantially miniaturized to a chip size has been developed. The structure of such a miniaturized semiconductor device is called a CSP structure. Japanese Publication of Unexamined Patent Application No. 121002/1997 (Tokukaihei 9-121002) discloses a semiconductor device having the CSP structure shown in FIG. **13**(a). This semiconductor device includes a semiconductor chip **42** disposed with its circuit formed surface facing up, and wires **43** for electrically connecting the semiconductor chip **42** to a wiring pattern **47**. The above publication discloses another semiconductor device having the CSP structure shown in FIG. **13**(b). This semiconductor device includes a semiconductor chip **64** disposed with its circuit formed surface facing down, and a bump electrode **70** for electrically connecting the semiconductor chip **64** to a wiring pattern **66**.

In FIG. **13**(a), **41** is a wiring component, **42** is a semiconductor chip, **43** is a wire, **44** is a resin sealing member, **45** is a throughhole, **46** is a substrate, **47** is a wiring pattern, **48** is an insulating material, **49** is an external connection-use terminal, **50** is an external connection area, **51** is an electrode, **52** is a window opening section, and **53** is an inner connection area. In FIG. **13**(b), **61** is a throughhole, **62** is a wiring component, **63** is an electrode, **64** is a semiconductor chip, **65** is a resin sealing member, **66** is a wiring pattern, **67** is an inner connection area, **68** is an external connection area, **69** is an external connection-use terminal, and **70** is a bump electrode.

In some devices such as portable devices, a plurality of semiconductor chips are mounted in a package so as to increase the added value and capacity of memory, etc. For example, a multi-chip module is provided with a plurality of semiconductor chips arranged parallel to each other in a package. However, such an arrangement makes it impossible to produce a package smaller than the total area of the semiconductor chips to be mounted. In order to solve the problem, a stacked package including a plurality of semiconductor chips laminated in a package to achieve a high packaging density is disclosed in Japanese Publication of Unexamined Patent Application No. 90486/1993 (Tokukaibei 5-90486).

Specifically, the semiconductor devices disclosed in the above publication are each packaged in ceramic packages and arranged in the following manner. In one of the semiconductor devices, a pair of semiconductor chips are adhered to each other with their back surfaces where a circuit is not formed facing each other, and are mounted on another pair of semiconductor chips via metal bumps. In the other semiconductor device, a pair of semiconductor chips are adhered to each other with the circuit formed surface of one semiconductor chip facing the back surface of the other semiconductor chip.

The above-mentioned stacked package is a small high-density semiconductor device. However, a semiconductor device smaller than such a stacked package has been required. For that reason, a semiconductor device having a CSP structure as well as a stacked package structure is required to be produced.

In a semiconductor device having a CSP structure where the semiconductor chips are laminated, an adhesive agent (paste) potting method and a method using a thermo-compression sheet are utilized for bonding the semiconductor chip to the substrate, and for bonding the laminated semiconductor chips to each other.

In the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent spreads beyond the outer edge of the semiconductor chip. For example, as shown in FIG. **14**(a), when bonding semiconductor chips **81** and **82** to each other with their back surfaces facing each other, an adhesive agent **87** between the semiconductor chips **81** and **82** overflows. In addition, as shown in FIG. **15**, in the step of wire-bonding the semiconductor chip **82** disposed on the top to an electrode section of a wiring layer **84** (before a sealing resin **89** and packaging-use external terminals **90** are formed), wiring on an insulating substrate **83** must be provided far from the side surfaces of the semiconductor chips **81** and **82** so as to keep the overflown adhesive agent **87**a from coming into contact with a jig **92** of a wire bonder. Such an arrangement causes the package size to be increased in the end. Furthermore, as shown in FIG. **14**(b), when bonding the back surface of the semiconductor chip **82** to the circuit formed surface of the semiconductor chip **81**, the overflown adhesive agent **87**a may stick to an electrode pad provided on the semiconductor chip **81**.

On the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips **81** and **82**. This gap cannot be filled with the sealing resin **89**, thereby causing problems such as separation of the semiconductor chip **82** from the semiconductor chip **81**.

The method using a thermo-compression sheet requires the steps of placing members at the right locations. Specifically, a thermo-compression sheet having the same size as the semiconductor chip **82** must be placed accurately at a specific location on the semiconductor chip **81**. In addition, the semiconductor chip **82** must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet.

In FIGS. **14**(a) and **14**(b), **85** is an insulating sheet, **86** is a metal bump, and **91** is an adhesive sheet.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a further-miniaturized semiconductor device having a stacked package structure as well as a CSP structure.

In order to achieve the above object, a semiconductor device in accordance with the present invention has a

stacked package structure and a chip size package structure and is characterized in including:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a first insulating adhesion layer adhered to its back surface where a circuit is not formed, the first semiconductor chip being mounted on the wiring layer through the first insulating adhesion layer; and

a second semiconductor chip having a second insulating adhesion layer adhered to its back surface where a circuit is not formed, the second semiconductor chip being mounted on a circuit-formed front surface of the first semiconductor chip through the second insulating adhesion layer;

each of the first and second semiconductor chips being wire-bonded to the electrode section with a wire, the first and second semiconductor chips and the wire being sealed with a resin.

In the above structure, the first semiconductor chip and the second semiconductor chip are each wire-bonded to the electrode section provided on the wiring layer with the wires, and the second insulating adhesion layer is used for affixing the second semiconductor chip to the first semiconductor chip. This structure eliminates the need for wire-bonding the first and second semiconductor chips to points on the wiring layer, far from the side surfaces of the first and second semiconductor chips, considering a situation in which the excessively applied adhesive agent overflows the space between the first and second semiconductor chips. Therefore, a miniaturized, high-density semiconductor device can be realized.

Furthermore, in the case of using a thermo-compression sheet, when mounting the first or second semiconductor chip at a desired location, accurate positioning is required twice, i.e., positioning the thermo-compression sheet, etc., and positioning the first or second semiconductor chip on the thermo-compression sheet. In contrast, the first and second insulating adhesion layers according to the present invention are in advance disposed on the back surfaces of the first and second semiconductor chips, respectively. Therefore, the first or second semiconductor chip can be mounted at a desired location by accurately positioning it once. It is thus possible to miniaturize the semiconductor device without complicating its manufacturing process.

A semiconductor device in accordance with the present invention can be arranged to include:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a circuit formed on its front surface and an insulating adhesion layer adhered to its back surface;

a metal bump, disposed between the first semiconductor chip and the wiring layer, for bump-bonding the front surface of the first semiconductor chip to the wiring layer so that the front surface faces the wiring layer; and

a second semiconductor chip whose back surface where a circuit is not formed is mounted on the back surface of the first semiconductor chip through the insulating adhesion layer;

the second semiconductor chip being wire-bonded to the electrode section of the wiring layer with a wire, the first and second semiconductor chips and the wire being sealed with a resin.

In the above arrangement, the first semiconductor chip is connected to the wiring layer through the metal bump, the second semiconductor chip is wire-bonded to the electrode sections on the wiring layer with wires, and the back surfaces of the first and second semiconductor chips are adhered to each other by the insulating layer. This arrangement eliminates the need for wire-bonding the second semiconductor chip to points on the wiring layer, far from the side surfaces of the first and second semiconductor chips, considering a situation in which the excessively applied adhesive agent overflows the space between the first and second semiconductor chips. Therefore, a miniaturized, high-density semiconductor device can be realized.

In the case of using the thermo-compression sheet, when mounting the second semiconductor chip on the first semiconductor chip, accurate positioning is required twice in a conventional manufacturing method, i.e., positioning the thermo-compression sheet on the first semiconductor chip, and positioning the second semiconductor chip on the thermo-compression sheet. However, the insulating adhesion layer according to the present invention are disposed on the back surface of the second semiconductor chip in advance. Therefore, the second semiconductor chip can be mounted at a desired location on the first semiconductor chip by accurately positioning it once. It is thus possible to miniaturize the semiconductor chip without complicating its manufacturing process.

A method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:

(a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;

(b) producing separate first semiconductor chips from the first wafer by dicing;

(c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;

(d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;

(e) producing separate second semiconductor chips from the second wafer by dicing;

(f) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;

(g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;

(h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and

(i) sealing the first and semiconductor chips and the wires.

With the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface in advance when being in the wafer state, the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip. It is thus possible to simplify the process of manufacturing the semiconductor chip.

Moreover, in the above manufacturing method, the adhesive agent does not overflow the space between the first and second semiconductor chips, the first and second semiconductor chips can be wire-bonded to the wiring layer at a location closer to the edges of the first and second semiconductor chips. It is thus possible to realize a miniaturized, high-density semiconductor device.

A method of manufacturing a semiconductor device in accordance with the present invention including the steps of:

(a) forming an insulating layer and a metal bump on a wiring layer;

(b) mounting a first semiconductor chip on the wiring layer with its circuit-formed surface facing the wiring layer;

(c) forming an insulating adhesion layer on a back surface of a wafer having a circuit formed on its front surface;

(d) producing separate second semiconductor chips from the wafer by dicing;

(e) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;

(f) wire-bonding the second semiconductor chip to the wiring layer with a wire; and

(g) sealing the first and second semiconductor chips and the wire.

In this manufacturing method, like the above-mentioned method of the present invention, since the second semiconductor chip has the insulating adhesion layer adhered to its back surface in advance when being in the wafer state, the second semiconductor chip can be mounted at a desired location without the step of accurately positioning the insulating adhesion layer on the second semiconductor chip. It is thus possible to simplify the process of manufacturing the semiconductor chip.

Furthermore, in the above manufacturing method, the adhesive agent does not overflow the space between the first and second semiconductor chips, the second semiconductor chip can be wire-bonded to the wiring layer at a location closer to the edges of the first and second semiconductor chips. It is thus possible to realize a miniaturized, high-density semiconductor device.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a semiconductor device in accordance with the first embodiment of the present invention.

FIG. **2**(a) is a plan view of a circuit board before being cut, and FIG. **2**(b) is a partially enlarged view of the circuit board shown in FIG. **2**(a).

FIG. **3**(a) is an explanatory view showing an arrangement of ball-like external connection-use terminals, and FIG. **3**(b) is an explanatory view showing an arrangement of trapezoidal external connection-use terminals.

FIG. **4** is an explanatory view showing how laminated semiconductor chips are each wire-bonded to the circuit board.

FIGS. **5**(a) to **5**(g) show one example of a process of manufacturing the semiconductor device.

FIG. **6**(a) is a partially enlarged view of the circuit board including a wiring layer disposed on one surface of an insulating substrate, and FIG. **6**(b) is a partially enlarged view of a circuit board including a wiring layer disposed on each surface of the insulating substrate.

FIG. **7**(a) is an explanatory view showing a wiring state when two laminated semiconductor chips are connected to the same electrode section, and FIG. **7**(b) is an explanatory view showing another state that the two laminated semiconductor chips are connected to the same electrode section.

FIG. **8**(a) is an explanatory view showing a wiring state that the two laminated semiconductor chips are connected to different electrode sections, and FIG. **8**(b) is an explanatory view showing another wiring state that the two laminated semiconductor chips are connected to different electrode sections.

FIG. **9**(a) is an explanatory view showing one example of an arrangement of dummy pads formed on a first semiconductor chip, and FIG. **9**(b) is an explanatory view showing another example of the arrangement of the dummy pads disposed on the first semiconductor chip.

FIG. **10** is a cross-sectional view of a semiconductor device in accordance with the second embodiment of the present invention.

FIGS. **11**(a) to **11**(g) show one example of a process for manufacturing the semiconductor device.

FIG. **12**(a) is a perspective view showing that a second semiconductor chip in the semiconductor device in accordance with the first embodiment or the second embodiment protrudes from a first semiconductor chip, and FIG. **12**(b) is a perspective view showing that the second semiconductor chip is reinforced.

FIG. **13**(a) is a cross-sectional view showing a semiconductor device having a CSP structure manufactured by a conventional wire bonding method, and FIG. **13**(b) is a cross-sectional view showing a semiconductor device having a CSP structure manufactured by a conventional face-down bonding method.

FIGS. **14**(a) and **14**(b) are cross-sectional views of conventional semiconductor devices having a stacked package structure.

FIG. **15** is a cross-sectional view of the semiconductor device shown in FIG. **14**(a) during manufacturing.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

The following descriptions will explain one embodiment of the present invention with reference to FIGS. **1** to **9**.

As shown in FIG. **1**, in a semiconductor device according to this embodiment, a first semiconductor chip **1** and a second semiconductor chip **2** are laminated in this order on a circuit board **5** including an insulating substrate **3** and a wiring layer **4** mounted on the insulating substrate **3**. Regarding the first semiconductor chip **1** and the second semiconductor chip **2**, the surface (front surface) on which an element is formed is hereinafter referred to as a "circuit formed surface", and the surface opposite thereto is referred to as a "back surface".

The semiconductor chip **1** is disposed with its back surface facing the insulating substrate **3**. The second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1** through a thermo-compression sheet (adhesion layer) **6** so that its back surface is adhered to the thermo-compression sheet **6**.

The semiconductor device in accordance with the present embodiment is arranged so that the second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1**. With this arrangement, the second semiconductor chip **2** on the top of the first semiconductor chip **1** does not influence (interfere with) electrode pads of the first semiconductor chip **1**. The circuit formed surface of the first semiconductor chip **1** is in advance coated with an insulating-resin, etc. Namely, the coating is applied to the circuit formed surface of the first semiconductor chip **1** by a spin coating method, etc. when the first semiconductor chip **1** is in a wafer state before subjected to dicing. In this case, the coating material on the electrode pads (not shown) disposed on the circuit formed surface of the first semiconductor chip **1** is removed.

The first semiconductor chip **1** and the second semiconductor chip **2** are each connected (wire-bonded) to electrode sections of the wiring layer **4** on the insulating substrate **3** with wires **7**.

The first semiconductor chip **1**, the second semiconductor chip **2** and the wires **7**, arranged as above, are covered by a sealing resin **8**.

The insulating substrate **3** includes via holes **9** at the locations corresponding to below-described land sections **12** constituting the wiring layer **4**. Ball-like packaging-use external terminals **10** are connected in an area-array-like arrangement to the land sections **12** through the via holes **9** from the side of the insulating substrate **3**, on which side the first semiconductor chip **1** and the second semiconductor chip **2** are not formed.

Next, the following descriptions will explain in further detail the above-mentioned members constituting the semiconductor device in accordance with the present embodiment.

FIG. **2**(a) is a plan view of the circuit board **5** before being cut in the process of manufacturing the semiconductor device. As shown in FIG. **2**(a), four guide holes **11** are formed in both side sections of the insulating substrate **3** (the upper part and the lower part of the insulating substrate **3** in FIG. **2**(a)) of the circuit board **5** before being cut. The guide holes **11**a formed in one of the side section and the guide holes **11**b formed in the other side section have different shapes. These guide holes **11** are used for transporting the semiconductor device during its manufacturing process.

The material of the insulating substrate **3** is not particularly limited, and a resin substrate or a film having excellent heat resistance is acceptable. The insulating material **3** may be a resin substrate, etc. made of, for example, polyimide, epoxy resin containing glass fiber, bismaleid triazine (BT) resin, polyester, polyamide, fluororesin, ceramic, and polyester containing glass fiber. Polyimide is the most preferable of the above materials.

FIG. **2**(b) is a partially enlarged view of the circuit board **5** shown in FIG. **2**(a), showing the structure of the wiring layer **4**. As shown in FIG. **2**(b), the wiring layer **4** includes the land sections **12**, electrode sections **13**, and wiring sections **14**, disposed on the insulating substrate **3**. Each of the wiring sections **14** connects the land section **12** to the electrode section **13**.

The electrode sections **13** are formed on both ends of the wiring layer **4** (the left part and the right part of the wiring layer **4** in FIG. **2**(b)). As explained in detail later, each of the electrode section **13** is connected to the first semiconductor chip **1** or the second semiconductor chip **2** by the wire **7**. Therefore, the electrode sections **13** are located outside the area of the wiring layer **4**, where the first semiconductor chip **1** and the second semiconductor chip **2** are mounted.

The land section **12** is a packaging-use external terminal forming section for connecting the packaging-use external terminal **10** and the wiring layer **4** through the via hole **9** of the insulating substrate **3**.

The first semiconductor chip **1** can be completely insulated from the wiring layer **4** by, for example, providing a sheet of an insulating resin on an area of the wiring layer **4** where the first semiconductor chip **1** is to be mounted or applying an insulating resin coating to the area of the wiring layer **4**. The wiring layer **4** is made of copper (Cu), aluminum (Al), gold (Au), nickel (Ni), and other materials. Cu is particularly preferable because it is less costly. Methods of forming the wiring layer **4** on the insulating substrate **3** include a vapor deposition method and a plating method. In order to pattern the wiring layer **4** to form a desired pattern, a conventional photolithography method can be utilized.

FIG. **3**(a) is a view seen from the back side of the semiconductor device shown in FIG. **1**, i.e., the side where the packaging-use external terminals **10** are disposed. As shown in FIG. **3**(a), ball-like packaging-use external terminals **10** are disposed in an area-array-like arrangement, and connected to the land sections **12** provided on the wiring layer **4**. The packaging-use external terminals **10** are not limited to a ball-like shape, and may have a trapezoidal shape as shown in FIG. **3**(b).

Each of the wires **7** is used for connecting the electrode pad disposed on the first semiconductor chip **1** or the second semiconductor chip **2** to the electrode section **13** of the wiring layer **4**. In a conventional semiconductor device, a gold ball provided on only one end of the wire is in contact with the electrode pad of the first semiconductor chip or the second semiconductor chip, and the other end of the wire is connected to the electrode section of the wiring layer on the insulating substrate. Here, the gold ball can be provided on only one end of the wire. The gold ball is brought into contact with the electrode pad by imposing a load lighter than the load applied in connecting, by thermo-compression bonding, the wire to the electrode section of the wiring layer on the insulating substrate. This is because connecting the wires to the semiconductor chips by thermo-compression bonding, i.e., by application of a heavy load, increases the possibility of damaging the semiconductor chips.

However, the above conventional arrangement has the following problem. Namely, the wires, especially those connected to the second semiconductor chip, are connected to the electrode sections of the wiring layer provided on the circuit board at a small angle with respect to the circuit board. Therefore, the wire is connected to the circuit board, far from the end of the first semiconductor chip.

In order to solve the problem, in the semiconductor device according to the present embodiment, the first semiconductor chip **1** and the second semiconductor chip **2** are each wire-bonded to the circuit board **5** as shown in FIG. **4**. The first semiconductor chip **1** and the circuit board **5** are wire-bonded in the same manner as the conventional semiconductor device. Then, the wire **7** is connected to the circuit board **5** with a gold ball **7**a provided on one end of the wire **7**. Thereafter, the other end of the wire **7** is connected, by thermo-compression boding, to a gold bump **16** formed on the electrode pad of the second semiconductor chip **2** in advance so as to connect the second semiconductor chip **2** to the circuit board **5**.

Since wire-bonding between the second semiconductor chip **2** and the circuit board **5** is performed as above, the wire **7** connected to the second semiconductor chip **2** is connected to the circuit board **5** at an angle closer to 90° with respect to the circuit board **5**. Therefore, the wire **7** is connected to the circuit board **5** at a closer location to the end of the first semiconductor chip **1**, thereby enabling further miniaturization of the semiconductor device in accordance with the present embodiment.

The wire **7** is connected to the gold bump **16** by thermo-compression bonding by a load nearly equal to the load applied when connecting the wire **7** to the electrode section of the wiring layer **4** on the insulating substrate **3** by thermo-compression bonding. However, by using the gold bump **16**, the stress applied to the second semiconductor chip **2** can be lowered. It is thus possible to reduce the possibility that the second semiconductor chip **2** is damaged by a heavy load applied thereto.

The gold bump **16** is formed by connecting a gold ball, provided on the end of the wire by the conventional method, to the electrode pad on the second semiconductor chip **2**, and then cutting the wire **7**. Thereafter, by making the upper surface of the gold bump **16** flat with a stamping jig, the wire **7** can be surely affixed to the gold bump **16** by thermo-compression bonding.

Note that the first semiconductor chip **1** and the circuit board **5** can be wire-bonded to each other in the same manner as the above-mentioned wire-bonding of the second semiconductor chip **2** and the circuit board **5**.

The following descriptions will explain one example of the process (including steps (1) to (5)) for manufacturing the semiconductor device in accordance with the present embodiment with reference to FIGS. **5**(a) to **5**(g).

(1) First, the first semiconductor chip **1** is mounted on the circuit board **5** (see FIG. **5**(a)). When the first semiconductor chip **1** is in a wafer state, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips **1**. The first semiconductor chip **1** is mounted on the circuit board **5** at a location inside a mount location recognition-use mark **15** provided on the circuit board **5**. Here, instead of providing the thermo-compression sheet **6** in advance when the first semiconductor chip **1** is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board **5** before the first semiconductor chip **1** is mounted on the circuit board **5**.

(2) Next, the second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1** (see FIG. **5**(b)). When the second semiconductor chip **2** is in the wafer state, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer, and then the wafer is cut to produce separate pieces of second semiconductor chips **2**. The second semiconductor chip **2** is accurately positioned at a specific location on the circuit formed surface of the first semiconductor chip **1**.

By affixing the thermo-compression sheet **6** to the back surface of the second semiconductor chip **2** in advance, accurate positioning is necessary only when mounting the second semiconductor chip **2** on the first semiconductor chip **1**. Therefore, since one step requiring accurate positioning is omitted in the process for manufacturing the semiconductor device in accordance with the present embodiment, this manufacturing process is simplified compared with the conventional process in which the thermo-compression sheet **6** is disposed on the circuit formed surface of the first semiconductor chip **1**, and then the second semiconductor chip **2** is adhered to the thermo-compression sheet **6**.

(3) Then, each of the electrode pads (not shown) disposed on the first semiconductor chip **1** and the second semiconductor chip **2** is connected, with the wire **7** made of Au, to the electrode section **13** formed in the wiring layer **4** on the circuit board **5**. More specifically, the first semiconductor chip **1** and the wiring layer **4** are first electrically connected to each other (see FIG. **5**(c)), and then the second semiconductor chip **2** and the wiring layer **4** are electrically connected to each other (see FIG. **5**(d)). Since the first semiconductor chip **1** and the second semiconductor chip **2** are each electrically connected to the wiring layer **4** in the above order, it is possible to avoid such a problem that the wire **7** for connecting the first semiconductor chip **1** to the circuit board **5** and the wire **7** for connecting the second semiconductor chip **2** to the circuit board **5** across each other, and prevent connection of the first semiconductor chip **1** to the circuit board **5**.

(4) Thereafter, each of the packaging-use external terminals **10** is disposed on the location where the via hole **9** is provided on the insulating substrate **3** on the circuit board **5** (see FIG. **5**(f)). Here, positioning the packaging-use external terminal **10** is performed in such a manner that a solder ball is temporarily fixed to each via hole **9**, heated in a reflow furnace, and then joined to the land section **12**. Methods of temporarily fixing the solder ball to the via hole **9** include a method in which the solder ball is affixed to the via hole **9** after applying a flux to the via hole **9**, and a method in which the solder ball is affixed to the via hole **9** after adhering the flux to the solder ball.

(5) Finally, a plurality of semiconductor devices produced on the circuit board **5** are divided into pieces of semiconductor devices (see FIG. **5**(d)) by cutting the insulating substrate **3** along its unnecessary part, i.e., along the outer edge of the sealing resin **8** of each semiconductor device. Methods of cutting the insulating substrate **3** include a punching method using die, and an eximer laser cutting method.

As shown in FIG. **6**(a), the semiconductor device in accordance with the present embodiment includes the wiring layer **4** on only one of the surfaces of the insulating substrate **3**. However, the wiring layer **4** can be provided on both surfaces of the insulating substrate **3** as shown in FIG. **6**(b).

When the wiring layer **4** is formed on both surfaces of the insulating substrate **3**, as shown in FIG. **6**(b), the wiring layers **4** on the respective surfaces are electrically connected to each other through the plated via holes **9** as shown in FIG. **6**(b). Regarding the wiring layer **4** on the side of the insulating substrate **3**, the side where the first semiconductor chip **1** is not mounted, the area where the packaging-use external terminals **10** are not to be formed are covered with a solder resist **20**, etc. In the area which is not covered with the solder resist **20**, i.e., the area where the packaging-use external terminals **10** are to be provided, the packaging-use external terminals **10** are arranged in an area-array-like pattern.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to the electrode sections **13** of the wiring layer **4** with the wires **7**, if the wires **7** become too close to each other because of the layout of the electrode pads of the first semiconductor chip **1** and the second semiconductor chip **2**, the wires **7** can be arranged as below.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to the same electrode section **13** of the wiring layer **4**, two arrangements shown in FIGS. **7**(a) and **7**(b) are acceptable. In the arrangement shown in FIG. **7**(a), the electrode section **13** of the wiring layer **4**, to which two wires **7** are connected, is arranged to have two parts. In the arrangement shown in FIG. **7**(b), an electrode pad **17**a of the first semiconductor chip **1** is connected to an electrode pad **17**b of the second semiconductor chip **2** with the wire **7**, and the electrode pad **17**a is connected to the electrode section **13** of the wiring layer **4** with the wire **7**, thereby connecting each of the electrode pads **17**a and **17**b to the electrode section **13**.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to different electrode sections **13** of the wiring layer **4**, two arrangements shown in FIGS. **8**(a) and **8**(b) are acceptable. In the arrangement shown in FIG. **8**(a), the electrode pad **17**a of the first semiconductor chip **1** and the electrode pad **17**b of the second semiconductor chip **2** are each connected directly to the electrode section **13** of the wiring layer **4** with the wire **7**. In the arrangement shown in FIG. **8**(b), dummy pads **18** are

provided on the first semiconductor chip **1**, and the electrode pad **17**b disposed on the second semiconductor chip **2** is connected to the electrode section **13** of the wiring layer **4** via the dummy pad **18**. This arrangement shown in FIG. **8**(b) is more preferable because the overhanging part of the wire **7** is shorter than that in the arrangement shown in FIG. **8**(a).

FIGS. **9**(a) and **9**(b) show examples of the arrangement of the dummy pads **18** provided on the first semiconductor chip **1**.

Embodiment 2

With reference to FIGS. **10** to **12**, the following descriptions will explain the second embodiment of the present invention. The members having the same structure as those in the above-mentioned first embodiment will be designated by the same reference numbers and their description will be omitted.

A semiconductor device in accordance with the present embodiment is arranged as shown in FIG. **10**. Specifically, a first semiconductor chip **21** is mounted on a circuit board **5** with its circuit formed surface facing the circuit board **5**, i.e., facing down. The circuit board **5** includes an insulating substrate **3**, and a wiring layer **4** formed on the insulating substrate **3**. A second semiconductor chip **22** is mounted on the back surface of the first semiconductor chip **21** through a thermo-compression sheet **6**. The back surface of the second semiconductor chip **22** faces the first semiconductor chip **21**. Namely, the back surfaces of the first semiconductor chip **21** and the second semiconductor chip **22** are adhered to each other through the thermo-compression sheet **6**. The thermo-compression sheet **6** is provided as an adhesion layer for holding the second semiconductor chip **22** on the first semiconductor chip **21**.

The first semiconductor chip **21** is electrically connected to first electrode sections (not shown) provided in the wiring layer **4** through metal bumps **23**. The first electrode sections are disposed inside an area of the wiring layer **4**, where the first semiconductor chip **21** is mounted.

Meanwhile, the second semiconductor chip **22** is electrically connected to second electrode sections (not shown) provided in the wiring layer **4** with wires **7**. Since the second electrode sections are used for wire-bonding the second semiconductor chip **22** to the wiring layer **4**, they are disposed outside the area of the wiring layer **4**, where the first semiconductor chip **21** and the second semiconductor chip **22** are mounted.

A resin sheet **24** is provided between the first semiconductor chip **21** and the wiring layer **4**. The resin sheet **24** is formed by extending a resin sheet used in the step of connecting the first semiconductor chip **21** to the wiring layer **4** through the metal bumps **23**.

If electrode pads provided on the circuit formed surface of the first semiconductor chip **21** are made of Al, the metal bumps **23** are preferably made of Au which is easily alloyed with Al. With this arrangement, the metal bumps **23** can be more firmly affixed to the electrode pads.

The material for forming the resin sheet **24** may be a thermoplastic resin or a thermosetting resin. However, the thermoplastic resin is more favorable than the thermosetting resin because the resin sheet **24** is used for the following purpose. Namely, it is used so that the resin extends by heat applied in connecting the first semiconductor chip **21** to the wiring layer **4** with the metal bumps **23**, covers the metal bumps **23** as junctions, and prevents degradation of the junctions caused by shock, etc.

The resin sheet **24** can be a three-layer resin sheet including a layer of a light blocking material such as metallic foil. With this arrangement, it is possible to prevent a malfunction of the first semiconductor chip **21** due to a light incident from the surface where the packaging-use external terminals **10** are mounted passing through the semiconductor device. In this case, the size of the metallic foil must be such that the metallic foil is out of contact with the metal bumps **23**.

Although the semiconductor device in accordance with the present embodiment uses the resin sheet **24**, the following arrangement is also acceptable. Namely, the semiconductor chip **21** is mounted without using the resin sheet **24**, and then the space produced at a junction of the first semiconductor chip **21** and the wiring layer **4** is filled with a liquid resin, etc., thereby covering the metal bumps **23** as the junctions.

Next, referring to FIGS. **11**(a) to **11**(g), the following descriptions will explain the process (including steps (1) to (7)) for manufacturing the semiconductor device in accordance with the present embodiment.

(1) First, the resin sheet **24** and the metal bumps **23** are disposed on the circuit board **5** (see FIG. **11**(a)). In this case, each of the metal bumps **23** is disposed on the first electrode section provided in the wiring layer **4** on the circuit board **5**. The resin sheet **24** is disposed on the circuit board **5** at the location where the first semiconductor chip **21** and the second semiconductor chip **22** are to be mounted.

(2) Next, the first semiconductor chip **21** is connected to the wiring layer **4** on the circuit board **5** by a flip chip method in a face-down mode (see FIG. **11**(b)).

(3) Then, the second semiconductor chip **22** is mounted on the back surface of the first semiconductor chip **21** (see FIG. **11**(c)). When the second semiconductor chip **22** is in a state of wafer, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips **22**. The second semiconductor chip **22** is accurately positioned at a specific location on the circuit formed surface of the first semiconductor chip **21**.

Like the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet **6** to the back surface of the second semiconductor chip **22** in advance.

(4) Then, the second semiconductor chip **22** is electrically connected to the wiring layer **4** on the circuit board **5** (see FIG. **11**(d)). more specifically, each of the electrode pads disposed on the circuit formed surface of the second semiconductor chip **22** is connected to the second electrode section of the wiring layer **4** with the wire **7**.

(5) Thereafter, the first semiconductor chip **21**, the second semiconductor chip **22**, and the wires **7**, provided on the circuit board **5**, are sealed with a sealing resin **8** (see FIG. **11**(e)). The method of forming the sealing resin **8** is similar to that described in the first embodiment.

(6) Then, each of the packaging-use external terminals **10** is disposed at a location of a via hole **9** formed in the insulating substrate **3** of the circuit board **5** (see FIG. **11**(f)).

(7) Finally, a plurality of semiconductor devices produced on the circuit board **5** are divided into pieces of semiconductor devices by cutting the insulating substrate **3** along the unnecessary part of the insulating substrate **3** of the circuit board **5**, i.e., along the outer edge of the sealing resin **8** of each semiconductor device unnecessary parts (see FIG. **11**(d)). The methods of cutting the insulating substrate **3** including a punching method using a die, and an eximer laser method.

In the above-described first embodiment (and in the second embodiment), when mounting the second semiconductor chips **2** (**22**) on the first semiconductor chips **1** (**21**), if the first semiconductor chips **1** (**21**) and the second semiconductor chips **2** (**22**) have different shapes, the second semiconductor chips **2** (**22**) may protrude from the first semiconductor chips **1** (**21**) as shown in FIG. **12**(a). In this case, since the protruded part of the second semiconductor chip **2** (**22**) is of low strength, the second semiconductor chip **2** (**22**) may be possibly destroyed by shock produced when, for example, wire-bonding the electrode pads **17**b of the second semiconductor chip **2** (**22**) to the wiring layer **4**.

In order to solve the problem, as shown in FIG. **12**(b), a support member **19** having the same height and the same shape as the first semiconductor device **1** (**21**) is fixed under the protruded part of the second semiconductor chip **2** (**22**). By reinforcing the second semiconductor chip **2** (**22**) with the support member **19**, destruction thereof can be prevented. The support member **19** is preferably made of Silicon (Si) in order to reduce generation of stress, etc. against a heat load applied during and after manufacturing the semiconductor device with the CSP structure. In addition, the support member **19** has the same coefficient of linear expansion as the second semiconductor chip **2** (**22**).

The above-mentioned semiconductor devices in accordance with Embodiments 1 and 2 include two laminated semiconductor chips. However, the present invention can be arranged to include three or more laminated semiconductor chips. In this case, the third semiconductor chip can be mounted on the top of the two semiconductor chips with its circuit formed surface facing up and wire-bonded to the wiring layer **4**. Alternatively, the third semiconductor chip can be mounted on the top of the two semiconductor chips with its circuit formed surface facing down through metal bumps by providing electrode pads for disposing the metal bumps on the circuit formed surface of the second semiconductor chip **2** (**22**).

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. A semiconductor device including a stacked package structure and a chip size package structure, comprising:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first **[**insulating**]** adhesion layer; and

a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second **[**insulating**]** adhesion layer;

each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

2. A semiconductor device including a stacked package structure and a chip size package structure, comprising:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a paste applied to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through said paste; and

a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer;

each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

3. A semiconductor device comprising:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a circuit forming on its front surface and an adhesion layer adhered to its back surface;

a metal bump, disposed between said first semiconductor chip and said wiring layer, for bump-bonding the front surface of said first semiconductor chip to said wiring layer so that the front surface faces said wiring layer; and

a second semiconductor chip whose back surface where a circuit is not formed is mounted on the back surface of said first semiconductor chip through the adhesion layer;

said second semiconductor chip being wire-bonded to the electrode section of said wiring layer with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

4. The semiconductor device as set forth in claim **3**,

wherein the back surfaces of said first and second semiconductor chips have a same shape.

5. The semiconductor device as set forth in claim **3**, further comprising a light blocking layer, disposed between said first semiconductor chip and said wiring layer, for blocking a light incident from said insulating substrate.

6. The semiconductor device as set forth in claim **1**,

wherein, when said first and second semiconductor chips have different shapes, a support member is used for supporting and fixing a protruding part of the back surface of said second semiconductor chip, which is not facing said first semiconductor chip, said support member having a same shape as the protruding part.

7. The semiconductor device as set forth in claim **2**,

wherein, when said first and second semiconductor chips have different shapes, a support member is used for supporting and fixing a protruding part of the back surface of said second semiconductor chip, which is not facing said first semiconductor chip, said support member having a same shape as the protruding part.

8. The semiconductor device as set forth in claim **3**,

wherein, when said first and second semiconductor chips have different shapes, a support member is used for supporting and fixing a protruding part of the back surface of said second semiconductor chip, which is not facing said first semiconductor chip, said support member having a same shape as the protruding part.

9. The semiconductor device as set forth in claim **6**,

wherein said support member has a same coefficient of linear expansion as said second semiconductor chip.

10. The semiconductor device as set forth in claim **7**,

wherein said support member has a same coefficient of linear expansion as said second semiconductor chip.

11. The semiconductor device as set forth in claim **8**, wherein said support member has a same coefficient of linear expansion as said second semiconductor chip.

12. The semiconductor device as set forth in claim **1**, wherein one end of the wire for connecting said first semiconductor chip to said wiring layer and the wire for connecting said second semiconductor chip to said wiring layer are connected in a first electrode pad disposed on said first semiconductor chip and a second electrode pad disposed on said second semiconductor chip, respectively, and the other ends of the wires are connected to the electrode sections of said wiring layer.

13. The semiconductor device as set forth in claim **2**, wherein one end of the wire for connecting said first semiconductor chip to said wiring layer and the wire for connecting said second semiconductor chip to said wiring layer are connected to a first electrode pad disposed on said first semiconductor chip and a second electrode pad disposed on said second semiconductor chip, respectively, and the other ends of the wires are connected to the electrode sections of said wiring layer.

14. The semiconductor device as set forth in claim **12**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire and when the other ends of the first and second wires are bonded to the same electrode section, the electrode section is arranged to have a first electrode portion to which the first electrode pad is connected with the first wire and a second electrode portion to which the second electrode pad is connected with the second wire.

15. The semiconductor device as set forth in claim **13**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire, and when the other ends of the first and second wires are bonded to the same electrode section, the electrode section is arranged to have a first electrode portion to which the first electrode pad is connected with the first wire and a second electrode portion to which the second electrode pad is connected with the second wire.

16. The semiconductor device as set forth in claim **12**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire, and when the first and second electrode pads are bonded to the same electrode section, the first and second electrode pads are connected to each other by connecting the other end of the second wire to the first electrode pad, and the first electrode pad is connected to the electrode section with the first wire.

17. The semiconductor device as set forth in claim **13**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire, and when the first and second electrode pads are bonded to the same electrode section, the first and second electrode pads are connected to each other by connecting the other end of the second wire to the first electrode pad, and the first electrode pad is connected to the electrode section with the first wire.

18. The semiconductor device as set forth in claim **12**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire, and when the other ends of the first and second wires are bonded to different electrode sections, a dummy pad is provided on the first semiconductor chip so as to connect the second electrode pad to said wiring layer with the second wire via the dummy pad.

19. The semiconductor device as set forth in claim **13**, wherein the wire connected to the first electrode pad in one end is a first wire and the wire connected to the second electrode pad in one end is a second wire, and when the other ends of the first and second wires are bonded to different electrode sections, a dummy pad is provided on the first semiconductor chip so as to connect the second electrode pad to said wiring layer with the second wire via the dummy pad.

20. The semiconductor device as set forth in claim **3**, further comprising an insulating layer for preventing degradation of said metal bump, said insulating layer being disposed between said first semiconductor chip and said wiring layer.

21. The semiconductor device as set forth in claim **20**, wherein said insulating layer includes a layer having a light blocking property and a size arranged so as not to come into contact with said metal bump.

22. The semiconductor device as set forth in claim **3**, further comprising a filling material for preventing degradation of said metal bump, said filling material being filled between said first semiconductor chip and said wiring layer.

23. A semiconductor device comprising:

an insulating substrate including a wiring layer on its surface and a packaging-use external terminal on its back surface, the wiring layer having an electrode section, the packaging-use external terminal being electrically connected to said wiring layer through a via hole;

a first semiconductor chip produced by forming a first adhesion layer on a back surface of a wafer having a desired circuit formed on its front surface and by dicing the wafer, said first semiconductor chip being mounted on said insulating substrate through the first adhesion layer; and

a second semiconductor chip produced by forming a second adhesion layer on a back surface of a wafer having a circuit formed on its front surface and by dicing the wafer, said second semiconductor chip being mounted on a circuit-formed surface of said first semiconductor chip through the second adhesion layer;

said first and second semiconductor chips being connected to the electrode section of the wiring layer with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

24. A semiconductor device comprising:

an insulating substrate including a wiring layer on its front surface and a packaging-use external terminal on its back surface, the wiring layer having an electrode section, the packaging-use external terminal being electrically connected to said wiring layer through a via hole;

a first semiconductor chip having a desired circuit formed on its front surface, said first semiconductor chip being mounted through an insulating paste; and

a second semiconductor chip produced by forming **[**a**]** *an* **[**second insulating**]** adhesion layer on a back surface of a wafer having a desired circuit formed on its front surface and by dicing the wafer, said second semiconductor chip being mounted on a circuit-formed surface

of said first semiconductor chip through the [second insulating] adhesion layer;

said first and second semiconductor chips being connected to the electrode section of the wiring layer with a wire,

said first and second semiconductor chips and the wire being sealed with a resin.

25. The semiconductor device as set forth in claim **23**,

wherein, when an outer edge of said second semiconductor chip protrudes from an outer edge of said first semiconductor chip, a support member having a same thickness as said first semiconductor chip is provided under a protruding part of said second semiconductor chip.

26. The semiconductor device as set forth in claim **24**,

wherein, when an outer edge of said second semiconductor chip protrudes from an outer edge of said first semiconductor chip, a support member having a same thickness as said first semiconductor chip is provided under said second semiconductor chip.

27. A semiconductor device comprising:

a first semiconductor chip;

an insulating substrate including on its front surface a wiring layer having an electrode section; an insulating layer disposed in an area where said first semiconductor chip is to be mounted, except for a part to be connected to said first semiconductor chip; and a metal bump for making electrical connection to said first semiconductor chip, said insulating substrate including on its back surface a packaging-use external terminal electrically connected to said wiring layer through a via hole, said first semiconductor chip being mounted on the front surface of said insulating substrate by face-down bonding through said metal bump; and

a second semiconductor chip produced by forming a first adhesion layer on a back surface of a wafer having a desired circuit formed on its front surface and by dicing the wafer, said second semiconductor chip being mounted on a surface of said first semiconductor chip on which surface a circuit is not formed, through the first adhesion layer;

said second semiconductor chip being connected to the electrode section of the wiring layer with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

28. The semiconductor device as set forth in claim **27**,

wherein the insulating layer includes a light blocking layer.

29. The semiconductor device as set forth in claim **27**,

wherein, when an outer edge of said second semiconductor chip protrudes from an outer edge of said first semiconductor chip, a support member having a same thickness as said first semiconductor chip is provided under a protruding part of said second semiconductor chip.

30. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;

(b) producing separate first semiconductor chips from said first wafer by dicing;

(c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer;

(d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;

(e) producing separate second semiconductor chips from said second wafer by dicing;

(f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip;

(g) wire-bonding said first semiconductor chip to an electrode section of said wiring layer with a wire;

(h) wire-bonding said second semiconductor chip to an electrode section of said wiring layer with a wire; and

(i) sealing said first and second semiconductor chips and the wires.

31. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming an insulating layer and a metal bump on a wiring layer;

(b) mounting a first semiconductor chip on said wiring layer with its circuit-formed surface facing said wiring layer;

(c) forming an insulating adhesion layer on a back surface of a wafer having a circuit formed on its front surface;

(d) producing separate second semiconductor chips from the wafer by dicing;

(e) mounting said second semiconductor chip on said first semiconductor chip with it back surface facing said first semiconductor chip;

(f) wire-bonding said second semiconductor chip to said wiring layer with a wire; and

(g) sealing said first and second semiconductor chips and the wire.

32. The method of manufacturing the semiconductor device as set forth in claim **30**, further comprising the steps of:

(j) forming a metal ball on each end of the wire for connecting said second semiconductor chip to the electrode section of the wiring layer;

(k) connecting one of the metal balls to said second semiconductor chip;

(l) cutting said wire; and

(m) making a surface of the metal ball connected to said second semiconductor chip flat;

said steps (j) to (m) being included between said steps (g) and (h).

33. The method of manufacturing the semiconductor device as set forth in claim **31**, further comprising the steps of:

(h) forming a metal ball on each end of the wire;

(i) connecting one of the metal balls to said second semiconductor chip;

(j) cutting the wire; and

(k) making a surface of the metal ball connected to said second semiconductor chip flat;

said steps (h) to (k) being included between said steps (e) and (f).

* * * * *

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Fukui et al.

(10) **Patent No.: US 6,352,879 B1**
(45) **Date of Patent: Mar. 5, 2002**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

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(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/604,081**

(22) Filed: **Jun. 27, 2000**

Related U.S. Application Data

(62) Division of application No. 09/223,272, filed on Dec. 30, 1998, now Pat. No. 6,100,594.

(30) **Foreign Application Priority Data**

Jan. 14, 1998 (JP) 10-5221

(51) **Int. Cl.**[7] **H01L 21/44**; H01L 21/48; H01L 21/50

(52) **U.S. Cl.** **438/106**; 438/107; 438/109; 438/118; 438/127

(58) **Field of Search** 438/110, 107–109, 438/114, 118, 124, 458, 106; 257/777, 738, 778

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(74) *Attorney, Agent, or Firm*—Nixon & Vanderhye P.C.

(57) **ABSTRACT**

A first semiconductor chip is produced by affixing a thermo-compression sheet to the back surface of a wafer having a circuit formed on its front surface. The first semiconductor chip is mounted on a circuit board including an insulating substrate and a wiring layer provided on the insulating substrate so that the back surface of the first semiconductor chip faces the circuit board. A second semiconductor chip produced in the same manner as the first semiconductor chip is mounted on the first semiconductor chip with its back surface facing the first semiconductor chip. Each of the first and second semiconductor chips is wire-bonded to the wiring layer with a wire. The first and second semiconductor chips and the wire are sealed with a sealing resin. The wiring layer is connected to external connection terminals through via holes provided in the insulating substrate.

15 Claims, 15 Drawing Sheets

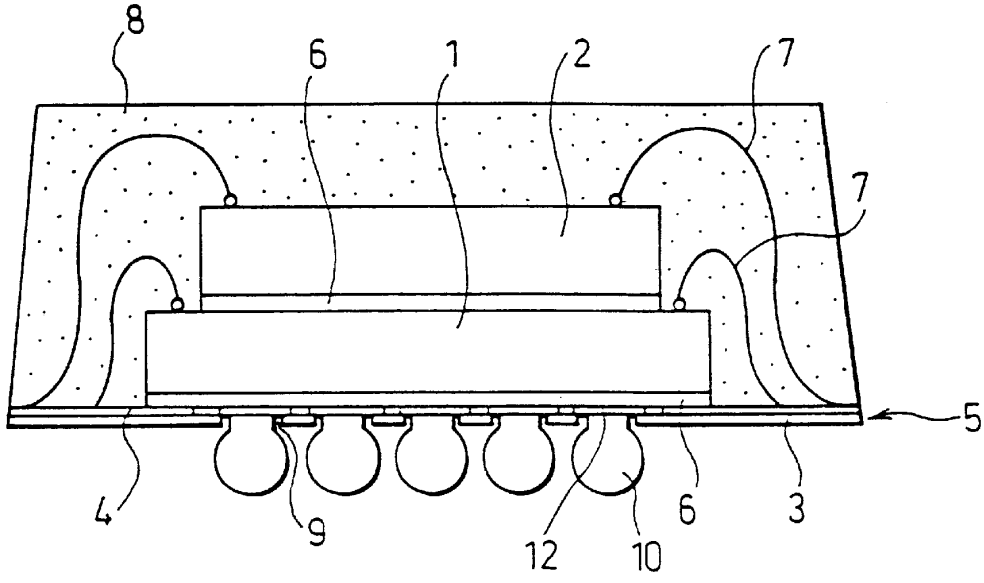


FIG.1

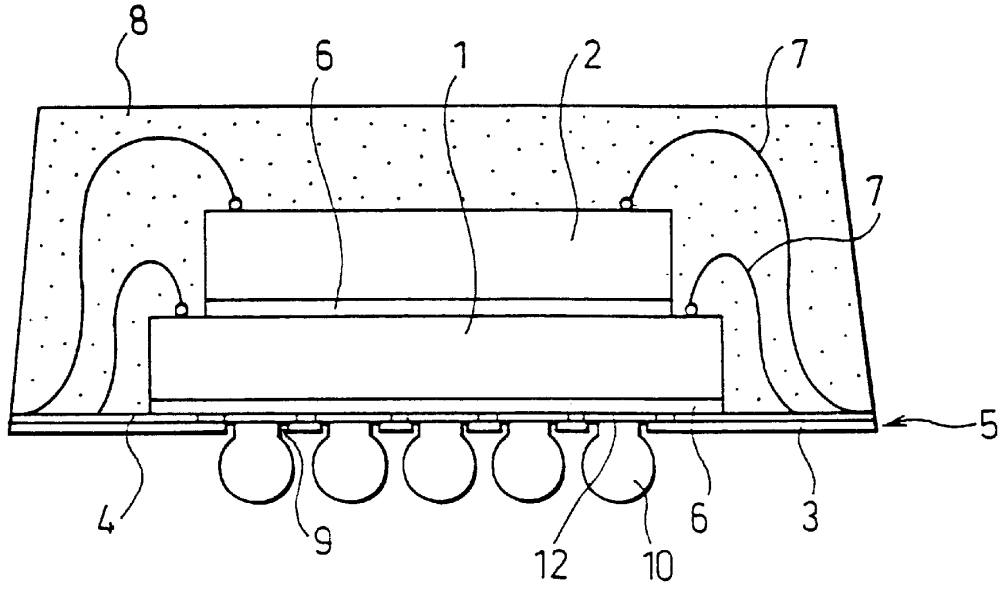


FIG. 2(a)

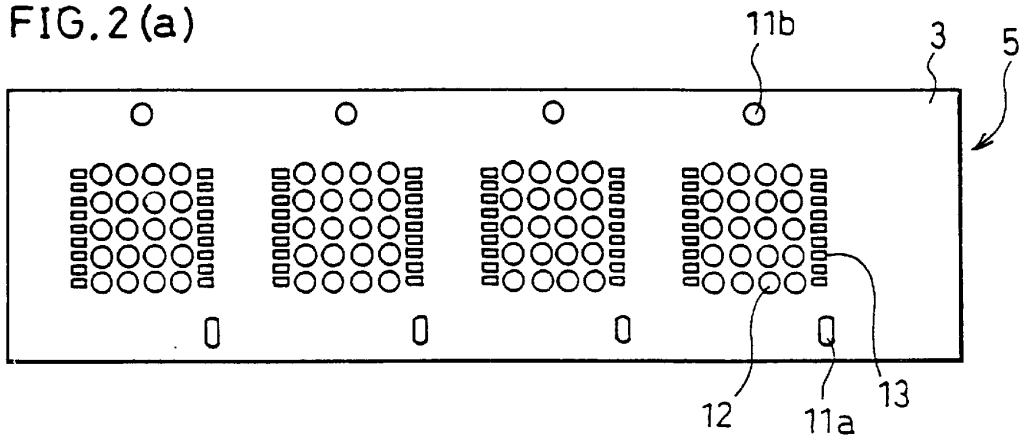


FIG. 2(b)

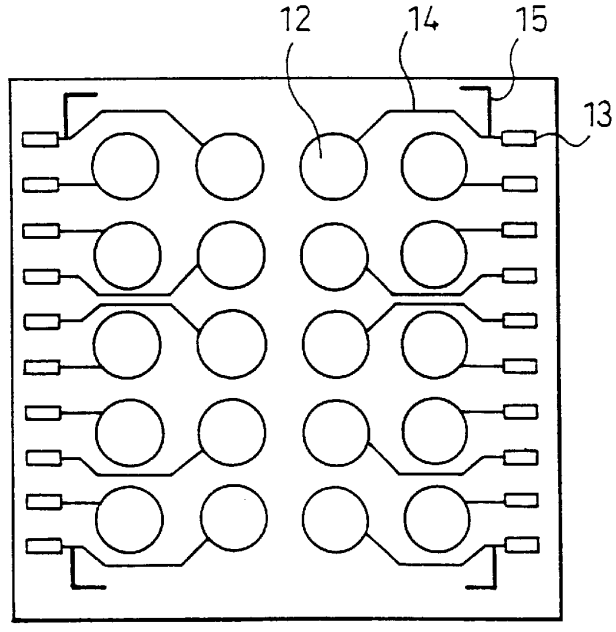


FIG.3(a)

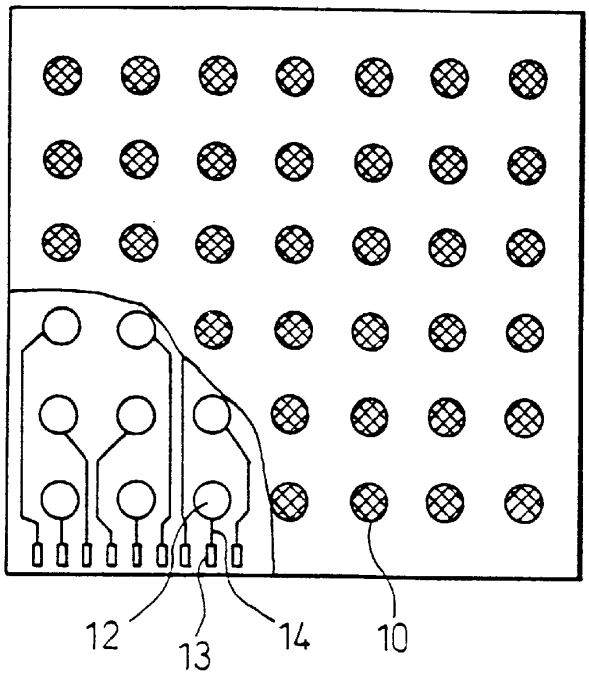


FIG.3(b)

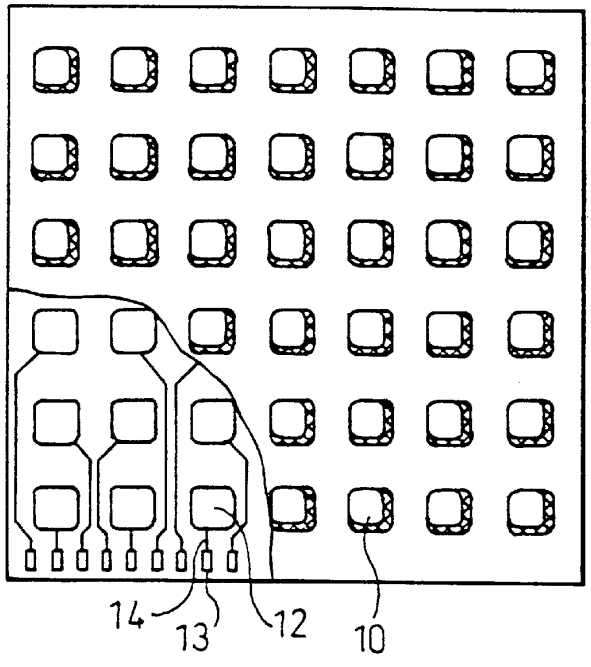


FIG. 4

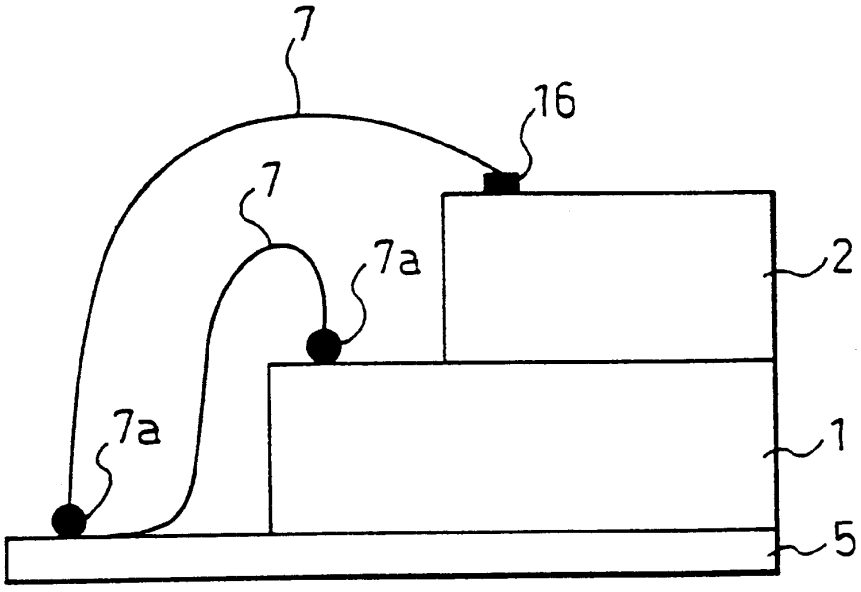


FIG.5(a)

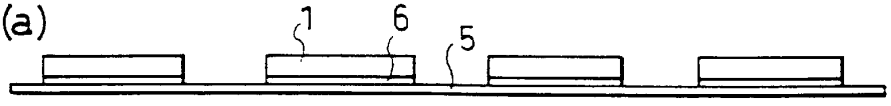


FIG.5(b)

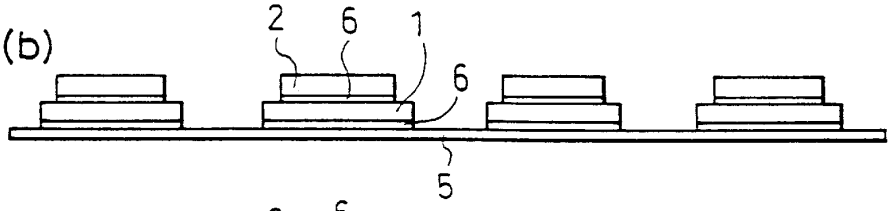


FIG.5(c)

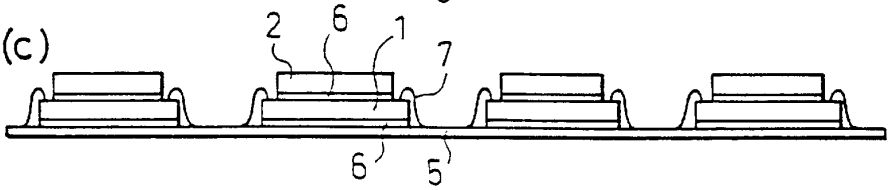


FIG.5(d)

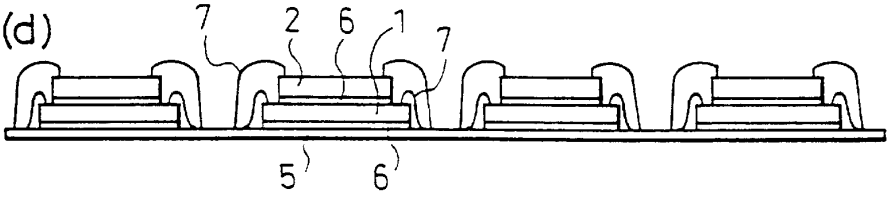


FIG.5(e)

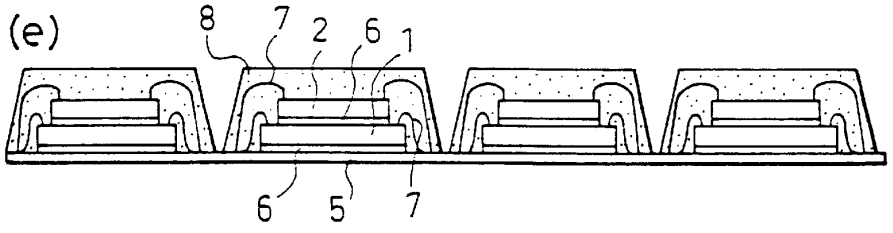


FIG.5(f)

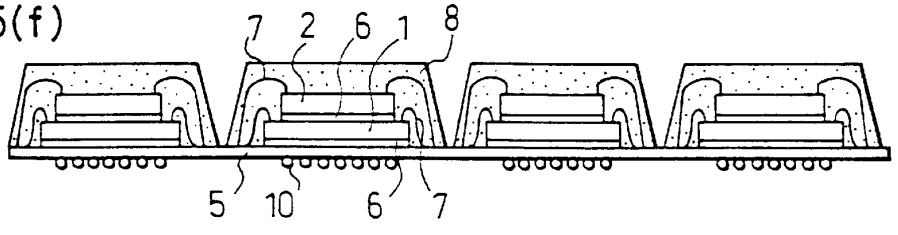


FIG.5(g)

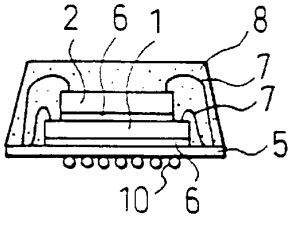


FIG.6 (a)

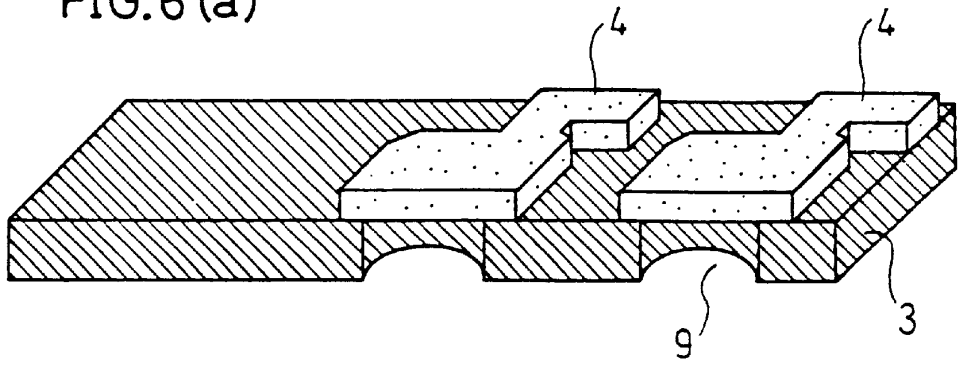


FIG.6 (b)

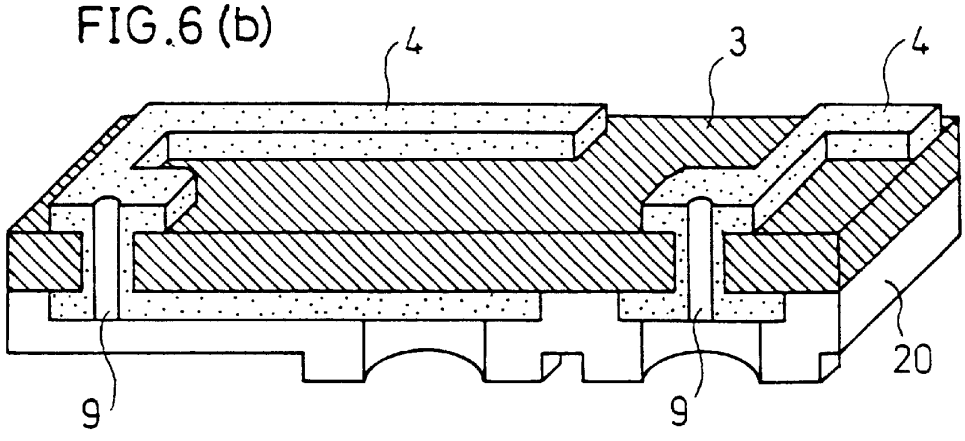


FIG.7(a)

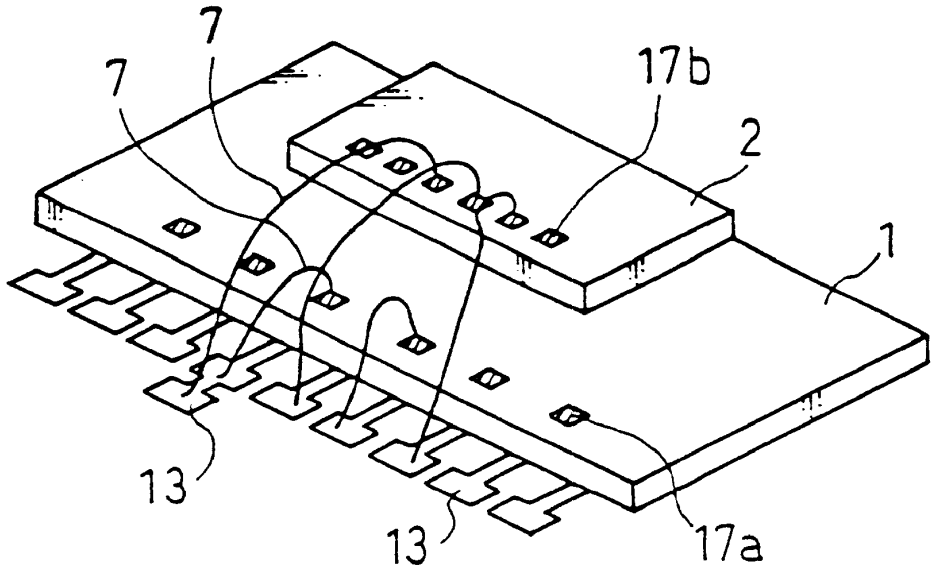


FIG.7(b)

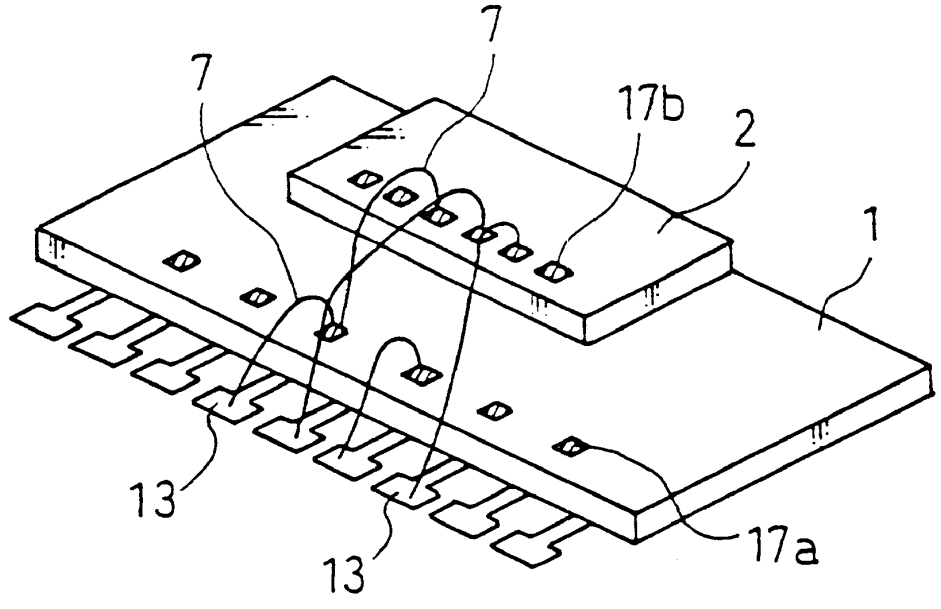


FIG.8(a)

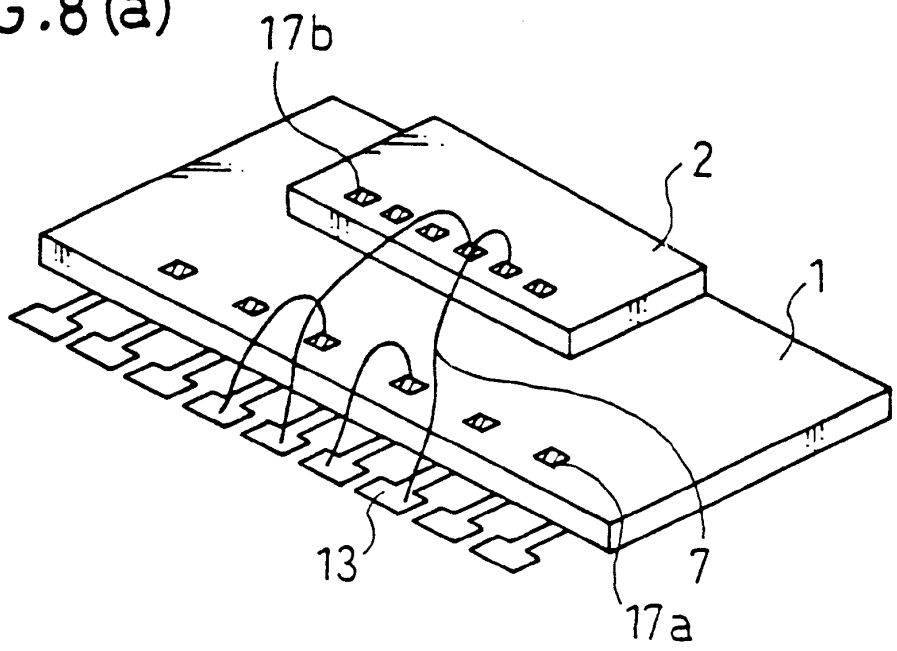


FIG.8(b)

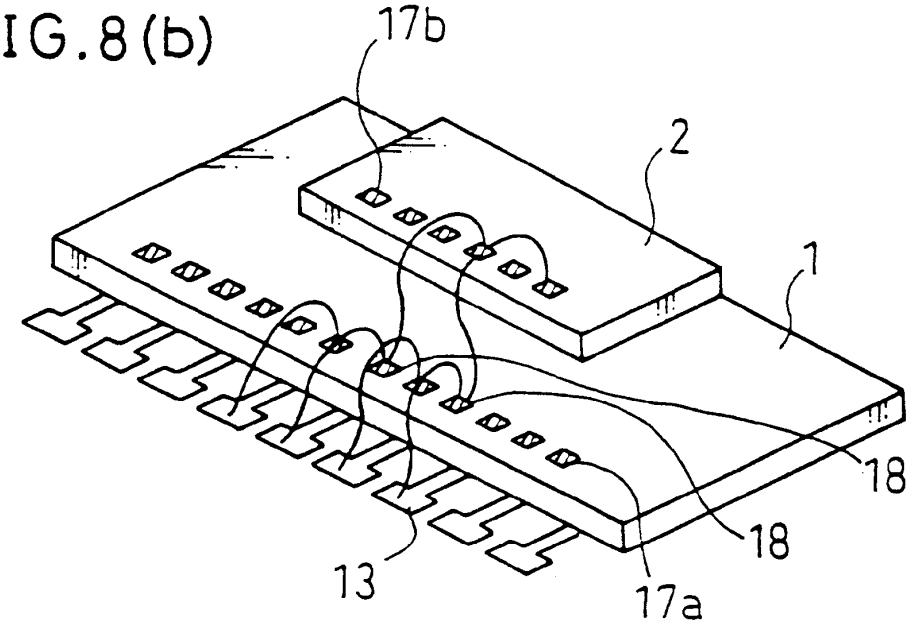


FIG. 9(a)

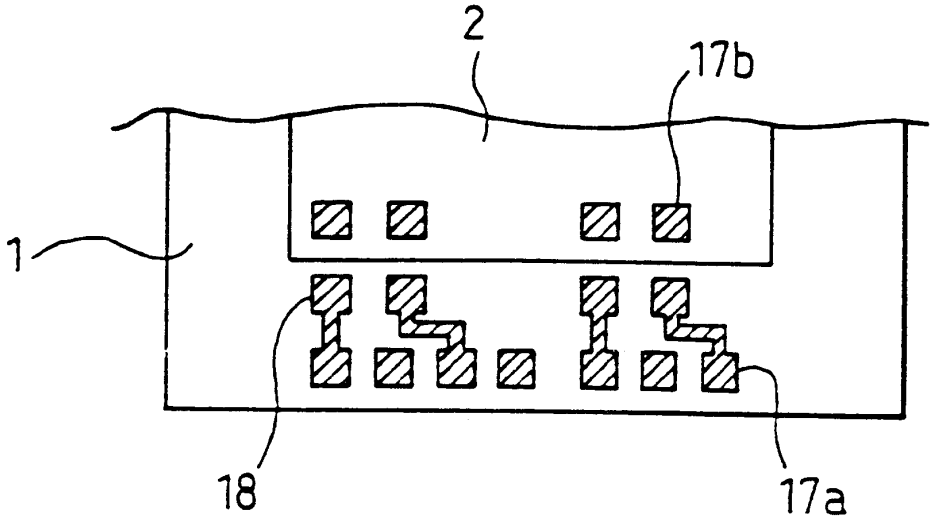


FIG. 9(b)

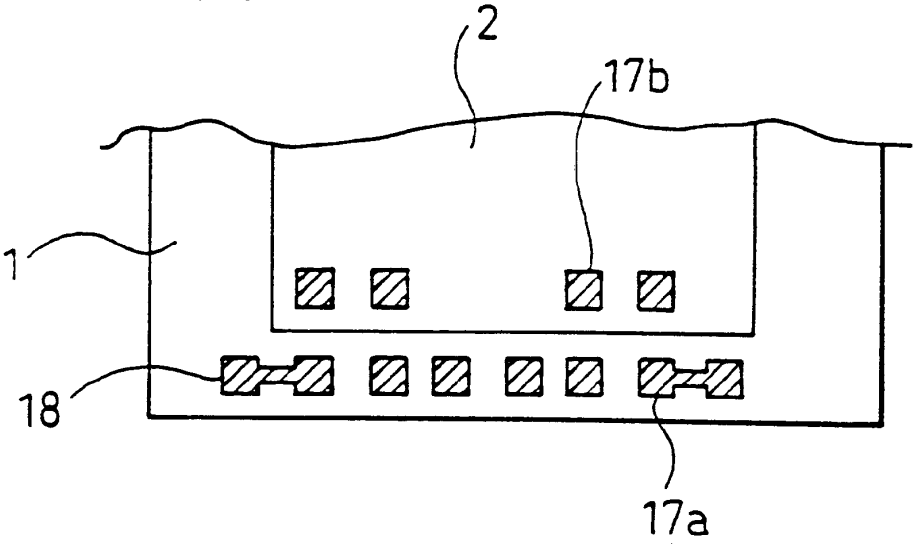


FIG.10

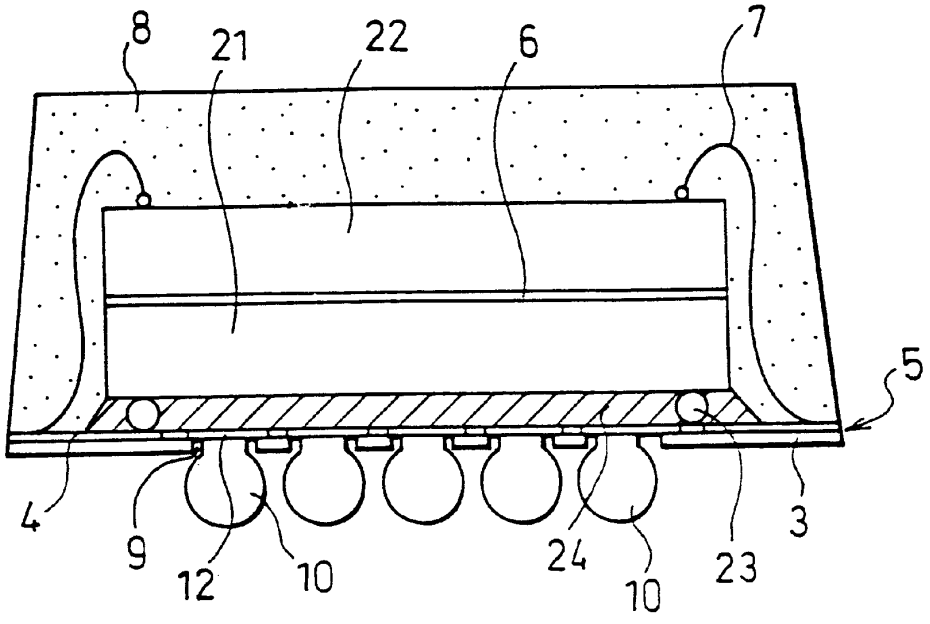


FIG.11(a)

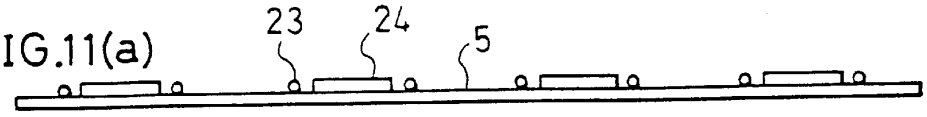


FIG.11(b)

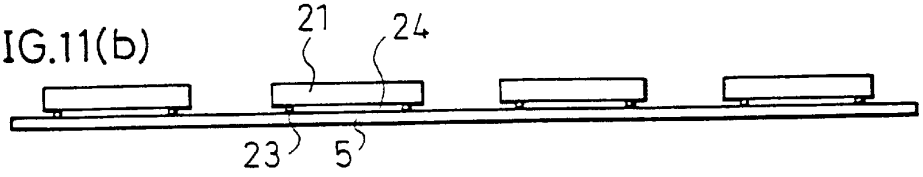


FIG.11(c)

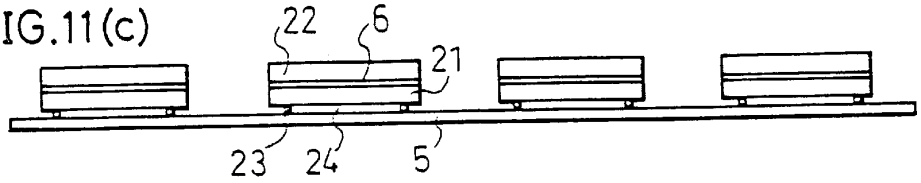


FIG.11(d)

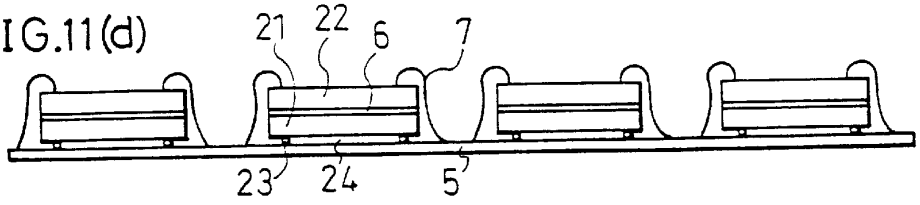


FIG.11(e)

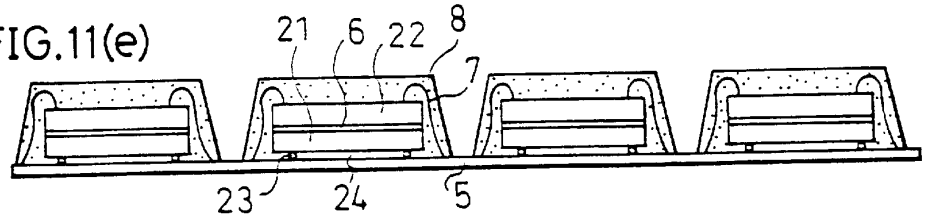


FIG.11(f)

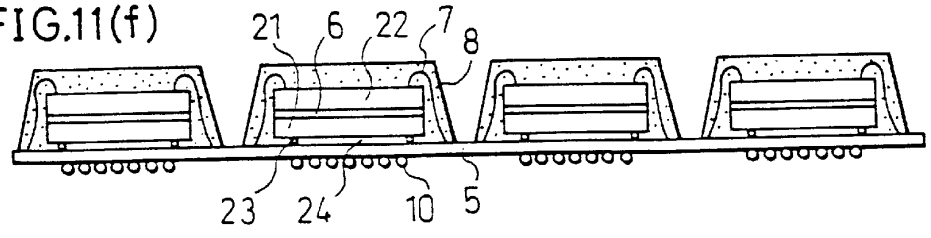


FIG.11(g)

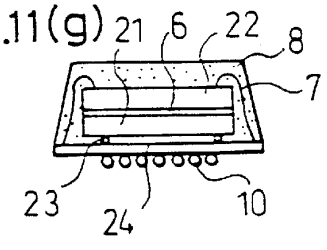


FIG.12(a)

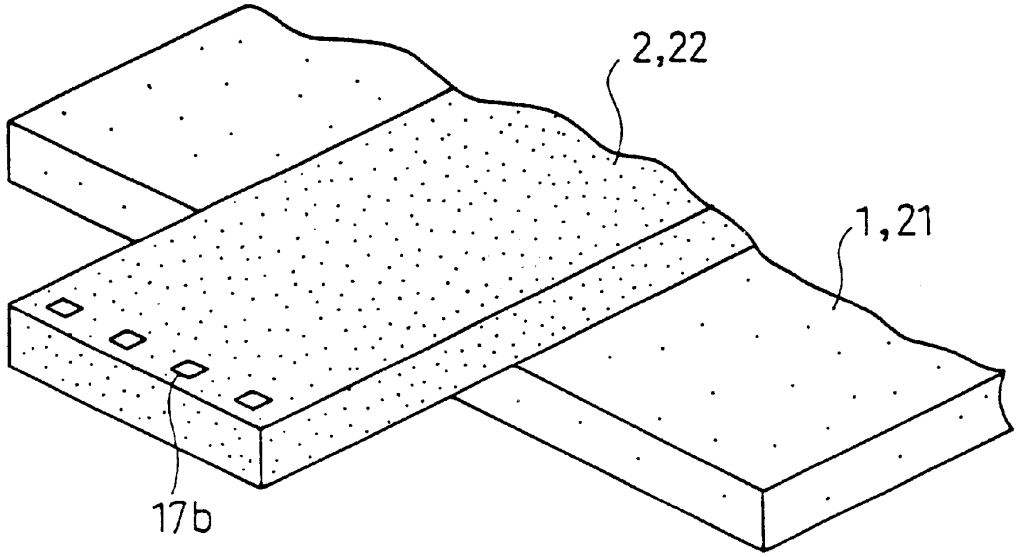


FIG.12(b)

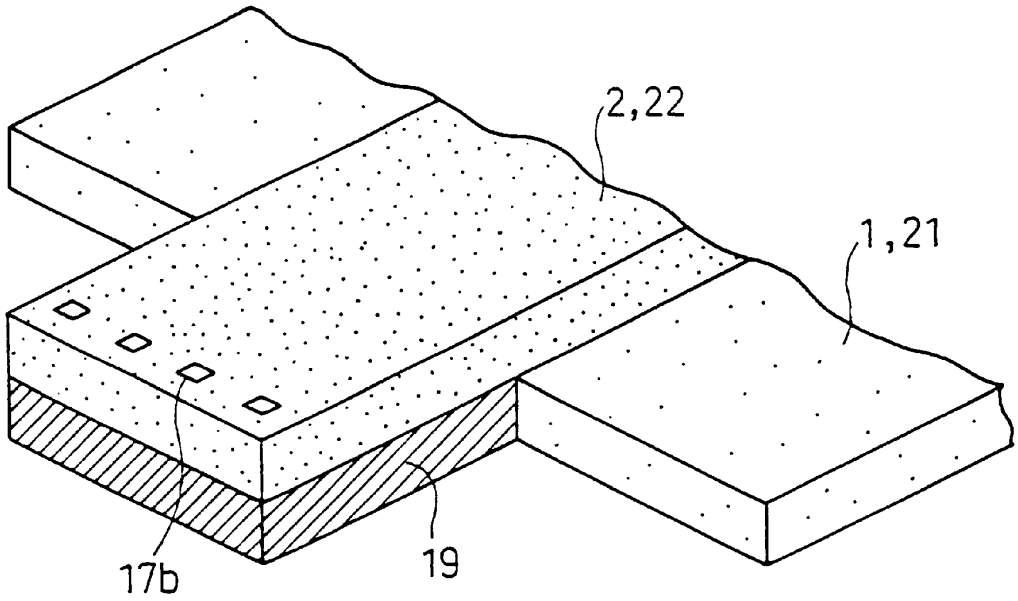


FIG.13(a)

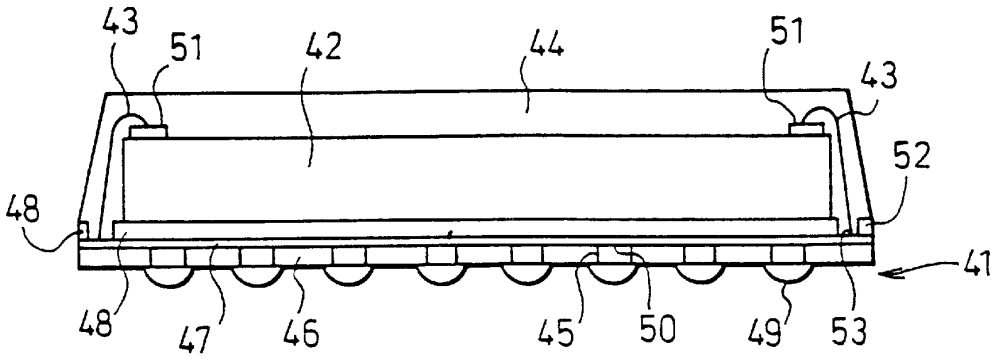


FIG.13(b)

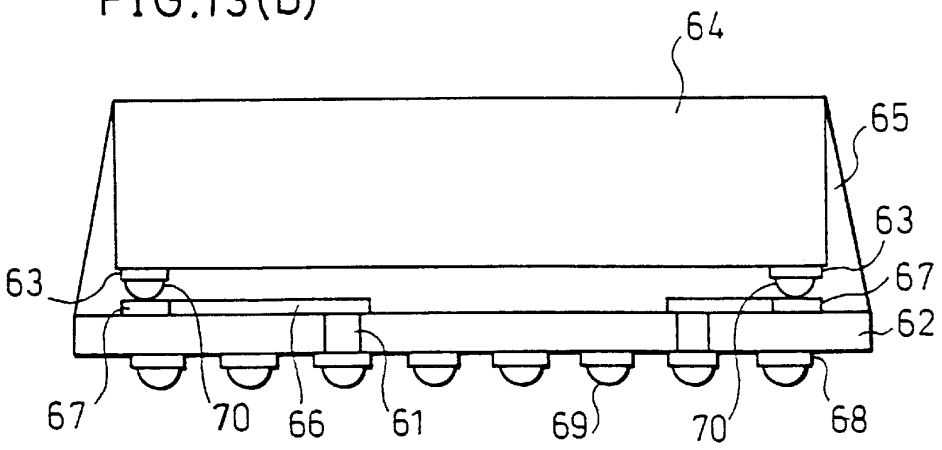


FIG.14(a)

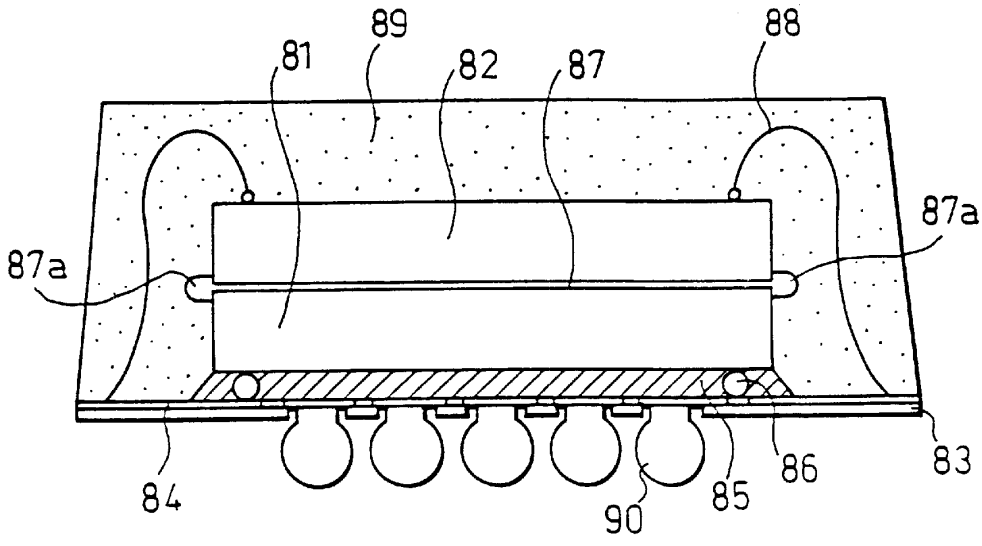


FIG.14(b)

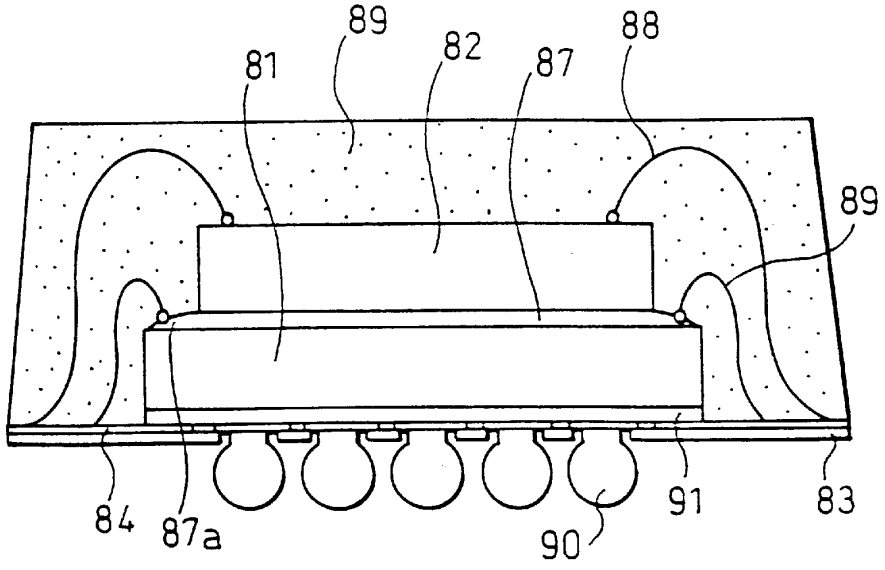
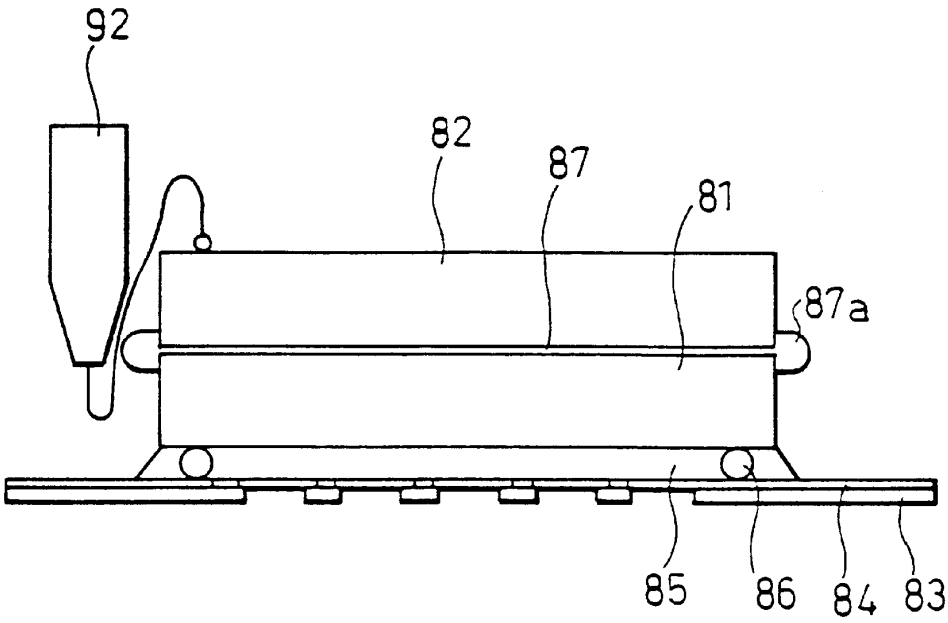


FIG.15



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a divisional of application Ser. No. 09/223,272, filed Dec. 30, 1998, the entire content of which is hereby incorporated by reference in this application now U.S. Pat. No. 6,100,594.

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacturing the same, and more particularly relates to a semiconductor device having a structure substantially miniaturized to a chip size, i.e., a CSP (Chip Size Package) structure, and a method of manufacturing such a semiconductor device.

BACKGROUND OF THE INVENTION

Miniaturization of a semiconductor device is in progress so as to achieve a high-density semiconductor device for use on a printed circuit board. Recently, a semiconductor device substantially miniaturized to a chip size has been developed. The structure of such a miniaturized semiconductor device is called a CSP structure. Japanese Publication of Unexamined Patent Application No. 121002/1997 (Tokukaihei 9-121002) discloses a semiconductor device having the CSP structure shown in FIG. **13**(*a*). This semiconductor device includes a semiconductor chip **42** disposed with its circuit formed surface facing up, and wires **43** for electrically connecting the semiconductor chip **42** to a wiring pattern **47**. The above publication discloses another semiconductor device having the CSP structure shown in FIG. **13**(*b*). This semiconductor device includes a semiconductor chip **64** disposed with its circuit formed surface facing down, and a bump electrode **70** for electrically connecting the semiconductor chip **64** to a wiring pattern **66**.

In FIG. **13**(*a*), **41** is a wiring component, **42** is a semiconductor chip, **43** is a wire, **44** is a resin sealing member, **45** is a throughhole, **46** is a substrate, **47** is a wiring pattern, **48** is an insulating material, **49** is an external connection-use terminal, **50** is an external connection area, **51** is an electrode, **52** is a window opening section, and **53** is an inner connection area. In FIG. **13**(*b*), **61** is a throughhole, **62** is a wiring component, **63** is an electrode, **64** is a semiconductor chip, **65** is a resin sealing member, **66** is a wiring pattern, **67** is an inner connection area, **68** is an external connection area, **69** is an external connection-use terminal, and **70** is a bump electrode.

In some devices such as portable devices, a plurality of semiconductor chips are mounted in a package so as to increase the added value and capacity of memory, etc. For example, a multi-chip module is provided with a plurality of semiconductor chips arranged parallel to each other in a package. However, such an arrangement makes it impossible to produce a package smaller than the total area of the semiconductor chips to be mounted. In order to solve the problem, a stacked package including a plurality of semiconductor chips laminated in a package to achieve a high packaging density is disclosed in Japanese Publication of Unexamined Patent Application No. 90486/1993 (Tokukaihei 5-90486).

Specifically, the semiconductor devices disclosed in the above publication are each packaged in ceramic packages and arranged in the following manner. In one of the semiconductor devices, a pair of semiconductor chips are adhered to each other with their back surfaces where a circuit is not formed facing each other, and are mounted on another pair of semiconductor chips via metal bumps. In the other semiconductor device, a pair of semiconductor chips are adhered to each other with the circuit formed surface of one semiconductor chip facing the back surface of the other semiconductor chip.

The above-mentioned stacked package is a small, high-density semiconductor device. However, a semiconductor device smaller than such a stacked package has been required. For that reason, a semiconductor device having a CSP structure as well as a stacked package structure is required to be produced.

In a semiconductor device having a CSP structure where the semiconductor chips are laminated, an adhesive agent (paste) potting method and a method using a thermo-compression sheet are utilized for bonding the semiconductor chip to the substrate, and for bonding the laminated semiconductor chips to each other.

In the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent spreads beyond the outer edge of the semiconductor chip. For example, as shown in FIG. **14**(*a*), when bonding semiconductor chips **81** and **82** to each other with their back surfaces facing each other, an adhesive agent **87** between the semiconductor chips **81** and **82** overflows. In addition, as shown in FIG. **15**, in the step of wire-bonding the semiconductor chip **82** disposed on the top to an electrode section of a wiring layer **84** (before a sealing resin **89** and packaging-use external terminals **90** are formed), wiring on an insulating substrate **83** must be provided far from the side surfaces of the semiconductor chips **81** and **82** so as to keep the overflown adhesive agent **87***a* from coming into contact with a jig **92** of a wire bonder. Such an arrangement causes the package size to be increased in the end. Furthermore, as shown in FIG. **14**(*b*), when bonding the back surface of the semiconductor chip **82** to the circuit formed surface of the semiconductor chip **81**, the overflown adhesive agent **87***a* may stick to an electrode pad provided on the semiconductor chip **81**.

On the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips **81** and **82**. This gap cannot be filled with the sealing resin **89**, thereby causing problems such as separation of the semiconductor chip **82** from the semiconductor chip **81**.

The method using a thermo-compression sheet requires the steps of placing members at the right locations. Specifically, a thermo-compression sheet having the same size as the semiconductor chip **82** must be placed accurately at a specific location an the semiconductor chip **81**. In addition, the semiconductor chip **82** must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet.

In FIGS. **14**(*a*) and **14**(*b*), **85** is an insulating sheet, **86** is a metal bump, and **91** is an adhesive sheet.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a further-miniaturized semiconductor device having a stacked package structure as well as a CSP structure.

In order to achieve the above object, a semiconductor device in accordance with the present invention has a stacked package structure and a chip size package structure and is characterized in including:

- an insulating substrate including a wiring layer having electrode sections;
- a first semiconductor chip having a first insulating adhesion layer adhered to its back surface where a circuit is

not formed, the first semiconductor chip being mounted on the wiring layer through the first insulating adhesion layer; and

a second semiconductor chip having a second insulating adhesion layer adhered to its back surface where a circuit is not formed, the second semiconductor chip being mounted on a circuit-formed front surface of the first semiconductor chip through the second insulating adhesion layer;

each of the first and second semiconductor chips being wire-bonded to the electrode section with a wire, the first and second semiconductor chips and the wire being sealed with a resin.

In the above structure, the first semiconductor chip and the second semiconductor chip are each wire-bonded to the electrode section provided on the wiring layer with the wires, and the second insulating adhesion layer is used for affixing the second semiconductor chip to the first semiconductor chip. This structure eliminates the need for wire-bonding the first and second semiconductor chips to points on the wiring layer, far from the side surfaces of the first and second semiconductor chips, considering a situation in which the excessively applied adhesive agent overflows the space between the first and second semiconductor chips. Therefore, a miniaturized, high-density semiconductor device can be realized.

Furthermore, in the case of using a thermo-compression sheet, when mounting the first or second semiconductor chip at a desired location, accurate positioning is required twice, i.e., positioning the thermo-compression sheet, etc., and positioning the first or second semiconductor chip on the thermo-compression sheet. In contrast, the first and second insulating adhesion layers according to the present invention are in advance disposed on the back surfaces of the first and second semiconductor chips, respectively. Therefore, the first or second semiconductor chip can be mounted at a desired location by accurately positioning it once. It is thus possible to miniaturize the semiconductor device without complicating its manufacturing process.

A semiconductor device in accordance with the present invention can be arranged to include:

an insulating substrate including a wiring layer having electrode sections;

a first semiconductor chip having a circuit formed on its front surface and an insulating adhesion layer adhered to its back surface;

a metal bump , disposed between the first semiconductor chip and the wiring layer, for bump-bonding the front surface of the first semiconductor chip to the wiring layer so that the front surface faces the wiring layer; and

a second semiconductor chip whose back surface where a circuit is not formed is mounted on the back surface of the first semiconductor chip through the insulating adhesion layer;

the second semiconductor chip being wire-bonded to the electrode section of the wiring layer with a wire, the first and second semiconductor chips and the wire being sealed with a resin.

In the above arrangement, the first semiconductor chip is connected to the wiring layer through the metal bump, the second semiconductor chip is wire-bonded to the electrode sections on the wiring layer with wires, and the back surfaces of the first and second semiconductor chips are adhered to each other by the insulating layer. This arrangement eliminates the need for wire-bonding the second semiconductor chip to points on the wiring layer, far from the side surfaces of the first and second semiconductor chips, considering a situation in which the excessively applied adhesive agent overflows the space between the first and second semiconductor chips. Therefore, a miniaturized, high-density semiconductor device can be realized.

In the case of using the thermo-compression sheet, when mounting the second semiconductor chip on the first semiconductor chip, accurate positioning is required twice in a conventional manufacturing method, i.e., positioning the thermo-compression sheet on the first semiconductor chip, and positioning the second semiconductor chip on the thermo-compression sheet. However, the insulating adhesion layer according to the present invention are disposed on the back surface of the second semiconductor chip in advance. Therefore, the second semiconductor chip can be mounted at a desired location on the first semiconductor chip by accurately positioning it once. It is thus possible to miniaturize the semiconductor chip without complicating its manufacturing process.

A method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:

(a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;

(b) producing separate first semiconductor chips from the first wafer by dicing;

(c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;

(d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;

(e) producing separate second semiconductor chips from the second wafer by dicing;

(f) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;

(g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;

(h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and

(i) sealing the first and semiconductor chips and the wires.

With the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface in advance when being in the wafer state, the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip. It is thus possible to simplify the process of manufacturing the semiconductor chip.

Morever, in the above manufacturing method, the adhesive agent does not overflow the space between the first and second semiconductor chips, the first and second semiconductor chips can be wire-bonded to the wiring layer at a location closer to the edges of the first and second semiconductor chips. It is thus possible to realize a miniaturized, high-density semiconductor device.

A method of manufacturing a semiconductor device in accordance with the present invention including the steps of:

(a) forming an insulating layer and a metal bump on a wiring layer;

(b) mounting a first semiconductor chip on the wiring layer with its circuit-formed surface facing the wiring layer;

(c) forming an insulating adhesion layer on a back surface of a wafer having a circuit formed on its front surface;

(d) producing separate second semiconductor chips from the wafer by dicing;

(e) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;

(f) wire-bonding the second semiconductor chip to the wiring layer with a wire; and

(g) sealing the first and second semiconductor chips and the wire.

In this manufacturing method, like the above-mentioned method of the present invention, since the second semiconductor chip has the insulating adhesion layer adhered to its back surface in advance when being in the wafer state, the second semiconductor chip can be mounted at a desired location without the step of accurately positioning the insulating adhesion layer on the second semiconductor chip. It is thus possible to simplify the process of manufacturing the semiconductor chip.

Furthermore, in the above manufacturing method, the adhesive agent does not overflow the space between the first and second semiconductor chips, the second semiconductor chip can be wire-bonded to the wiring layer at a location closer to the edges of the first and second semiconductor chips. It is thus possible to realize a miniaturized, high-density semiconductor device.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a semiconductor device in accordance with the first embodiment of the present invention.

FIG. **2**(*a*) is a plan view of a circuit board before being cut, and

FIG. **2**(*b*) is a partially enlarged view of the circuit board shown in FIG. **2**(*a*).

FIG. **3**(*a*) is an explanatory view showing an arrangement of ball-like external connection-use terminals, and

FIG. **3**(*b*) is an explanatory view showing an arrangement of trapezoidal external connection-use terminals.

FIG. **4** is an explanatory view showing how laminated semiconductor chips are each wire-bonded to the circuit board.

FIGS. **5**(*a*) to **5**(*g*) show one example of a process for manufacturing the semiconductor device.

FIG. **6**(*a*) is a partially enlarged view of the circuit board including a wiring layer disposed on one surface of an insulating substrate, and FIG. **6**(*b*) is a partially enlarged view of a circuit board including a wiring layer disposed on each surface of the insulating substrate.

FIG. **7**(*a*) is an explanatory view showing a wiring state when two laminated semiconductor chips are connected to the same electrode section, and

FIG. **7**(*b*) is an explanatory view showing another state that the two laminated semiconductor chips are connected to the same electrode section.

FIG. **8**(*a*) is an explanatory view showing a wiring state that the two laminated semiconductor chips are connected to different electrode sections, and

FIG. **8**(*b*) is an explanatory view showing another wiring state that the two laminated semiconductor chips are connected to different electrode sections.

FIG. **9**(*a*) is an explanatory view showing one example of an arrangement of dummy pads formed on a first semiconductor chip, and

FIG. **9**(*b*) is an explanatory view showing another example of the arrangement of the dummy pads disposed on the first semiconductor chip.

FIG. **10** is a cross-sectional view of a semiconductor device in accordance with the second embodiment of the present invention.

FIGS. **11**(*a*) to **11**(*g*) show one example of a process for manufacturing the semiconductor device.

FIG. **12**(*a*) is a perspective view showing that a second semiconductor chip in the semiconductor device in accordance with the first embodiment or the second embodiment protrudes from a first semiconductor chip, and

FIG. **12**(*b*) is a perspective view showing that the second semiconductor chip is reinforced.

FIG. **13**(*a*) is a cross-sectional view showing a semiconductor device having a CSP structure manufactured by a conventional wire bonding method, and

FIG. **13**(*b*) is a cross-sectional view showing a semiconductor device having a CSP structure manufactured by a conventional face-down bonding method.

FIG. **14**(*a*) and FIG. **14**(*b*) are cross-sectional views of conventional semiconductor devices having a stacked package structure.

FIG. **15** is a cross-sectional view of the semiconductor device shown in FIG. **14**(*a*) during manufacturing.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

The following descriptions will explain one embodiment of the present invention with reference to FIGS. **1** to **9**.

As shown in FIG. **1**, in a semiconductor device according to this embodiment, a first semiconductor chip **1** and a second semiconductor chip **2** are laminated in this order on a circuit board **5** including an insulating substrate **3** and a wiring layer **4** mounted on the insulating substrate **3**. Regarding the first semiconductor chip **1** and the second semiconductor chip **2**, the surface (front surface) on which an element is formed is hereinafter referred to as a "circuit formed surface", and the surface opposite thereto is referred to as a "back surface".

The semiconductor chip **1** is disposed with its back surface facing the insulating substrate **3**. The second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1** through a thermo-compression sheet (adhesion layer) **6** so that its back surface is adhered to the thermo-compression sheet **6**.

The semiconductor device in accordance with the present embodiment is arranged so that the second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1**. With this arrangement, the second semiconductor chip **2** on the top of the first semiconductor chip **1** does not influence (interfere with) electrode pads of the first semiconductor chip **1**. The circuit formed surface of the first semiconductor chip **1** is in advance coated with an insulating-resin, etc. Namely, the coating is applied to the circuit formed surface of the first semiconductor chip **1** by a spin coating method, etc. when the first semiconductor chip **1** is in a wafer state before subjected to dicing. In this case, the coating material on the electrode pads (not shown) disposed on the circuit formed surface of the first semiconductor chip **1** is removed.

The first semiconductor chip **1** and the second semiconductor chip **2** are each connected (wire-bonded) to electrode sections of the wiring layer **4** on the insulating substrate **3** with wires **7**.

The first semiconductor chip **1**, the second semiconductor chip **2** and the wires **7**, arranged as above, are covered by a sealing resin **8**.

The insulating substrate **3** includes via holes **9** at the locations corresponding to below-described land sections **12** constituting the wiring layer **4**. Ball-like packaging-use external terminals **10** are connected in an area-array-like arrangement to the land sections **12** through the via holes **9** from the side of the insulating substrate **3**, on which side the first semiconductor chip **1** and the second semiconductor chip **2** are not formed.

Next, the following descriptions will explain in further detail the above-mentioned members constituting the semiconductor device in accordance with the present embodiment.

FIG. **2**(*a*) is a plan view of the circuit board **5** before being cut in the process of manufacturing the semiconductor device. As shown in FIG. **2**(*a*) four guide holes **11** are formed in both side sections of the insulating substrate **3** (the upper part and the lower part of the insulating substrate **3** in FIG. **2**(*a*)) of the circuit board **5** before being cut. The guide holes **11***a* formed in one of the side section and the guide holes **11***b* formed in the other side section have different shapes. These guide holes **11** are used for transporting the semiconductor device during its manufacturing process.

The material of the insulating substrate **3** is not particularly limited, and a resin substrate or a film having excellent heat resistance is acceptable. The insulating material **3** may be a resin substrate, etc. made of, for example, polyimide, epoxy resin containing glass fiber, bismaleid triazine (BT) resin, polyester, polyamide, fluororesin, ceramic, and polyester containing glass fiber. Polyimide is the most preferable of the above materials.

FIG. **2**(*b*) is a partially enlarged view of the circuit board **5** shown in FIG. **2**(*a*), showing the structure of the wiring layer **4**. As shown in FIG. **2**(*b*), the wiring layer **4** includes the land sections **12**, electrode sections **13**, and wiring sections **14**, disposed on the insulating substrate **3**. Each of the. wiring sections **14** connects the land section **12** to the electrode section **13**.

The electrode sections **13** are formed on both ends of the wiring layer **4** (the left part and the right part of the wiring layer **4** in FIG. **2**(*b*)). As explained in detail later, each of the electrode section **13** is connected to the first semiconductor chip **1** or the second semiconductor chip **2** by the wire **7**. Therefore, the electrode sections **13** are located outside the area of the wiring layer **4**, where the first semiconductor chip **1** and the second semiconductor chip **2** are mounted.

The land section **12** is a packaging-use external terminal forming section for connecting the packaging-use external terminal **10** and the wiring layer **4** through the via hole **9** of the insulating substrate **3**.

The first semiconductor chip **1** can be completely insulated from the wiring layer **4** by, for example, providing a sheet of an insulating resin on an area of the wiring layer **4** where the first semiconductor chip **1** is to be mounted or applying an insulating resin coating to the area of the wiring layer **4**. The wiring layer **4** is made of copper (Cu), aluminum (Al), gold (Au), nickel (Ni), and other materials. Cu is particularly preferable because it is less costly. Methods of forming the wiring layer **4** on the insulating substrate **3** include a vapor deposition method and a plating method. In order to pattern the wiring layer **4** to form a desired pattern, a conventional photolithography method can be utilized.

FIG. **3**(*a*) is a view seen from the back side of the semiconductor device shown in FIG. **1**, i.e., the side where the packaging-use external terminals **10** are disposed. As shown in FIG. **3**(*a*), ball-like packaging-use external terminals **10** are disposed in an area-array-like arrangement, and connected to the land sections **12** provided on the wiring layer **4**. The packaging-use external terminals **10** are not limited to a ball-like shape, and may have a trapezoidal shape as shown in FIG. **3**(*b*).

Each of the wires **7** is used for connecting the electrode pad disposed on the first semiconductor chip **1** or the second semiconductor chip **2** to the electrode section **13** of the wiring layer **4**. In a conventional semiconductor device, a gold ball provided on only one end of the wire is in contact with the electrode pad of the first semiconductor chip or the second semiconductor chip, and the other end of the wire is connected to the electrode section of the wiring layer on the insulating substrate. Here, the gold ball can be provided on only one end of the wire. The gold ball is brought into contact with the electrode pad by imposing a load lighter than the load applied in connecting, by thermo-compression bonding, the wire to the electrode section of the wiring layer on the insulating substrate. This is because connecting the wires to the semiconductor chips by thermo-compression bonding, i.e., by application of a heavy load, increases the possibility of damaging the semiconductor chips.

However, the above conventional arrangement has the following problem. Namely, the wires, especially those connected to the second semiconductor chip, are connected to the electrode sections of the wiring layer provided on the circuit board at a small angle with respect to the circuit board. Therefore, the wire is connected to the circuit board, far from the end of the first semiconductor chip.

In order to solve the problem, in the semiconductor device according to the present embodiment, the first semiconductor chip **1** and the second semiconductor chip **2** are each wire-bonded to the circuit board **5** as shown in FIG. **4**. The first semiconductor chip **1** and the circuit board **5** are wire-bonded in the same manner as the conventional semiconductor device. Then, the wire **7** is connected to the circuit board **5** with a gold ball **7***a* provided on one end of the wire **7**. Thereafter, the other end of the wire **7** is connected, by thermo-compression bonding, to a gold bump **16** formed on the electrode pad of the second semiconductor chip **2** in advance so as to connect the second semiconductor chip **2** to the circuit board **5**.

Since wire-bonding between the second semiconductor chip **2** and the circuit board **5** is performed as above, the wire **7** connected to the second semiconductor chip **2** is connected to the circuit board **5** at an angle closer to 90° with respect to the circuit board **5**. Therefore , the wire **7** is connected to the circuit board **5** at a closer location to the end of the first semiconductor chip **1**, thereby enabling further miniaturization of the semiconductor device in accordance with the present embodiment.

The wire **7** is connected to the gold bump **16** by thermo-compression bonding by a load nearly equal to the load applied when connecting the wire **7** to the electrode section of the wiring layer **4** on the insulating substrate **3** by thermo-compression bonding. However, by using the gold bump **16**, the stress applied to the second semiconductor chip **2** can be lowered. It is thus possible to reduce the possibility that the second semiconductor chip **2** is damaged by a heavy load applied there to.

The gold bump **16** is formed by connecting a gold ball, provided on the end of the wire by the conventional method, to the electrode pad on the second semiconductor chip **2**, and then cutting the wire **7**. Thereafter, by making the upper surface of the gold bump **16** flat with a stamping jig, the wire **7** can be surely affixed to the gold bump **16** by thermo-compression bonding.

Note that the first semiconductor chip **1** and the circuit board **5** can be wire-bonded to each other in the same manner as the above-mentioned wire-bonding of the second semiconductor chip **2** and the circuit board **5**.

The following descriptions will explain one example of the process (including steps (1) to (5)) for manufacturing the semiconductor device in accordance with the present embodiment with reference to FIGS. **5**(*a*) to **5**(*g*).

(1) First, the first semiconductor chip **1** is mounted on the circuit board **5** (see FIG. **5**(*a*)) When the first semiconductor chip **1** is in a wafer state, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips **1**. The first semiconductor chip **1** is mounted on the circuit board **5** at a location inside a mount location recognition-use mark **15** provided on the circuit board **5**. Here, instead of providing the thermo-compression sheet **6** in advance when the first semiconductor chip **1** is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board **5** before the first semiconductor chip **1** is mounted on the circuit board **5**.

(2) Next, the second semiconductor chip **2** is mounted on the circuit formed surface of the first semiconductor chip **1** (see FIG. **5**(*b*)). When the second semiconductor chip **2** is in the wafer state, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer, and then the wafer is cut to produce separate pieces of second semiconductor chips **2**. The second semiconductor chip **2** is accurately positioned at a specific location on the circuit formed surface of the first semiconductor chip **1**.

By affixing the thermo-compression sheet **6** to the back surface of the second semiconductor chip **2** in advance, accurate positioning is necessary only when mounting the second semiconductor chip **2** on the first semiconductor chip **1**. Therefore, since one step requiring accurate positioning is omitted in the process for manufacturing the semiconductor device in accordance with the present embodiment, this manufacturing process is simplified compared with the conventional process in which the thermo-compression sheet **6** is disposed on the circuit formed surface of the first semiconductor chip **1**, and then the second semiconductor chip **2** is adhered to the thermo-compression sheet **6**.

(3) Then, each of the electrode pads (not shown) disposed on the first semiconductor chip **1** and the second semiconductor chip **2** is connected, with the wire **7** made of Au, to the electrode section **13** formed in the wiring layer **4** on the circuit board **5**. More specifically, the first semiconductor chip **1** and the wiring layer **4** are first electrically connected to each other (see FIG. **5**(*c*)), and then the second semiconductor chip **2** and the wiring layer **4** are electrically connected to each other (see FIG. **5**(*d*)). Since the first semiconductor chip **1** and the second semiconductor chip **2** are each electrically connected to the wiring layer **4** in the above order, it is possible to avoid such a problem that the wire **7** for connecting the first semiconductor chip **1** to the circuit board **5** and the wire **7** for connecting the second semiconductor chip **2** to the circuit board **5** cross each other, and prevent connection of the firs t semiconductor chip **1** to the circuit board **5**.

(4) Thereafter, each of the packaging-use external terminals **10** is disposed on the location where the via hole **9** is provided on the insulating substrate **3** on the circuit board **5** (see FIG. **5**(*f*)). Here, positioning the packaging-use external terminal **10** is performed in such a manner that a solder ball is temporarily fixed to each via hole **9**, heated in a reflow furnace, and then joined to the land section **12**. Methods of temporarily fixing the solder ball to the via hole **9** include a method in which the solder ball is affixed to the via hole **9** after applying a flux to the via hole **9**, and a method in which the solder ball is affixed to the via hole **9** after adhering the flux to the solder ball.

(5) Finally, a plurality of semiconductor devices produced on the circuit board **5** are divided into pieces of semiconductor devices (see FIG. **5**(*d*)) by cutting the insulating substrate **3** along its unnecessary part, i.e., along the outer edge of the sealing resin **8** of each semiconductor device. Methods of cutting the insulating substrate **3** include a punching method using die, and an eximer laser cutting method.

As shown in FIG. **6**(*a*), the semiconductor device in accordance with the present embodiment includes the wiring layer **4** on only one of the surfaces of the insulating substrate **3**. However, the wiring layer **4** can be provided on both surfaces of the insulating substrate **3** as shown in FIG. **6**(*b*).

When the wiring layer **4** is formed on both surfaces of the insulating substrate **3**, as shown in FIG. **6**(*b*) the wiring layers **4** on the respective surfaces are electrically connected to each other through the plated via holes **9** as shown in FIG. **6**(*b*) Regarding the wiring layer **4** on the side of the insulating substrate **3**, the side where the first semiconductor chip **1** is not mounted, the area where the packaging-use external terminals **10** are not to be formed are covered with a solder resist **20**, etc. In the area which is not covered with the solder resist **20**, i.e., the area where the packaging-use external terminals **10** are to be provided, the packaging-use external terminals **10** are arranged in an area-array-like pattern.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to the electrode sections **13** of the wiring layer **4** with the wires **7**, if the wires **7** become too close to each other because of the layout of the electrode pads of the first semiconductor chip **1** and the second semiconductor chip **2**, the wires **7** can be arranged as below.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to the same electrode section **13** of the wiring layer **4**, two arrangements shown in FIGS. **7**(*a*) and **7**(*b*) are acceptable. In the arrangement shown in FIG. **7**(*a*), the electrode section **13** of the wiring layer **4**, to which two wires **7** are connected, is arranged to have two parts. In the arrangement shown in FIG. **7**(*b*), an electrode pad **17***a* of the first semiconductor chip **1** is connected to an electrode pad **17***b* of the second semiconductor chip **2** with the wire **7**, and the electrode pad **17***a* is connected to the electrode section **13** of the wiring layer **4** with the wire **7**, thereby connecting each of the electrode pads **17***a* and **17***b* to the electrode section **13**.

When connecting the first semiconductor chip **1** and the second semiconductor chip **2** to different electrode sections **13** of the wiring layer **4**, two arrangements shown in FIGS. **8**(*a*) and **8**(*b*) are acceptable. In the arrangement shown in FIG. **8**(*a*), the electrode pad **17***a* of the first semiconductor chip **1** and the electrode pad **17***b* of the second semiconductor chip **2** are each connected directly to the electrode section **13** of the wiring layer **4** with the wire **7**. In the arrangement shown in FIG. **8**(*b*), dummy pads **18** are

provided on the first semiconductor chip **1**, and the electrode pad **17***b* disposed on the second semiconductor chip **2** is connected to the electrode section **13** of the wiring layer **4** via the dummy pad **18**. This arrangement shown in FIG. **8**(*b*) is more preferable because the overhanging part of the wire **7** is shorter than that in the arrangement shown in FIG. **8**(*a*).

FIGS. **9**(*a*) and **9**(*b*) s how examples of the arrangement of the dummy pads **18** provided on the first semiconductor chip **1**.

Embodiment 2

With reference to FIGS. **10** to **12**, the following descriptions will explain the second embodiment of the present invention. The members having the same structure as those in the above-mentioned first embodiment will be designated by the same reference numbers and their description will be omitted.

A semiconductor device in accordance with the present embodiment is arranged as shown in FIG. **10**. Specifically, a first semiconductor chip **21** is mounted on a circuit board **5** with its circuit formed surface facing the circuit board **5**, i.e., facing down. The circuit board **5** includes an insulating substrate **3**, and a wiring layer **4** formed on the insulating substrate **3**. A second semiconductor chip **22** is mounted on the back surface of the first semiconductor chip **21** through a thermo-compression sheet **6**. The back surf ace of the second semiconductor chip **22** faces the first semiconductor chip **21**. Namely, the back surfaces of the first semiconductor chip **21** and the second semiconductor chip **22** are adhered to each other through the thermo-compression sheet **6**. The thermo-compression sheet **6** is provided as an adhesion layer for holding the second semiconductor chip **22** on the first semiconductor chip **21**.

The first semiconductor chip **21** is electrically connected to first electrode sections (not shown) provided in the wiring layer **4** through metal bumps **23**. The first electrode sections are disposed inside an area of the wiring layer **4**, where the first semiconductor chip **21** is mounted.

Meanwhile, the second semiconductor chip **22** is electrically connected to second electrode sections (not shown) provided in the wiring layer **4** with wires **7**. Since the second electrode sections are used for wire-bonding the second semiconductor chip **22** to the wiring layer **4**, they are disposed outside the area of the wiring layer **4**, where the first semiconductor chip **21** and the second semiconductor chip **22** are mounted.

A resin sheet **24** is provided between the first semiconductor chip **21** and the wiring layer **4**. The resin sheet **24** is formed by extending a resin sheet used in the step of connecting the first semiconductor chip **21** to the wiring layer **4** through the metal bumps **23**.

If electrode pads provided on the circuit formed surface of the first semiconductor chip **21** are made of Al, the metal bumps **23** are preferably made of Au which is easily alloyed with Al. With this arrangement, the metal bumps **23** can be more firmly affixed to the electrode pads.

The material for forming the resin sheet **24** may be a thermoplastic resin or a thermosetting resin. However, the thermoplastic resin is more favorable than the thermosetting resin because the resin sheet **24** is used for the following purpose. Namely, it is used so that the resin extends by heat applied in connecting the first semiconductor chip **21** to the wiring layer **4** with the metal bumps **23**, covers the metal bumps **23** as junctions, and prevents degradation of the junctions caused by shock, etc.

The resin sheet **24** can be a three-layer resin sheet including a layer of a light blocking material such as metallic foil. With this arrangement it is possible to prevent a malfunction of the first semiconductor chip **21** due to a light incident from the surface where the packaging-use external terminals **10** are mounted passing through the semiconductor device. In this case, the size of the metallic foil must be such that the metallic foil is out of contact with the metal bumps **23**.

Although the semiconductor device in accordance with the present embodiment uses the resin sheet **24**, the following arrangement is also acceptable. Namely, the semiconductor chip **21** is mounted without using the resin sheet **24**, and then the space produced at a junction of the first semiconductor chip **21** and the wiring layer **4** is filled with a liquid resin, etc., thereby covering the metal bumps **23** as the junctions.

Next, referring to FIGS. **11**(*a*) to **11**(*g*), the following descriptions will explain the process (including steps (1) to (7)) for manufacturing the semiconductor device in accordance with the present embodiment.

(1) First, the resin sheet **24** and the metal bumps **23** are disposed on the circuit board **5** (see FIG. **11**(*a*)). In this case, each of the metal bumps **23** is disposed on the first electrode section provided in the wiring layer **4** on the circuit board **5**. The resin sheet **24** is disposed on the circuit board **5** at the location where the first semiconductor chip **21** and the second semiconductor chip **22** are to be mounted.

(2) Next, the first semiconductor chip **21** is connected to the wiring layer **4** on the circuit board **5** by a flip chip method in a face-down mode (see FIG. **11**(*b*)).

(3) Then, the second semiconductor chip **22** is mounted on the back surface of the first semiconductor chip **21** (see FIG. **11**(*c*)). When the second semiconductor chip **22** is in a state of wafer, the insulating thermo-compression sheet **6** is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips **22**. The second semiconductor chip **22** is accurately positioned at a specific location on the circuit formed surface of the first semiconductor chip **21**.

Like the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet **6** to the back surface of the second semiconductor chip **22** in advance.

(4) Then, the second semiconductor chip **22** is electrically connected to the wiring layer **4** on the circuit board **5** (see FIG. **11**(*d*)). More specifically, each of the electrode pads disposed on the circuit formed surface of the second semiconductor chip **22** is connected to the second electrode section of the wiring layer **4** with the wire **7**.

(5) Thereafter, the first semiconductor chip **21**, the second semiconductor chip **22**, and the wires **7**, provided on the circuit board **5**, are sealed with a sealing resin **8** (see FIG. **11**(*e*)). The method of forming the sealing resin **8** is similar to that described in the first embodiment.

(6) Then, each of the packaging-use external terminals **10** is disposed at a location of a via hole **9** formed in the insulating substrate **3** of the circuit board **5** (see FIG. **11**(*f*)).

(7) Finally, a plurality of semiconductor devices produced on the circuit board **5** are divided into pieces of semiconductor devices by cutting the insulating substrate **3** along the unnecessary part of the insulating substrate **3** of the circuit board **5**, i.e., along the outer edge of the sealing resin **8** of each semiconductor device unnecessary parts (see FIG. **11**(*d*)). The methods of cutting the insulating substrate **3** include a punching method using a die, and an eximer laser method.

In the above-described first embodiment (and in the second embodiment), when mounting the second semiconductor chips **2** (**22**) on the first semiconductor chips **1** (**21**), if the first semiconductor chips **1** (**21**) and the second semiconductor chips **2** (**22**) have different shapes, the second semiconductor chips **2** (**22**) may protrude from the first semiconductor chips **1** (**21**) as shown in FIG. **12**(*a*). In this case, since the protruded part of the second semiconductor chip **2** (**22**) is of low strength, the second semiconductor chip **2** (**22**) may be possibly destroyed by shock produced when, for example, wire-bonding the electrode pads **17***b* of the second semiconductor chip **2** (**22**) to the wiring layer **4**.

In order to solve the problem, as shown in FIG. **12**(*b*), a support member **19** having the same height and the same shape as the first semiconductor device **1** (**21**) is fixed under the protruded part of the second semiconductor chip **2** (**22**). By reinforcing the second semiconductor chip **2** (**22**) with the support member **19**, destruction thereof can be prevented. The support member **19** is preferably made of Silicon (Si) in order to reduce generation of stress, etc. against a heat load applied during and after manufacturing the semiconductor device with the CSP structure. In addition, the support member **19** has the same coefficient of linear expansion as the second semiconductor chip **2** (**22**).

The above-mentioned semiconductor devices in accordance with Embodiments 1 and 2 include two laminated semiconductor chips. However, the present invention can be arranged to include three or more laminated semiconductor chips. In this case, the third semiconductor chip can be mounted on the top of the two semiconductor chips with its circuit formed surface facing up and wire-bonded to the wiring layer **4**. Alternatively, the third semiconductor chip can be mounted on the top of the two semiconductor chips with its circuit formed surface facing down through metal bumps by providing electrode pads for disposing the metal bumps on the circuit formed surface of the second semi conductor chip **2** (**22**).

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

(a) forming a first adhesion layer on a back surface of a first wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;

(b) producing separate first semiconductor chips from said first wafer by dicing;

(c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer;

(d) forming a second adhesion layer on a back surface of a second wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;

(e) producing separate second semiconductor chips from said second wafer by dicing; and

(f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip.

2. The method of manufacturing the semiconductor device as set forth in claim **1**, further comprising the steps of:

(g) wire-bonding an electrode section of said first semiconductor chip to an electrode section of said wiring layer with a first wire;

(h) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a second wire; and

(i) sealing said first and second semiconductor chips and said first and second wires,

said steps (g) to (i) being included after said step(f).

3. The method of manufacturing the semiconductor device as set forth in claim **2**, further comprising the steps of:

(j) forming a metal ball on each end of said second wire;

(k) connecting one of the metal balls to the electrode section of said second semiconductor chip;

(l) cutting said second wire; and

(m) making a surface of the metal ball connected to said second semiconductor chip flat;

said steps (j) to (m) being included between said steps (g) and (h).

4. The method of manufacturing the semiconductor device as set forth in claim **1**, further comprising the steps of:

(g) wire-bonding an electrode section of said first semiconductor chip to an electrode section of said wiring layer with a first wire;

(h) forming a metal ball on each end of a second wire;

(i) connecting one of the metal balls to the electrode section of said second semiconductor chip;

(j) cutting said second wire;

(k) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with said second wire; and

(l) sealing said first and second semiconductor chips and said first and second wires.

5. The method of manufacturing the semiconductor device as set forth in claim **1**, further comprising the steps of:

(g) forming a metal ball on each end of a first wire;

(h) connecting one of the metal balls to an electrode section of said first semiconductor chip;

(i) cutting said first wire;

(j) wire-bonding the electrode section of said first semiconductor chip to an electrode section of said wiring layer with said first wire;

(k) wire-bonding the electrode section of said first semiconductor chip to an electrode section of said second semiconductor chip with a second wire;

(l) sealing said first and second semiconductor chips and said first and second wires.

6. The method of manufacturing the semiconductor device as set forth in claim **1**, further comprising the steps of:

(g) forming a metal ball on each end of a first wire;

(h) connecting one of the metal balls to a dummy pad providing on said first semiconductor chip;

(i) cutting said first wire;

(j) wire-bonding the dummy pad of said first semiconductor chip to an electrode section of said wiring layer with said first wire;

(k) wire-bonding the dummy pad of said first semiconductor chip to an electrode section of said second semiconductor chip with a second wire; and

(l) sealing said first and second semiconductor chips and said first and second wires.

7. A method of manufacturing a semiconductor device comprising:

(a) forming an insulating layer and a metal bump on a wiring layer;

(b) mounting a first semiconductor chip on said wiring layer with its circuit-formed surface facing said wiring layer;

(c) forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer;

(d) producing separate second semiconductor chips from the wafer by dicing;

(e) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip;

(f) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a wire; and

(g) sealing said first and second semiconductor chips and said wire.

8. The method of manufacturing the semiconductor device as set forth in claim **7**, further comprising the steps of:

(h) forming a metal ball on each of said wire;

(i) connecting one of the metal balls to the electrode section of said second semiconductor chip;

(j) cutting said wire; and

(k) making a surface of the metal ball connected to said second semiconductor chip flat;

said steps (h) to (k) being including between said steps (e) and (f).

9. The method of manufacturing the semiconductor device as set forth in claim **7**, further comprising the steps of:

(h) forming a metal ball on each of said wire;

(i) connecting one of the metal balls to the electrode section of said second semiconductor chip; and

(j) cutting said wire;

said steps (h) to (j) being including between said steps (e) and (f).

10. A method of manufacturing a semiconductor device comprising:

(a) applying an adhesive paste on a wiring layer, and thereafter, mounting a first semiconductor chip on said wiring layer with a back surface of said semiconductor chip facing said wiring layer, the back surface having no circuit formed thereon;

(b) forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer;

(c) producing separate second semiconductor chips from the wafer by dicing; and

(d) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip.

11. The method of manufacturing the semiconductor device as set forth in claim **10**, further comprising the steps of:

(e) wire-bonding an electrode section of said first semiconductor chip to an electrode section of said wiring layer with a first wire;

(f) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a second wire; and

(g) sealing said first and second semiconductor chips and said wires,

said steps (e) to (g) being included after said step (d).

12. The method of manufacturing the semiconductor device as set forth in claim **10**, further comprising the steps of:

(e) wire-bonding an electrode section of said first semiconductor chip to an electrode section of said wiring layer with a first wire;

(f) forming a metal ball on each end of a second wire;

(g) connecting one of the metal balls to the electrode section of said second semiconductor chip; and

(h) cutting said second wire;

(i) wire-bonding an electrode section of said wiring layer to the electrode section of said second semiconductor chip with said second wire;

(j) sealing said first and second semiconductor chips and said first and second wires,

said steps (e) to (j) being included after said step (d).

13. The method of manufacturing the semiconductor device as set forth in claim **10**, further comprising the steps of:

(e) forming a metal ball on each end of a first wire;

(f) connecting one of the metal balls to the electrode section of said first semiconductor chip; and

(g) cutting said first wire;

(h) wire-bonding an electrode section of said wiring layer to the electrode section of said first semiconductor chip with said first wire;

(i) wire-bonding the electrode section of said first semiconductor chip to an electrode section of said second semiconductor chip with a second wire;

(j) sealing said first and second semiconductor chips and said first and second wires,

said steps (e) to (j) being included after said step (d).

14. The method of manufacturing the semiconductor device as set forth in claim **10**, further comprising the steps of:

(e) forming a metal ball on each end of a first wire;

(f) connecting one of the metal balls to a dummy pad providing on said first semiconductor chip;

(g) cutting said first wire;

(h) wire-bonding the dummy pad of said first semiconductor chip to an electrode section of said wiring layer with said first wire;

(i) wire-bonding the dummy pad of said first semiconductor chip to an electrode section of said second semiconductor chip with a second wire; and

(j) sealing said first and second semiconductor chips and said first and second wires,

said steps (e) to (j) being included after said step (d).

15. A method of manufacturing a semiconductor device comprising:

(a) forming a first adhesion layer on a back surface of a first wafer, no circuit being formed on the back surface of the first wafer;

(b) producing separate first semiconductor chips from said first wafer by dicing;

(c) mounting at least one of said first semiconductor chips on a wiring layer with the back surface of the at least one first semiconductor chip facing said wiring layer;

(d) forming a second adhesion layer on a back surface of a second wafer, no circuit being formed on the back surface of the second wafer;

(e) producing separate second semiconductor chips from said second wafer by dicing; and

(f) mounting at least one of said second semiconductor chips on said at least one of said first semiconductor chip with the back surface of the at least one second semiconductor chip facing said at least one of said first semiconductor chips.

* * * * *

US006731013B2

(12) **United States Patent**
Juso et al.

(10) **Patent No.: US 6,731,013 B2**
(45) **Date of Patent: May 4, 2004**

(54) **WIRING SUBSTRATE, SEMICONDUCTOR DEVICE AND PACKAGE STACK SEMICONDUCTOR DEVICE**

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(73) Assignee: **Sharp Kabushiki Kaisha**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 30 days.

(21) Appl. No.: **09/873,338**

(22) Filed: **Jun. 5, 2001**

(65) **Prior Publication Data**

US 2002/0000327 A1 Jan. 3, 2002

(30) **Foreign Application Priority Data**

Jun. 28, 2000 (JP) 2000-194732

(51) **Int. Cl.**[7] **H01L 23/48**

(52) **U.S. Cl.** **257/779**; 257/780; 257/783; 257/784; 257/786; 257/787; 174/52.2; 174/52.4; 361/772; 361/777; 361/808

(58) **Field of Search** 257/780, 782, 257/783, 784, 786, 700, 701, 737, 738, 787, 778, 779; 174/52.2, 52.3, 52.4; 361/767, 807, 808, 809, 810, 772, 777

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Primary Examiner—Alonzo Chambliss
(74) *Attorney, Agent, or Firm*—Nixon & Vanderhye

(57) **ABSTRACT**

A wiring substrate of the present invention includes a terminal section, provided on a first surface of an insulating substrate, for wire or flip-chip bondings; a land section, provided on the insulating substrate, for an external connection terminal; wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section; and a support pattern, provided on the second surface corresponding in position to the terminal section, for improving bondings. The wiring substrate can relieve connection failure in bondings.

25 Claims, 23 Drawing Sheets

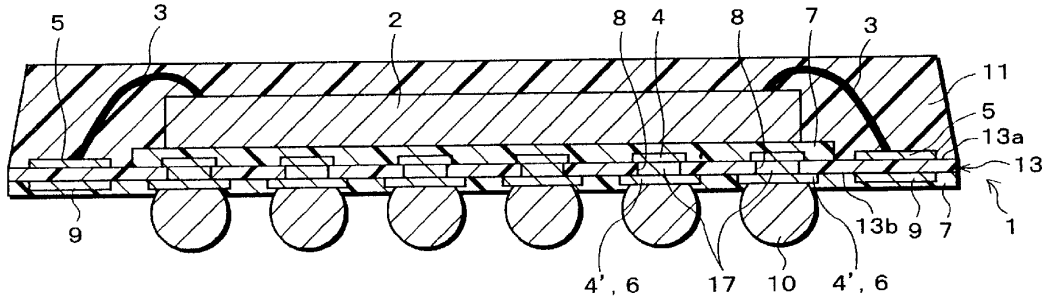


FIG.1

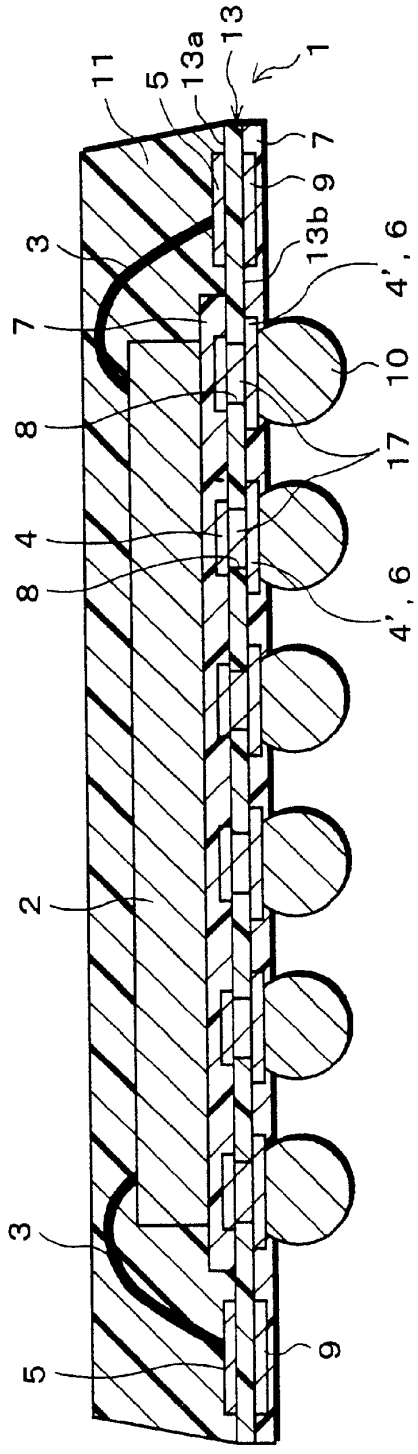


FIG.2 (a)

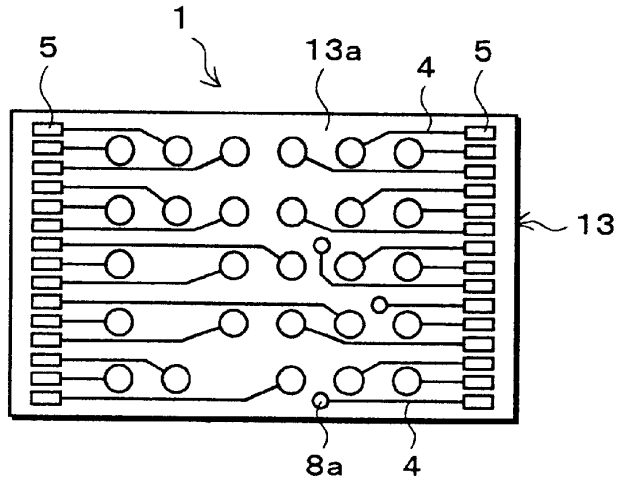


FIG.2 (b)

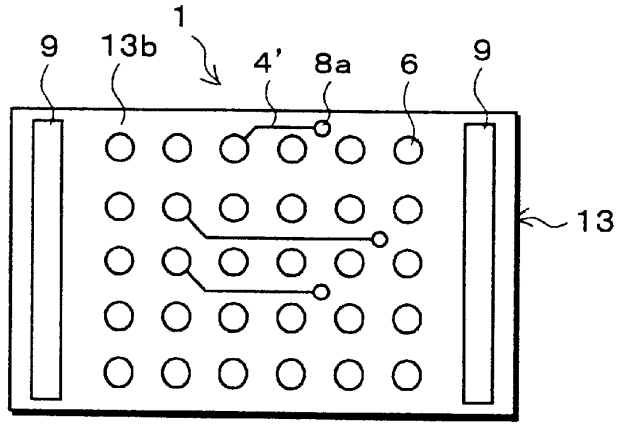


FIG.2 (c)

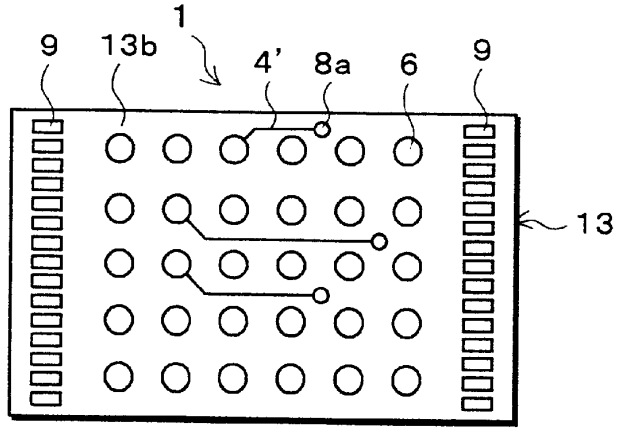


FIG.3 (a)

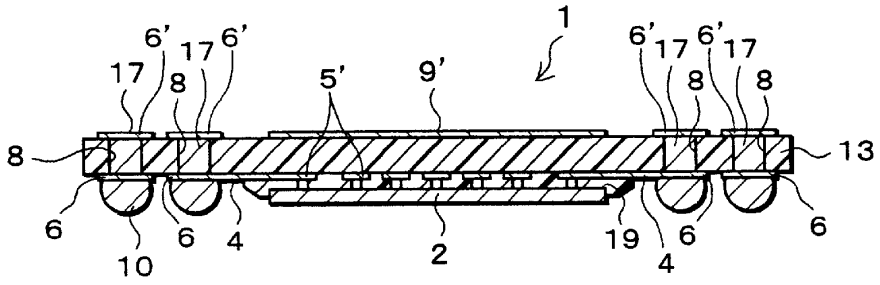
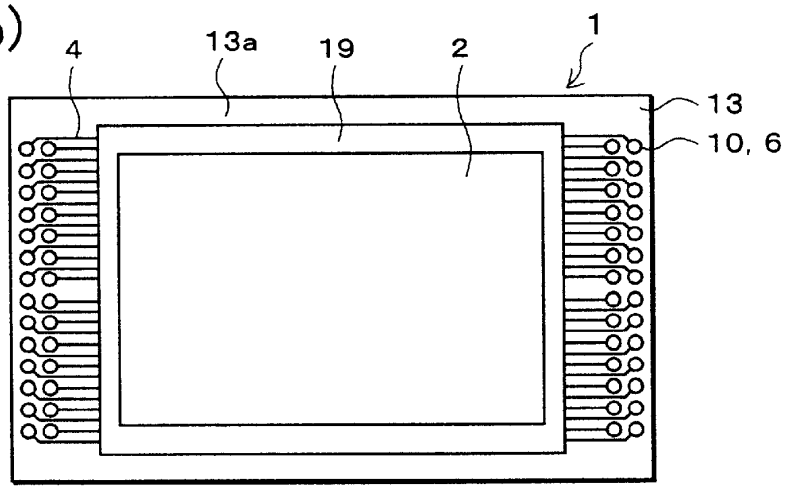


FIG.3 (b)



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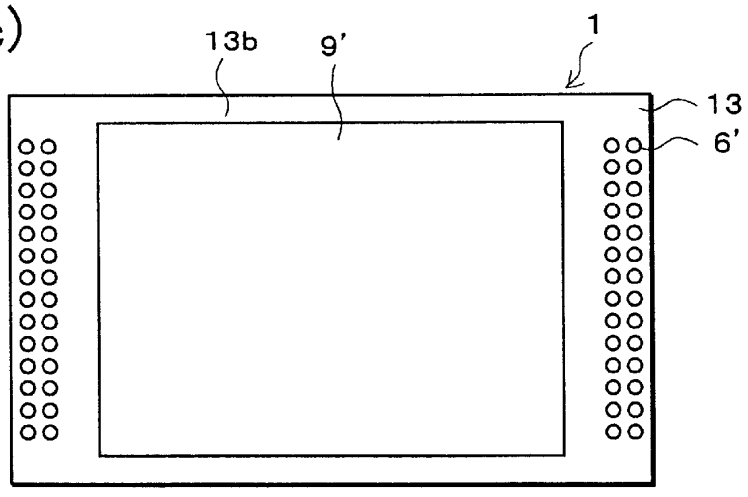


FIG.4 (a)

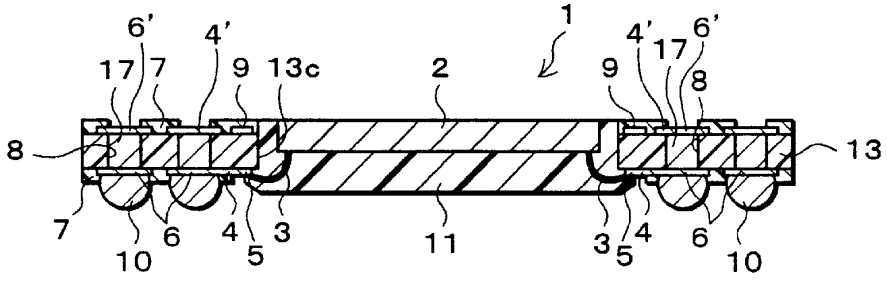


FIG.4 (b)

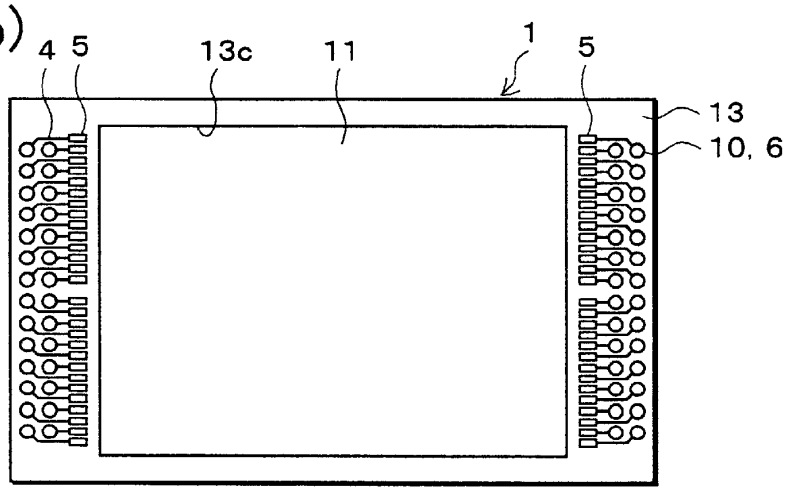


FIG.4 (c)

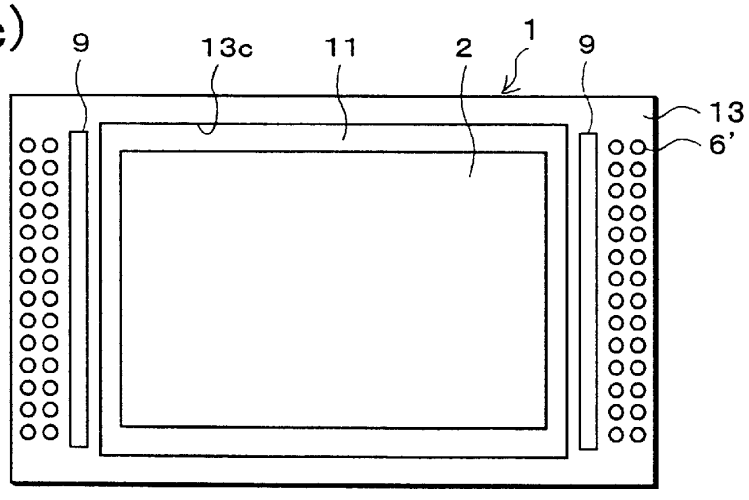


FIG.5 (a)

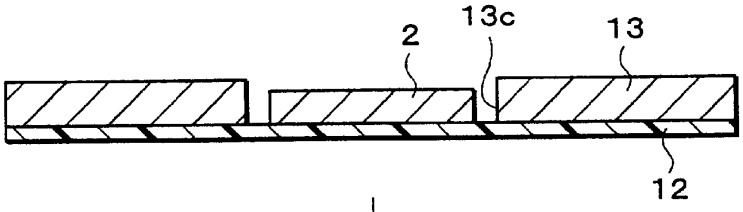


FIG.5 (b)

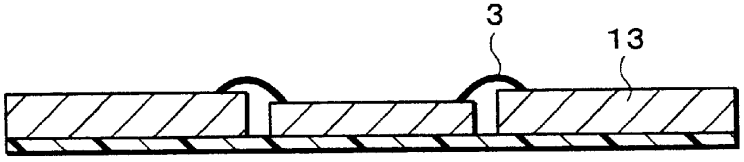


FIG.5 (c)

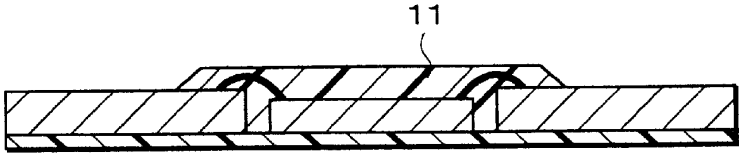


FIG.5 (d)

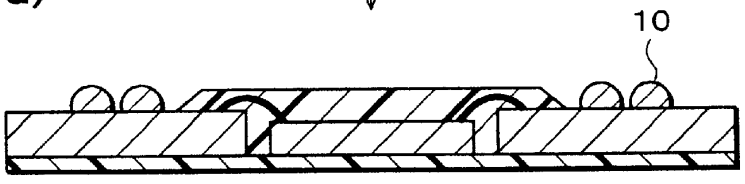


FIG.5 (e)

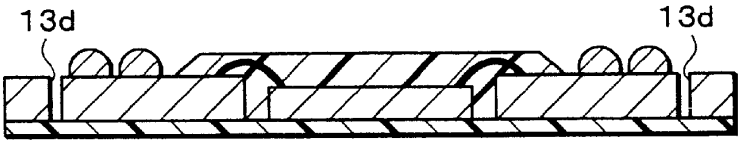


FIG.6

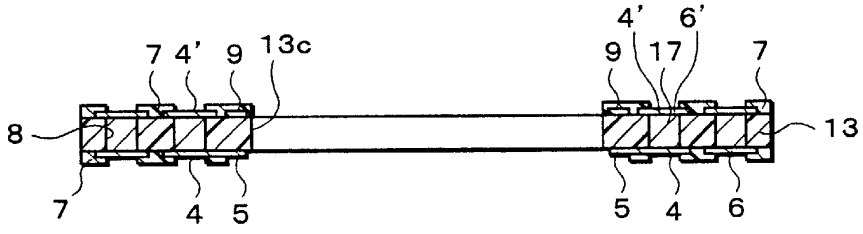


FIG.7 (a)

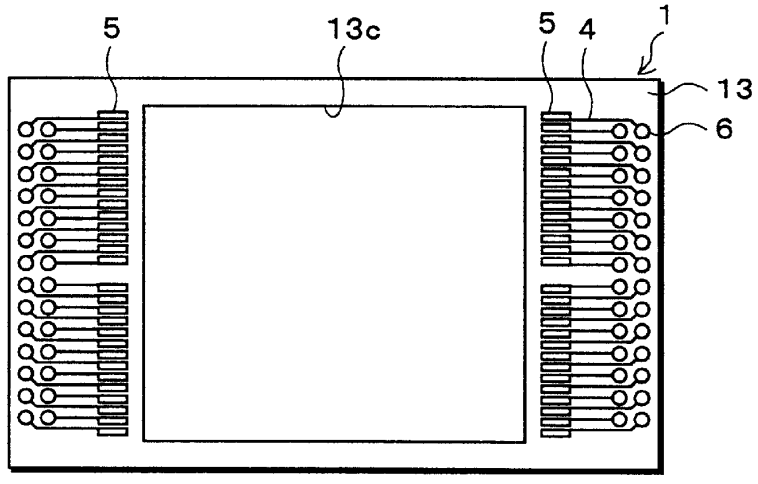


FIG.7 (b)

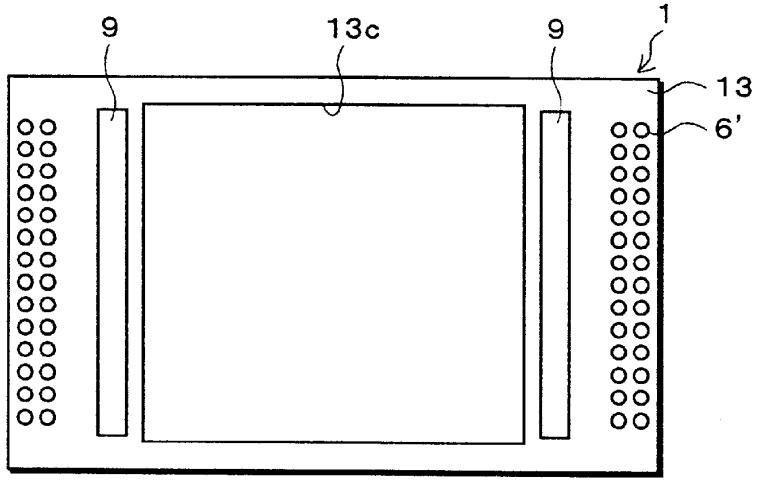


FIG.8

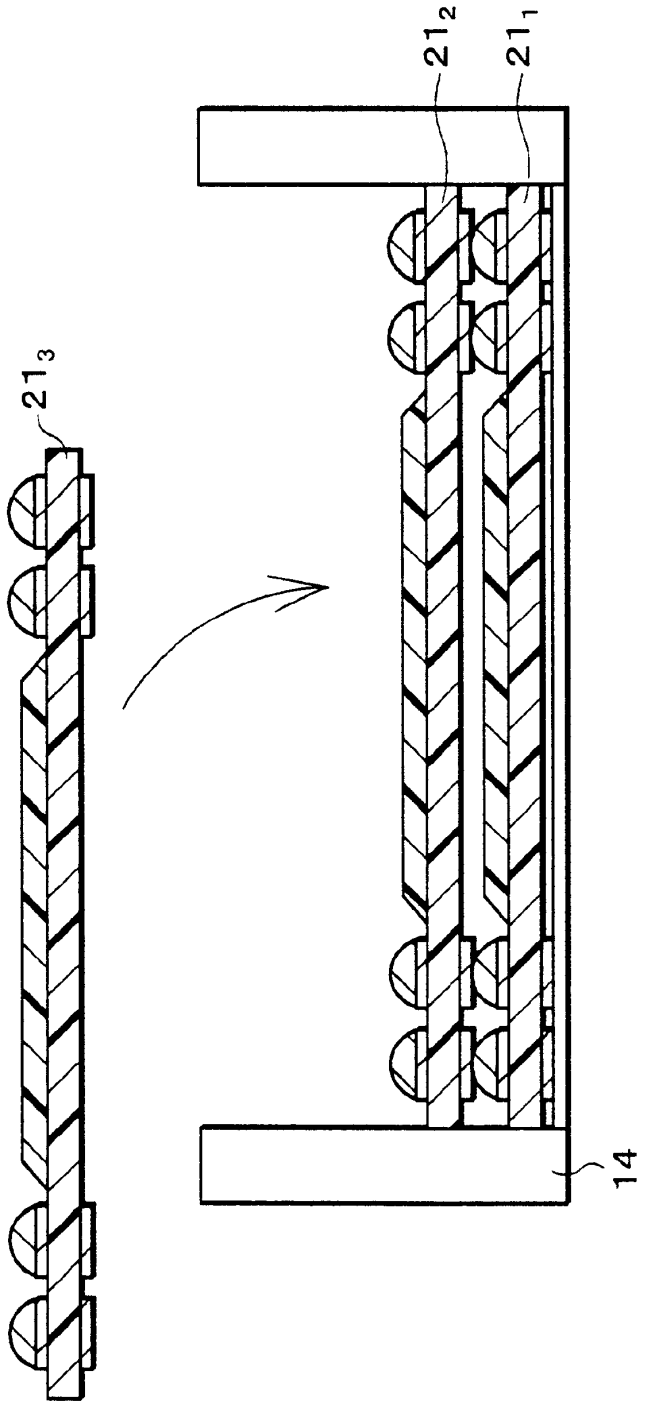


FIG.9

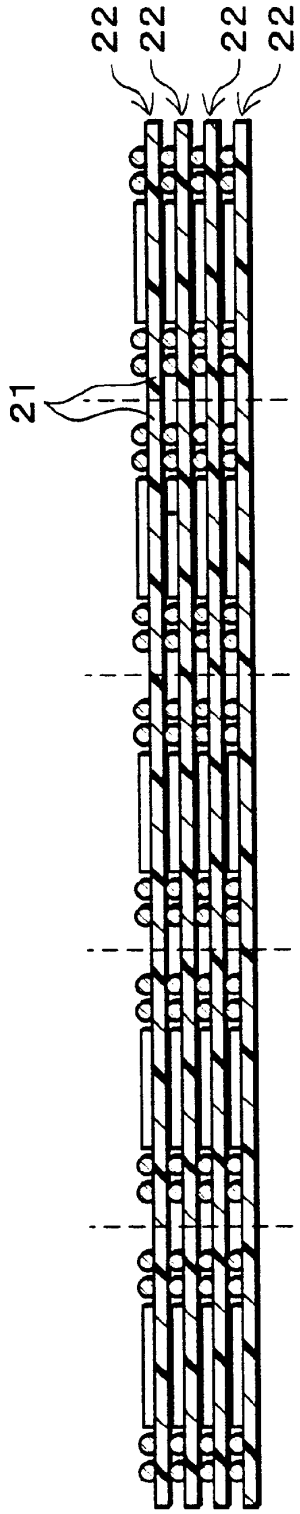


FIG.10 (a)

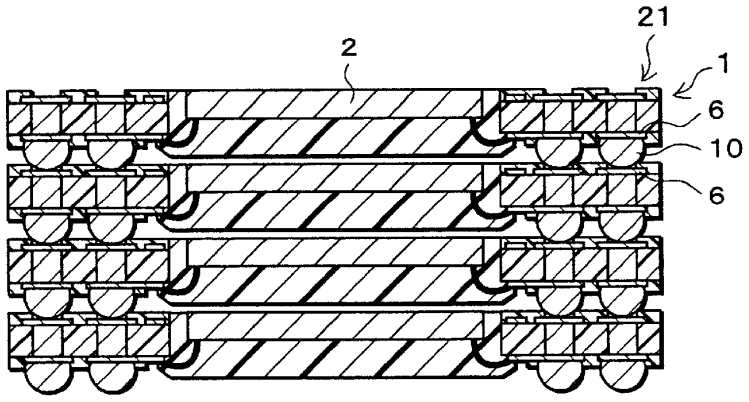


FIG.10 (b)

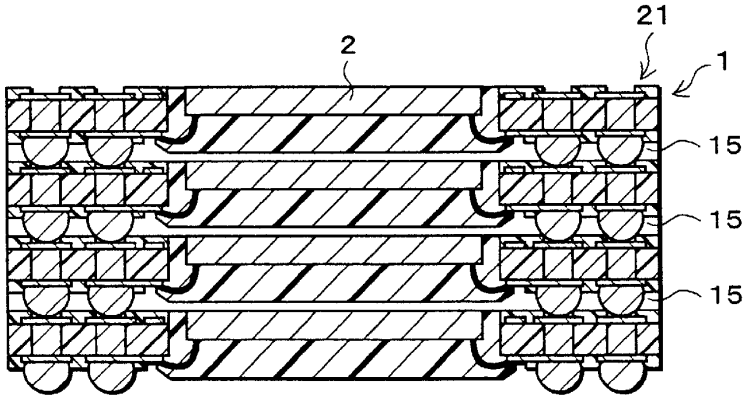


FIG.11 (a)

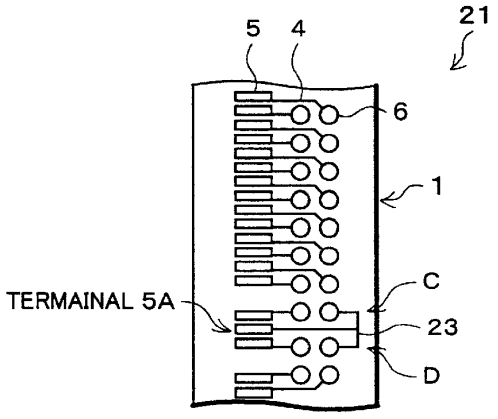


FIG.11 (b)

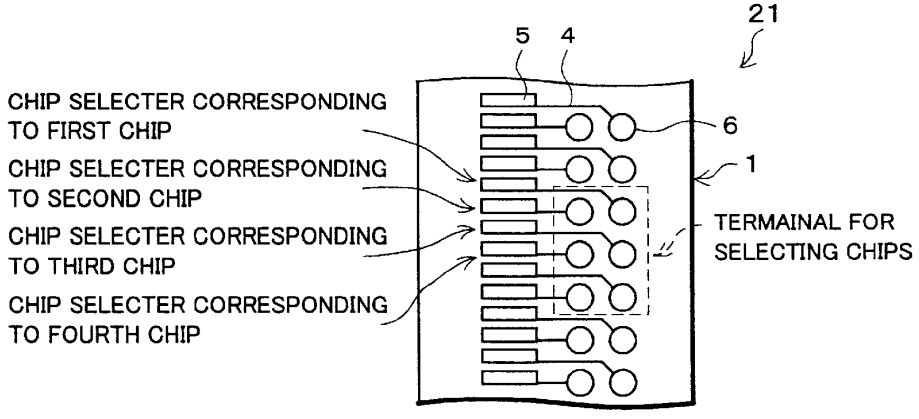


FIG.12

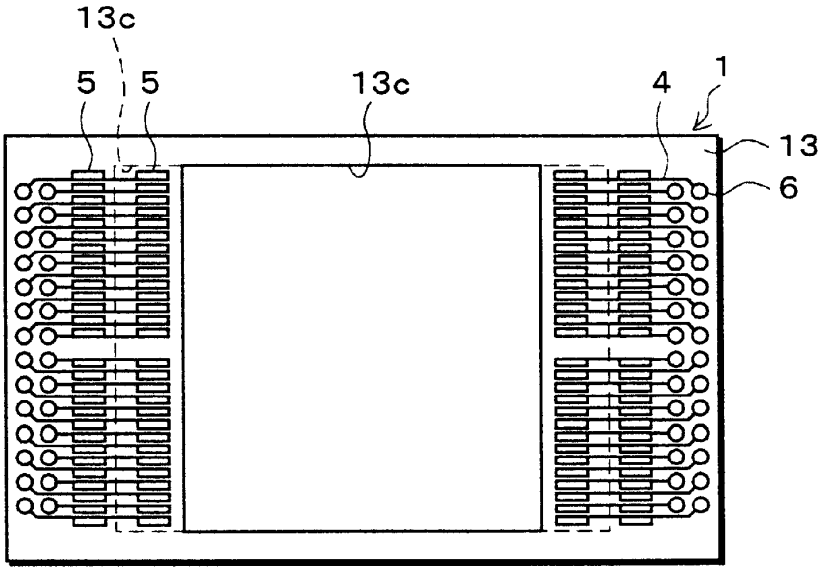


FIG.13

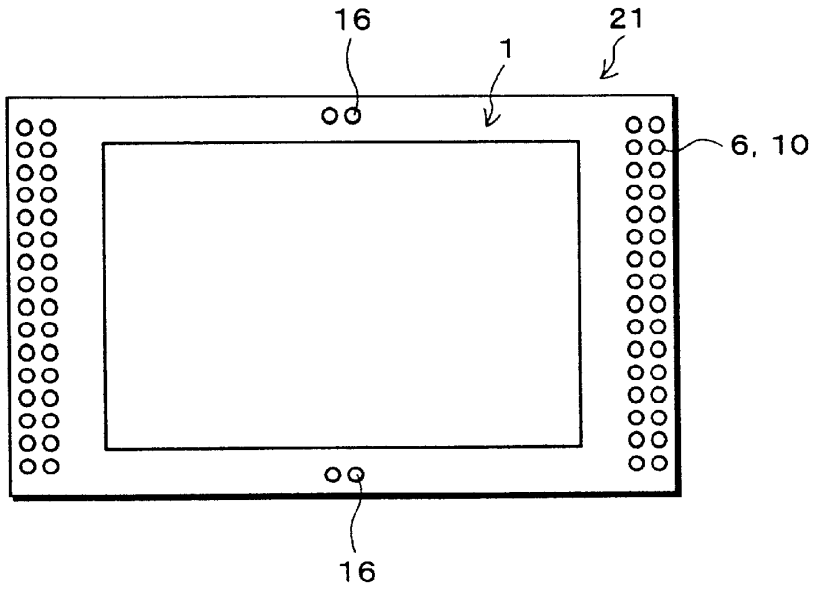


FIG.14 (a)

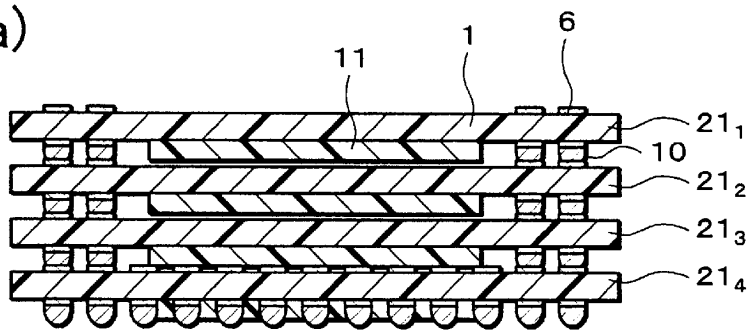


FIG.14 (b)

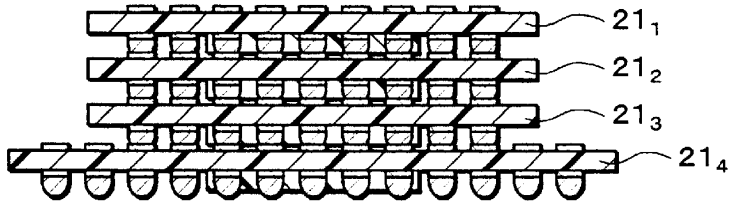


FIG.14 (c)

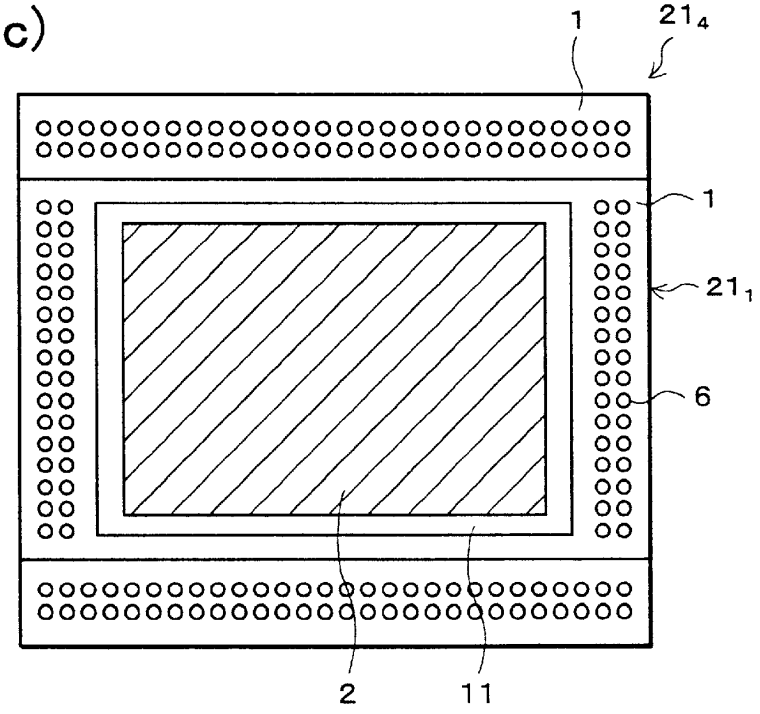


FIG.15

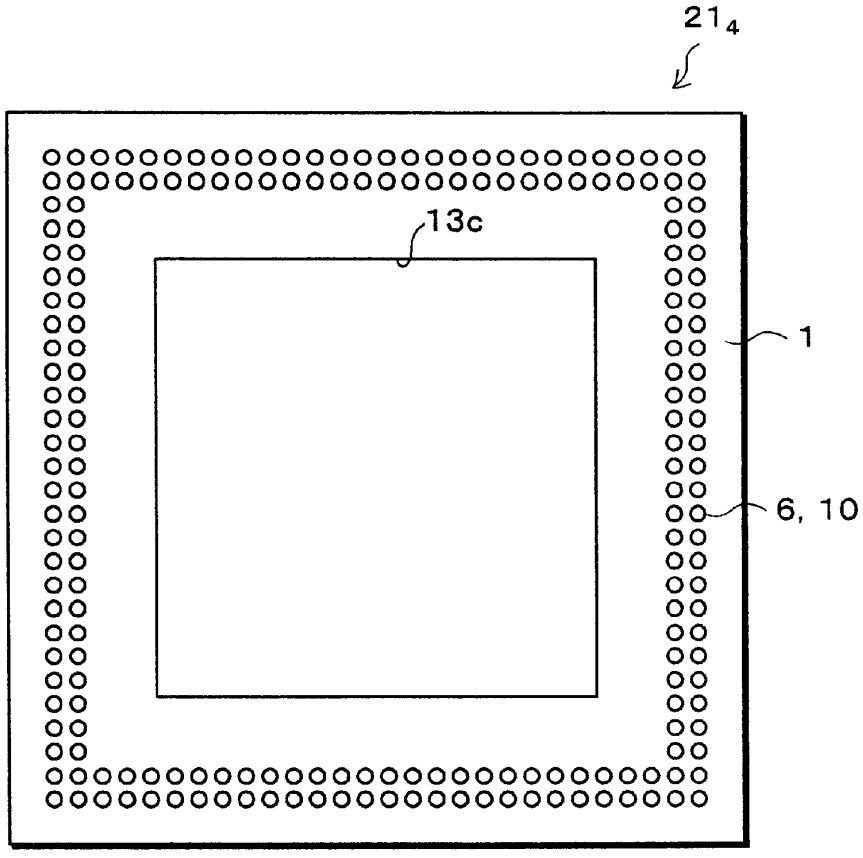


FIG.16 (a)

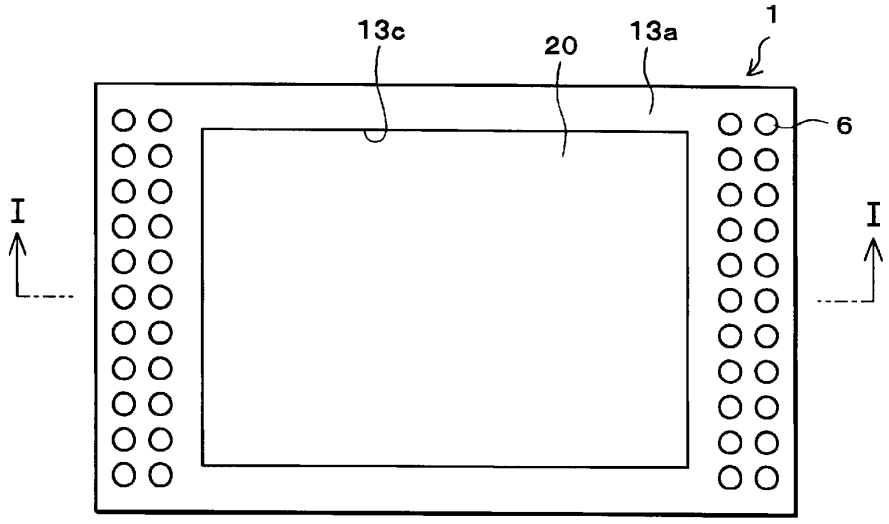


FIG.16 (b)

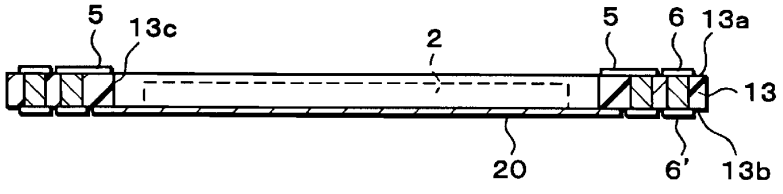


FIG.17

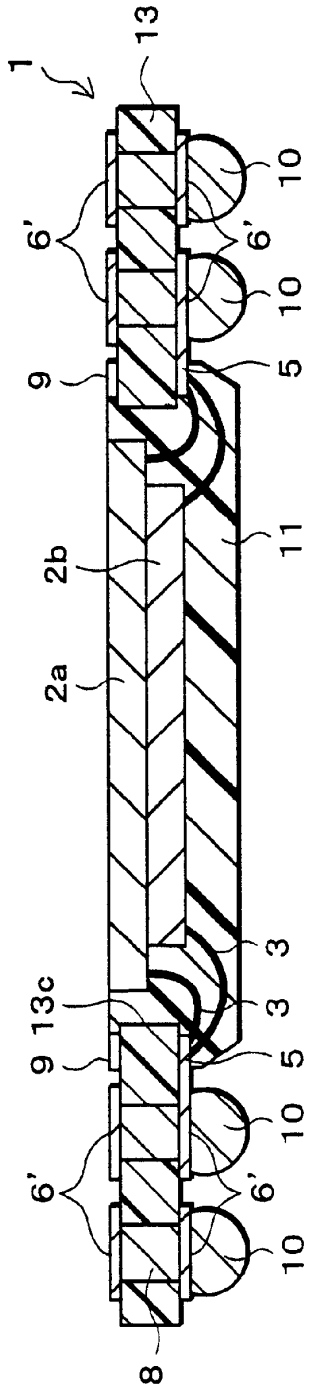


FIG.18

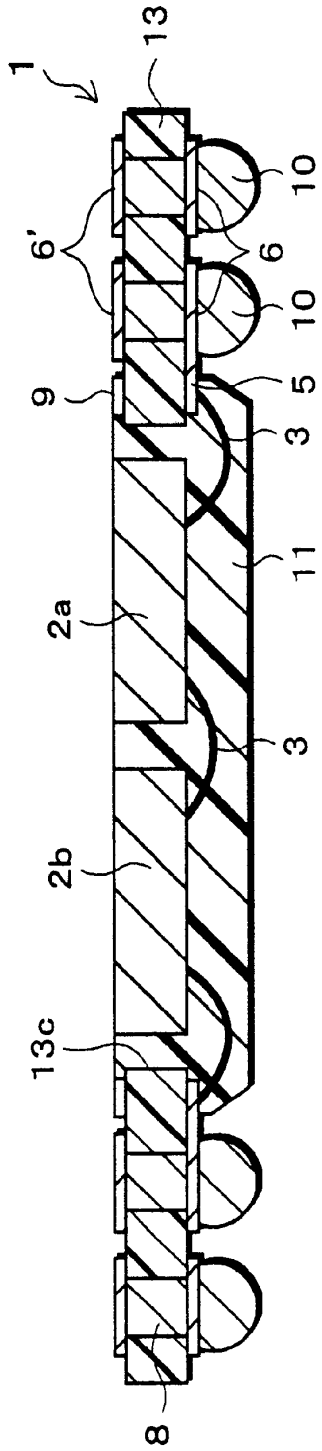


FIG.19

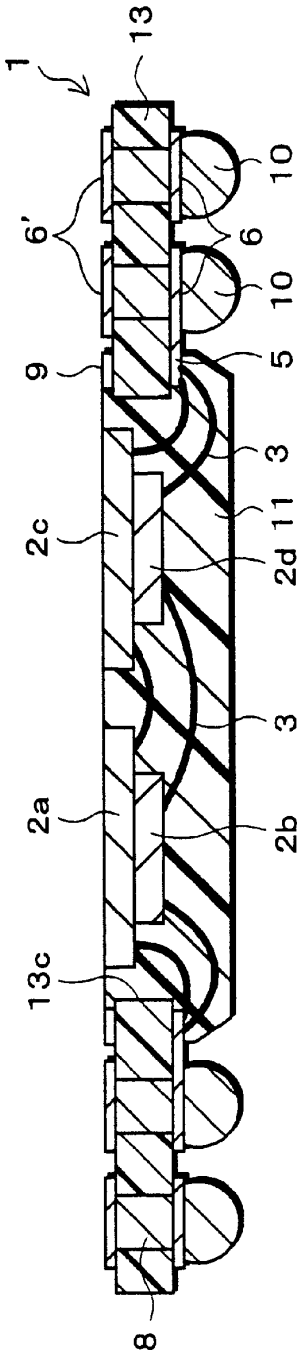


FIG.20

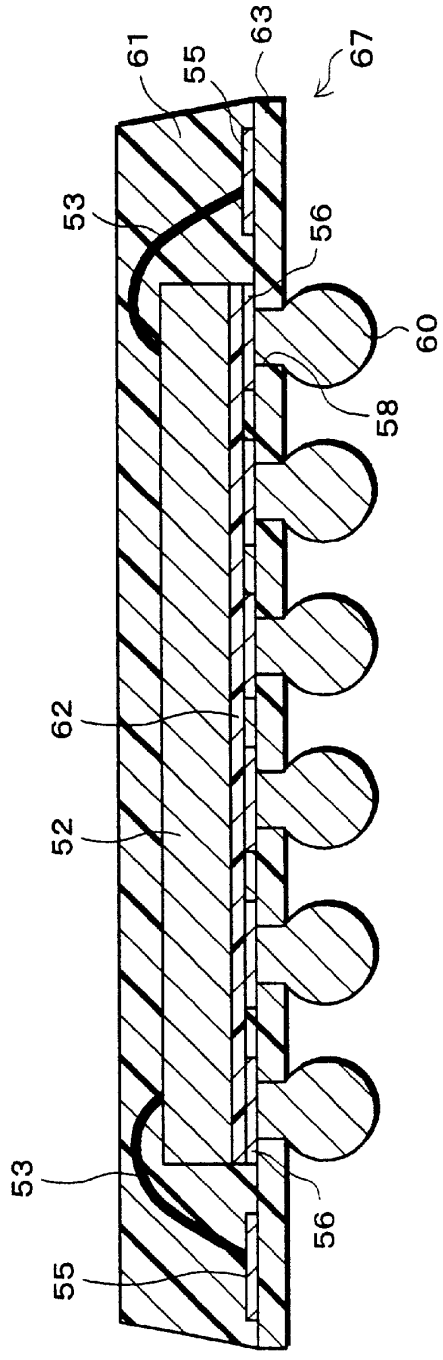


FIG.21

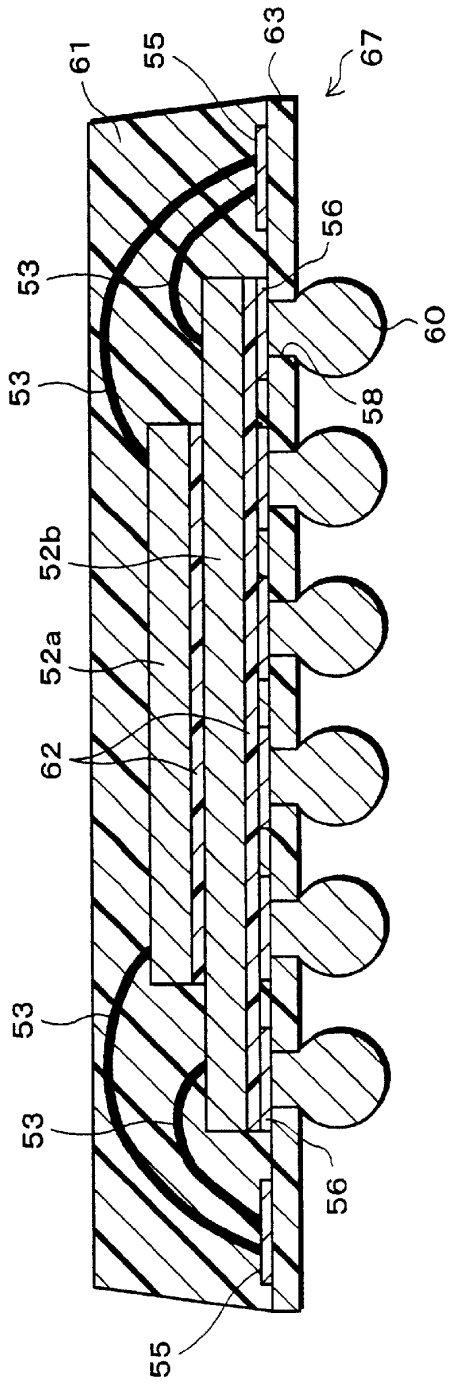


FIG.22

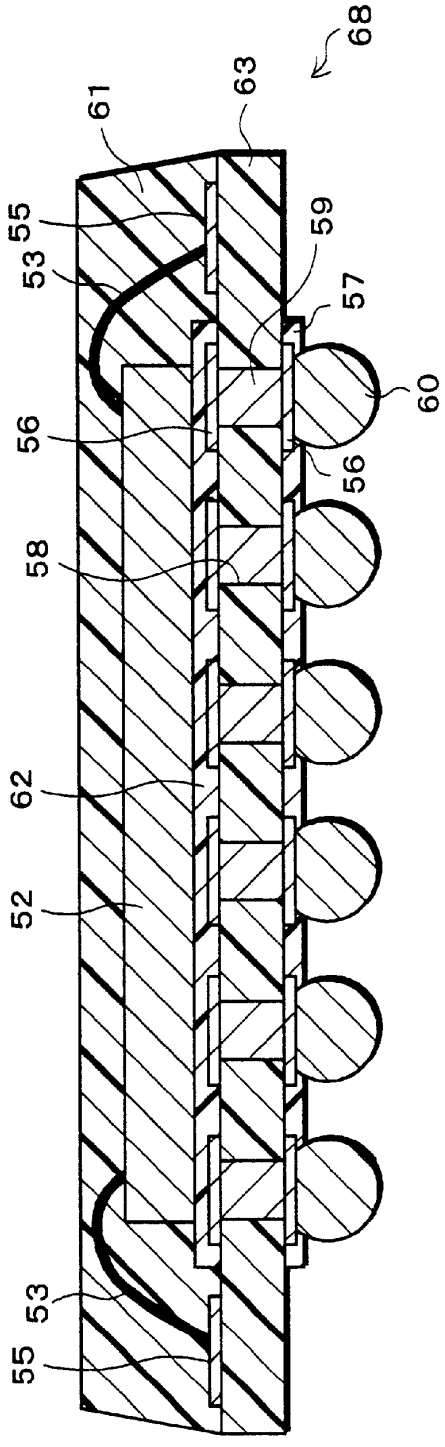
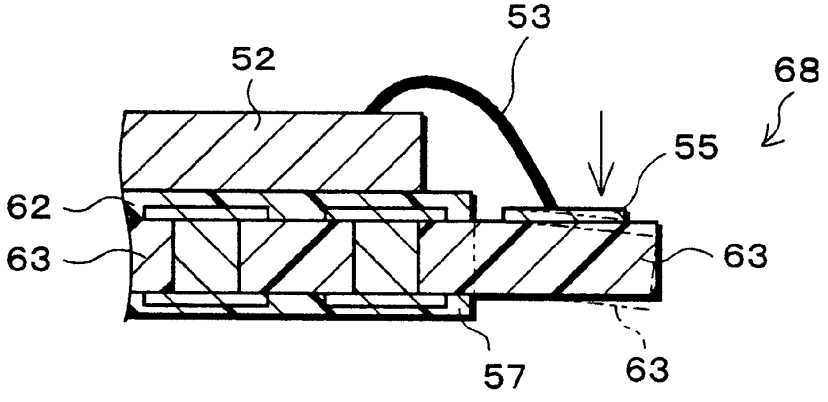


FIG.23



WIRING SUBSTRATE, SEMICONDUCTOR DEVICE AND PACKAGE STACK SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

This invention relates to a semiconductor device which is miniaturized to almost chip size to be suitable particularly for density packaging, and relates to a wiring substrate (printed circuit board) therefor, and to a package stack semiconductor device having a plurality of such a semiconductor device.

BACKGROUND OF THE INVENTION

Recently QFP (Quad Flat Package) type, BGA (Ball Grid Array) type, and CSP (Chip Size package) type semiconductor devices have been widely used as what meets the needs of miniaturizing electronic equipment.

These semiconductor devices need more and more external connection terminals since signal processing of a semiconductor chip (semiconductor-element) mounted therein has been highly speeded and highly facilitated. In such case, the BGA type whose external connection terminals are provided on a bottom face of a semiconductor device in a two-dimensional manner is widely adopted.

Of these BGA type semiconductor devices, conventionally known is a semiconductor device whose semiconductor chip and wiring substrate are connected to each other by wire bonding with a circuit forming surface of the semiconductor chip facing upward, wherein the semiconductor chip is conducted to external connection terminals through the wiring pattern of the wiring substrate. "Upward" means that the circuit forming surface is on the other side of the surface of semiconductor chip facing the wiring substrate.

Such a conventional resin-sealed semiconductor device is disclosed in Japanese Unexamined Patent Publication No. 121002/1997 (Tokukaihei 9-121002) (published date: May 6, 1997).

A semiconductor device which has a structure like this, as shown in FIG. **20**, has a wiring substrate **67**, a semiconductor chip **52** which is mounted on the wiring substrate **67**, an Au wire **53** which connects the semiconductor chip **52** to a terminal section **55** of the wiring substrate **67**, a resin sealing section **61** which seals the semiconductor chip **52** and the Au wire **53** with resin by transfer molding.

The wiring substrate **67** has an insulating substrate **63**, an insulating material **62** as an insulating layer on the chip side, and a wiring pattern provided between the insulating substrate **63** and the insulating material **62**. That is, the wiring substrate **67** has a metallic wiring pattern which is formed on the insulating substrate **63** provided with a through hole **58**, and the insulating material **62** is bonded with the metallic wiring pattern thereon.

Further, the wiring substrate **67** is provided with the through hole **58** through the insulating substrate **63** in a direction of thickness according to the wiring pattern. Thus, the wiring pattern is partially exposed on the through hole **58**, and the exposed portion of the wiring pattern makes up a land section **56** in FIG. **20**.

In addition, the wiring substrate **67** includes an external connection terminal **60** which is formed as a solder ball by reflow soldering. Thus, through the through hole **58**, the external connection terminal **60** is connected to the land section **56** provided on the upper side of the through hole **58**, and hangs down like a ball from the lower side of the through hole **58**.

Among such semiconductor devices, there has been known a semiconductor device having a plurality of semiconductor chips mounted therein in order to increase added values and capacity of a memory and the like in portable devices. For example, a multi-chip module which is provided with a plurality of board-shaped semiconductor chips side by side (in a direction of surface) is known.

However, since semiconductor chips are provided side by side, it is impossible to make a semiconductor device whose area (the area of bottom surface) is smaller than the total area of these semiconductor chips.

In view of this drawback, there has been proposed a semiconductor device (hereinbelow, referred to as stacked package) which improves packaging density by stacking a plurality of semiconductor chips in a direction of thickness and putting these chips in a semiconductor device.

An example of such a stacked package is disclosed in Japanese Unexamined Patent Publication No. 204720/1999 (Tokukaihei 11-204720) (published date: Jul. 30, 1999). The stacked package mentioned above, as shown in FIG. **21**, has semiconductor chips **52***a* and **52***b* which are stacked together to be mounted on the wiring substrate **67** which insulates electricity. Further, an external connection terminal **60** is provided in a matrix pattern on a land section **56** in the stacked package so that the external connection terminal **60** hangs down from the lower surface of the wiring substrate **67**. Thus, the stacked package has the CSP structure which has almost the same size as the semiconductor chip **52***a* and **52***b*.

The method of fabricating the stacked package like this is as follows. In the first place, the first semiconductor chip **52***b* is die-bonded on the wiring substrate **67** with its circuit forming surface facing upward, and then the second semiconductor chip **52***a* is die-bonded thereon.

Thereafter, each semiconductor chip **52***a*, **52***b* is connected to the terminal section **55** of the wiring substrate **67** with an Au wire **53** by wire bonding. In addition, each semiconductor chip **52***a*, **52***b*, and the Au wire **53** are sealed with a resin sealing section **61** by transfer molding. Then, a solder ball is provided as the external connection terminal **60** on the land **56** by reflow soldering. The ball is used as the external connection terminal **60**. The stacked package mentioned above is produced this way.

Depending on the type of the semiconductor chips **52***a* and **52***b* and the position where the external connection terminals **60** are drawn, it is sometimes impossible to form wiring patterns freely on the wiring substrate **67** which has a single layer wiring pattern like the semiconductor device mentioned above. Thus, as shown in FIG. **22**, a multi-layer wiring substrate **68** whose wiring pattern, made of Cu, is provided on its both surfaces is sometimes used.

The wiring pattern of the multi-layer wiring substrate is provided not only on the surface of the insulating substrate **63**, which is a base material, where the semiconductor chip is mounted (hereinbelow referred to as side A), but also on the surface where the external connection terminal **60** is formed (hereinbelow referred to as side B). The wiring pattern of side B is usually protected with a solder resist **57**.

Further, conduction is ensured between the land section **56** of the wiring pattern on side A and the land section **56** of the wiring pattern on side B which faces side A through the through hole **58**, by filling the through hole **58** with a conductor **59** such as a conductive paste.

However, there is a problem. As shown in FIG. **23**, in the foregoing conventional wiring substrate **68** which is provided with the wiring patterns on side A and side B,

inadequate wire bonding is incurred between the semiconductor chip **52** and the terminal section **55**.

That is, when the semiconductor chip **52** and the terminal section **55** are connected by wire bonding, the load applied on the terminal section **55** in a direction of thickness of the insulating substrate **63** to make connection causes deformation of the insulating substrate **63**. As a result, a load cannot be applied sufficiently on the terminal section **55**, and consequently, inadequate wire bonding tends to occur, which, in turn, may cause electrical connection failure between the semiconductor chip **52** and the terminal section **55**.

Meanwhile, as shown in FIG. **20**, the wiring substrate **67** which is provided with a wiring pattern only on one surface can avoid wire bonding problem mentioned above. That is, side B of the wiring substrate **67** does not have any wiring pattern, or any solder resist to protect wiring patterns, and thus the surface of side B is flat.

Therefore, since the wiring substrate **67** provided with the wiring pattern only on one surface has side B which is flat, the load applied on the terminal section **55** for wire bonding, while side B of the wiring substrate **67** placed on a stage of wire-bonder facing downward, does not cause deformation of the wiring substrate **67** since the load applied to the terminal section **55** can be held by sufficiently the stage.

However, in the case of the multi-layer wiring substrate **68** used in a semiconductor device shown in FIG. **22**, side B of the wiring substrate **68** also has the wiring pattern and the solder resist **57** thereon. In such case, side B comes to have protrudent parts depending on areas having or not having the wiring pattern or the solder resist **57** are formed or not formed.

When the insulating substrate **63** of the wiring substrate **68** is comparatively thick, or not less than 0.2 mm thick, the protrudent parts do not pose any problem. But when the substrate is less than 0.2 mm thick, particularly not more than 0.1 mm thick, stiffness of the insulating substrate **63** can becomes weak. It brings about the following problems in assembling the semiconductor device.

Specifically, after providing the semiconductor chip **52** on the insulating substrate **63** by die bonding, the semiconductor chip **52** and the terminal section **55** on the wiring substrate **68** are connected electrically by wire bonding.

Here, if the protrudent part is formed on side B, which is on the other side of the semiconductor chip **52** disposed on side A of the insulating substrate **63**, as shown in FIG. **23**, the insulating substrate **63** deforms in a direction of thickness when a load is applied on the terminal section **55** for wire bonding in an arrowhead direction (in a direction of thickness of the insulating substrate **63**) in wire bonding. Because of this, it was impossible conventionally to apply enough load in wire bonding, posing the problem of inadequate wire bonding which may cause electrical connection failure between the semiconductor chip **52** and the wiring substrate **68**.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a wiring substrate, a semiconductor device, and a package stack semiconductor device, all with improved reliability of connection by suppressing occurrence of inadequate electrical connection.

A wiring substrate of the present invention, in order to achieve the foregoing object, includes an insulating substrate, a terminal section for wire bonding or flip-chip connection and a support pattern, provided on a surface of the other side of the surface where the terminal section is provided, and on a position corresponding to the terminal section, for improving reliability of connection of wire bonding.

Therefore, this structure can suppress deformation of the insulating substrate by the support pattern, even when the terminal section is pressed in wire bonding or other connection methods. As a result, reliability of connection in wire bonding or other connection methods, can be improved than conventionally.

A semiconductor device of the present invention, in order to achieve the foregoing object, includes the wiring substrate. Therefore, this structure can provide a thinner semiconductor device with improved reliability of connection in wire bonding or flip-chip connection than conventionally.

A package stack semiconductor device of the present invention, in order to achieve the object mentioned above, comprises the foregoing semiconductor devices which are stacked to each other. Therefore, this structure ensures electrical connection between the semiconductor devices, even when they are stacked using external terminal connections which are provided on land sections which are exposed.

Other objects, characteristics and advantages of the present invention will become apparent from the detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross sectional view showing a wiring substrate and a semiconductor device using it in the first embodiment according to the present invention.

FIG. **2**(*a*) to FIG. **2**(*c*) are explanatory drawings concerning surfaces on the both sides of the wiring substrate, in which FIG. **2**(*a*) shows a layout on side A, and FIG. **2**(*b*) shows a layout on side B, and FIG. **2**(*c*) shows a modified example of the layout on side B.

FIG. **3**(*a*) to FIG. **3**(*c*) are explanatory drawings showing a wiring substrate and a semiconductor device using it in the second embodiment according to the present invention, in which FIG. **3**(*a*) is a cross sectional view, and FIG. **3**(*b*) is a top view, and FIG. **3**(*c*) is a bottom view.

FIG. **4**(*a*) to FIG. **4**(*c*) are explanatory drawings showing a wiring substrate and a semiconductor device using it in the third embodiment according to the present invention. FIG. **4**(*a*) is a cross sectional view, and FIG. **4**(*b*) is a top view, and FIG. **4**(*c*) is a bottom view.

FIG. **5**(*a*) to FIG. **5**(*e*) are a flow diagram which shows manufacturing steps of the semiconductor device.

FIG. **6** is a schematic cross sectional view showing a wiring substrate used in the semiconductor device.

FIG. **7**(*a*) and FIG. **7**(*b*) are explanatory drawings showing the wiring substrate mentioned above, in which FIG. **7**(*a*) is a top view, and FIG. **7**(*b*) is a bottom view.

FIG. **8** is an explanatory drawing showing a package stack semiconductor device according to the present invention.

FIG. **9** is an explanatory drawing showing how to manufacture the package stack semiconductor device.

FIG. **10**(*a*) and FIG. **10**(*b*) are explanatory drawings showing other examples of the package stack semiconductor device, in which FIG. **10**(*a*) is a schematic cross sectional view showing four stacked semiconductor devices, and FIG. **10**(*b*) is a schematic cross sectional view of the package

stack semiconductor device which fixing resin is injected between the semiconductor devices.

FIG. **11**(*a*) and FIG. **11**(*b*) are explanatory drawings showing layouts of chip selectors in each semiconductor device of the package stack semiconductor device, in which FIG. **11**(*a*) is a plan view of a main portion of the semiconductor device which shows wiring for selection in the semiconductor device, and FIG. **11**(*b*) is a plan view of a main portion of the semiconductor device which shows an example where terminal section has the chip selector function in the semiconductor device.

FIG. **12** is a schematic plan view showing another modified example of the wiring substrate.

FIG. **13** is a schematic plan view showing yet another modified example of the wiring substrate.

FIG. **14**(*a*) to FIG. **14**(C) are explanatory drawings showing another modified example of the package stack semiconductor device, in which FIG. **14**(*a*) is a front view, and FIG. **14**(*b*) is a side view, and FIG. **14**(*c*) is a plan view.

FIG. **15** is a plan view of a wiring substrate used in the package stack semiconductor device.

FIG. **16**(*a*) and FIG. **16**(*b*) are explanatory drawings showing yet another modified example of the wiring substrate, in which FIG. **16**(*a*) is a front view, and FIG. **16**(*b*) is a cross sectional view taken along both dotted lines and arrows of the FIG. **16**(*a*).

FIG. **17** is a cross sectional view of yet another modified example of the semiconductor device.

FIG. **18** is a cross sectional view of yet another modified example of the semiconductor device.

FIG. **19** is a cross sectional view of yet another modified example of the semiconductor device.

FIG. **20** is a cross sectional view of a conventional semiconductor device.

FIG. **21** is a cross sectional view of another conventional semiconductor device.

FIG. **22** is a cross sectional view of yet another conventional semiconductor device.

FIG. **23** is a cross sectional view of a main portion which shows deformation of an insulating substrate of the semiconductor device in wire bonding.

DESCRIPTION OF THE EMBODIMENTS

The following describes embodiments of the present invention with reference to FIG. **1** through FIG. **19**.

The First Embodiment

FIG. **1** is a cross sectional view of a semiconductor device in accordance with the first embodiment of the present invention. FIG. **2**(*a*) to FIG. **2**(*c*) are explanatory drawings showing a wiring substrate **1** used in the semiconductor device of the first embodiment in accordance with the present invention, in which FIG. **2**(*a*) shows a wiring pattern **4** of side A **13***a* of an insulating substrate **13**, and FIG. **2**(*b*) shows a wiring pattern **4'** of side B **13***b* of an insulating substrate **13**, FIG. **2**(*c*) shows a modification example of the wiring pattern **4'**.

The semiconductor device according to the first embodiment, as shown in FIG. **1**, has the wiring substrate **1**, a semiconductor chip **2**, Au wires (bonding wire section) **3**, a solder resist **7**, an external connection terminal **10**, and a resin sealing section **11**. Examples of the semiconductor chip **2** include a CPU (Central Processing Unit) and an integrated circuit (L.S.I:Large Scaled Integrated circuit) such as a memory.

The semiconductor chip **2** is mounted on the wiring substrate **1** by die bonding. The Au wires **3** are to electrically connect terminal sections **5** on the wiring substrate **1** to the semiconductor chip **2** by wire bonding. The resin sealing section **11** is to protect the semiconductor chip **2** and the Au wires **3** by covering them with a sealing resin by transfer molding.

The external connection terminal section (conductive member) **10** is provided in the form of solder balls by reflow soldering on land sections **6** (described later), which are formed on a surface (hereinbelow, referred to as side B **13***b*) on the other side of a surface on which the semiconductor chip **2** is provided (hereinbelow, referred to as side A **13***a*). The land section **6** is provided on side b **13***b*.

The wiring substrate **1**, as shown in FIG. **1**, FIG. **2**(*a*) and FIG. **2**(*b*), has the insulating substrate **13** made of, for example, a 0.06 mm thick glass epoxy material, and the plurality of conductive land sections **6** to connect the semiconductor chip **2** to the external device, are provided, as many as input/output terminals of the semiconductor chip **2**, on side B **13***b*, for example, in a matrix pattern.

Further, the wiring substrate **1** has the plurality of conductive terminal sections **5** made of, for example, Cu foil for wire bonding, which are to be electrically connected to terminals on the upper surface of the semiconductor chip **2** and provided side by side, as many as input/output terminals of the semiconductor chip **2**, on the periphery of the side A **13***a* on which the semiconductor chip **2** is mounted.

Further, on the side A **13***a* of the wiring substrate **1** is formed the wiring pattern **4**, made of conductive metallic foil, for example, such as Cu foil, to electrically connect the land sections **6** to the corresponding terminal sections **5**. Thus, in order to connect the ends of the wiring pattern **4** to the land sections **6** electrically, through hole sections **8** are provided through the insulating substrate **13** between the ends of the wiring pattern **4** and the land sections **6**, and connection sections **17** which are plated with silver, gold and the like, or are filled with a conductive paste are provided on the through hole section **8**.

Further, in the side B **13***b*, on the other side of the side A **13***a* of the wiring substrate **1**, the wiring pattern **4'** is provided to electrically connect the land sections **6**, which cannot be connected completely through the wiring pattern **4**, to the corresponding terminal sections **5**. The wiring pattern **4'** is made of conductive metallic foil such as Cu foil.

In order to connect this wiring pattern **4'** to the corresponding land sections **6** via the wiring pattern **4** on side A **13***a*, through hole sections **8***a* are provided according to the wiring pattern **4'**. The through hole sections **8***a* enable the wiring pattern **4** and the wiring pattern **4'** which lead to the through hole sections **8***a* to be connected electrically in accordance with an electrical conductor (not shown) such as a metal eyelet, for example, made of Cu, the plating mentioned above, or a conductive paste. Thus, the wiring pattern **4** of side A **13***a* includes a wiring pattern which connects the terminal sections **5** to the corresponding land sections **6** via the through hole sections **8**.

Further, on the side B **13***b* of the wiring substrate **1**, a support pattern **9** having almost the same, or preferably the same height as the wiring pattern **4'** or land sections **6** is provided on a position corresponding to or facing to the position where the terminal sections **5** are formed. The support pattern **9** is provided on substantially in the form of strips opposing each other on the sides of the side B **13***b* corresponding to the terminal sections **5**. Further, the support pattern **9** may be provided according to, or at the same height as, the height of the highest protrudent part on side B **13***b*.

The support pattern **9** is preferred to be made of the same material as the land sections **6** or the wiring pattern **4'**, because this makes it easy to produce them at once, and to match their heights, using the etching pattern for forming the terminal sections **5** on side A **13***a* when forming the wiring pattern **4'** by etching, etc.

In the wiring substrate **1**, a semiconductor chip **2** is mounted on side A **13***a* of the insulating substrate **13**, and the input/output terminals (not shown) on the circuit forming surface on the upper surface of the semiconductor chip **2** (the underside of the semiconductor chip **2** is connected to the insulating substrate **13** by die bonding) are respectively connected to the terminal sections **5** electrically via the Au wires **3** by wire bonding.

As a rule, wire bonding employs fixing on a stage of a wire bonder by suction, or fixing by the pressure of a clamper. If the wiring substrate **1** has enough stiffness, deformation of the wiring substrate **1** can be prevented when a load is applied on the wiring substrate **1** in wire bonding to make connection, even when there are irregularities such as the wiring pattern **4'** on side B **13***b* of the wiring substrate **1**, and fixing is not enough. This enables the electrical connection by wire bonding to be highly reliable.

On the other hand, as in the wiring substrate **1** mentioned in the first embodiment, when the insulating substrate **13** is as thin as, for example, 0.06 mm and the stiffness is not enough, the terminal sections **5** may be able to be fixed or supported sufficiently. In such a case, the insulating substrate **13** deforms in a direction of thickness when a load is applied on each terminal sections **5** on the insulating substrate **13** in a direction of thickness of the insulating substrate **13** in wire bonding. This brings about inadequate wire-bond connection due to failure in applying a load.

When the wiring pattern **4** is provided on only side A **13***a*, and when side B **13***b* is flat, the wiring substrate **1** like this can avoid inadequate wire bonding because it allows the insulating substrate **13** to be sufficiently fixed even when the insulating substrate **13** of the wiring substrate **1** is thin.

However, the wiring substrate **1** of the first embodiment is thin, and the wiring pattern **4'** and the like is formed on side B **13***b*. Thus, there are irregularities in height on side B **13***b*. Not the whole area of the wiring substrate **1** may be supported and fixed, but at least the side B **13***b* in position corresponding to the terminal sections **5** to be wire bonded needs to be fixed.

As such is the case, the wiring substrate **1** according to the present invention has the support pattern **9** which is provided on side B **13***b* corresponding in position to the terminal sections **5**, taking into consideration the height of other sections such as the wiring pattern **4'** on side B **13***b*. This allows the load to be supported on the support pattern **9** in wire bonding, thus preventing deformation of the wiring substrate **13** (elastic deformation or plastic deformation) when applying a load.

Therefore, the wiring substrate **1** allows a load to be accurately applied at a pre-set value, thereby ensuring electrical connection between the Au wires **3** and the terminal sections **5**.

Note that, in the wiring substrate **1**, the support pattern **9** which is formed on the side B **13***b* corresponding in position to the terminal sections **5** is provided so that the insulating substrate **13** can be supported on a wire bonder stage to prevent deformation of the insulating substrate **13** at the point of applied pressure. Thus, not only the dummy pattern but also the wiring pattern **4'** which is connected to the land sections **6** can be used as the support pattern **9**. Either as shown in FIG. **2**(*c*), the support pattern **9** may be divided into plural parts, for example, according to the layout of the terminal sections **5**.

The Second Embodiment

FIG. **3**(*a*) to FIG. **3**(*c*) are explanatory drawings showing a semiconductor device of the second embodiment in accordance with the present invention, in which FIG. **3**(*a*) is a cross sectional view, FIG. **3**(*b*) is a top view, and FIG. **3**(*c*) is a bottom view. In the semiconductor device of the second embodiment, as shown in FIG. **3**(*a*) to FIG. **3**(*c*), a semiconductor chip **2** and a wiring substrate **1** are connected electrically and fixed by each other, by connecting the semiconductor chip **2** in flip-chip with terminal sections **5'**, using, for example, an anisotropy conductive film **19**.

In this semiconductor device, external connection terminal sections **10** are provided by connecting solder balls by reflow soldering on land sections **6** of external connection terminals of the surface on which the semiconductor chip **2** is mounted, i.e., side A **13***a*. Thus, a wiring pattern **4** is provided on side A **13***a* so as to respectively connect the terminal sections **5'** to the land sections **6** electrically.

The wiring substrate **1** according to the second embodiment of the present invention has land sections **6'** for connecting semiconductor devices. The land sections **6'** are provided on side B **13***b* of an insulating substrate **13** which is made of a material, for example, such as glass epoxy with a thickness of not more than 0.1 mm, on a position facing land sections **6**. The land sections **6** and the land sections **6'** for connecting semiconductor devices are connected electrically through connection sections **17** of the through hole sections **8**. Therefore, the land sections **6'** and the land sections **6** facing each other are provided such that they have the same electrical signal.

The wiring substrate **1** a support pattern **9'**, similar to the support pattern **9** mentioned above, on side B **13***b* of the insulating substrate **13** on the other side of the area on which the semiconductor chip **2** is mounted in flip-chip, taking into consideration the height of the land sections **6'** for connecting semiconductor devices, so that pressure of flip-chip connection can be sufficiently applied to each point of connection between the semiconductor chip **2** and the terminal sections **5'** of the wiring substrate **1**. This ensures that the surface of the side B **13***b* is flat in connecting based on flip-chip.

In short, by the provision of the support pattern **9'**, electrical connection between the semiconductor chip **2** and each terminal section **5'** of the wiring substrate **1** is ensured.

The Third Embodiment

FIG. **4**(*a*) to FIG. **4**(*c*) are explanatory drawings showing a semiconductor device according to the third embodiment of the present invention, in which FIG. **4**(*a*) is a cross sectional view, FIG. **4**(*b*) is a top view, and FIG. (*c*) is a bottom view. The members which have the same functions as those described in the first and second embodiments are given the same reference numerals thereof are omitted as long as they are not needed.

In the semiconductor device of the third embodiment, as shown in FIG. **4**(*a*) to FIG. **4**(*c*), FIG. **6** and FIG. **7**(*a*) to FIG. **7**(*c*), a wiring substrate **1** having an opening section **13***c* in which a semiconductor chip **2** is mounted is connected to the semiconductor chip **2** via Au wires **3**, and the Au wires **3** and a circuit forming surface of the semiconductor chip **2** are sealed with a resin sealing section **11**, and external connection terminal sections **10** are mounted on the same surface as the resin-sealed surface.

A method of fabricating the semiconductor device of the third embodiment shown in FIG. **4**(*a*) to FIG. **4**(*b*) is described below, based on FIG. **5**(*a*) to FIG. **5**(*e*).

In the first place, the wiring substrate **1** is prepared by forming the opening section **13***c* of a substantially rectangular shape in substantially the middle of the insulating substrate **13** where the semiconductor chip **2** is to be mounted. A film **12** which has an adherent is pasted on the adherent to one surface of the wiring substrate **1** which has the opening section **13***c*.

Next, the semiconductor chip **2** is mounted on the film **12** in the opening section **13***c*. In mounting the semiconductor chip **2**, the surface of the semiconductor chip on the other side of the surface where input/output terminals are formed (hereinbelow referred to as a back surface) is pasted to the film **12** (see FIG. **5**(*a*)).

Thereafter, the semiconductor chip **2** is connected to the terminal sections **5** of the insulating substrate **13** electrically via the Au wires **3** by wire bonding (see FIG. **5**(*b*)), and the resin sealing section **11** is formed to seal over the circuit forming surface of the semiconductor chip **2** and the Au wires **3** (see FIG. **5**(*c*)).

Next, land sections **6** of an external connection terminals are soldered by reflow after printing a soldering paste thereon so as to form the external connection terminal sections **10** (see FIG. **5**(*d*)). Then, the wiring substrate **1** is divided into individual semiconductor devices at cutting grooves **13***d* using a dicing cutting device (see FIG. **5**(*e*)). Each divided semiconductor device is picked up and put on a tray.

More concrete description of production process is given below. FIG. **5**(*a*) to FIG. **5**(*e*) show manufacturing steps of the semiconductor device according to the third embodiment. FIG. **6** is a cross sectional view of the wiring substrate **1** having wiring on both surfaces, which is used for the foregoing semiconductor device. FIG. **7**(*a*) and FIG. **7**(*b*) show an example of wiring patterns **4** on the both surfaces.

The insulating substrate **13** of the wiring substrate **1** is made of a 0.06 mm to 0.1 mm thick epoxy which contains glass fibre cloth, has the opening section **13***c*, in which the semiconductor chip is mounted, is provided by boring by means of a rooter or a die.

The wiring substrate **1** is provided with wiring patterns **4** and **4'**, which are made of Cu, on both sides, and these corresponding wiring patterns **4** and **4'** are connected to each other by connection sections **17** of through hole sections **8**. Further, land sections **6**, which are external connection terminals, are provided on the surface of the insulating substrate **13** where the terminal sections **5** are formed, and land sections **6'** for connecting semiconductor devices are provided on the other side of the insulating substrate **13**.

Further, a support pattern **9**, similar to the foregoing support pattern **9**, is provided on the other side of the surface where the terminal sections **5** for wire bonding is formed, so as to improve wire bonding.

For example, the land sections **6** are disposed with 0.5 mm and the diameter of 0.2 mm to 0.3 mm. The through hole sections **8** may be provided just under the land sections **6** in a pad-on manner, or may be provided on a different position from the land sections **6** so as to make connection by the wiring pattern **4**. All the wiring except the land sections **6**, **6'** and terminal sections **5** for the wire bonding is covered with a solder resist **7** for protection. The finished wiring substrate **1** is about 0.1 mm to 0.2 mm thick.

The following describes a manufacturing process of the semiconductor device mentioned above based on FIG. **5**(*a*) to FIG. **5**(*e*). The film **12** to be a mount of the semiconductor chip **2** is pasted on the semiconductor chip mounting opening section **13***c* of the wiring substrate **1** having the wiring patterns **4** and **4'** on the both surfaces of the insulating substrate **13**, so that the semiconductor chip **2** is mounted on the film **12** in opening section **13***c*. Preferably, the film **12** has enough heat resistance with respect to the heat history of each assembling steps of the semiconductor device. Also, the film **12** preferably includes an adhesive component on one of its surfaces so that it can anchor the semiconductor chip **2** and can easily be pasted on the insulating substrate **13** (see FIG. **5**(*a*)).

Then, the wiring substrate **1** and the semiconductor chip **2** are connected by wire bonding, i.e., by the Au wires **3**. In order to provide a thin semiconductor device, extremely low loop wire bonding is employed. Wire bonding enables the semiconductor chip **2** and the wiring substrate **1** to be connected flexibly.

Employing other connection method such as flip-chip bonding or single point bonding requires redesigning of the wiring substrate **1** needs according to the type of the semiconductor chip **2**. However, with the use of wire bonding, redesigning of the wiring substrate **1** is not needed. Even when pad pitch of the semiconductor chip **2** is changed by chip shrink, or when a semiconductor chip **2** with a standardized terminal sequence of an element such as a memory is used (referred in FIG. **5**(*b*)).

Thereafter, the semiconductor chip **2** and the Au wires **3** are sealed with resin, so as to form the resin sealing section **11**. Only the circuit forming surface of the semiconductor chip **2** is sealed by transfer molding. The method of sealing is not just limited to transfer molding, and other methods such as wiring by potting or printing using a screen mask may be employed as well. (see FIG. **5**(*c*)).

The external connection terminal sections **10** are formed in the form of semi-spheres by reflow soldering after printing a solder paste on the land sections **6** which is on the same surface as the mold-sealed surface of the wiring substrate **1**. The external connection terminal sections **10** may be made with a solder ball instead of a solder paste by a ball mount method, in the same manner as the usual BGA (see FIG. **5**(*d*)).

After forming the external connection terminal sections **10**, a cutting grooves **13***d* are provided by dicing, so as to divide the semiconductor device into individual pieces (see FIG. **5**(*e*)). The method of dicing the semiconductor device is not just limited to dicing but it may be cut using a looter or a die. Alternatively, if slits are provided between semiconductor devices of the wiring substrate **1** in advance, the device can be effectively cut at the slits.

In the semiconductor device of the third embodiment, by setting the thickness of the external connection terminal sections 10 to about 0.1 mm to 0.15 mm, the semiconductor device can be manufactured with the thickness of about 0.2 mm to 0.3 mm.

The Fourth Embodiment

A stacked semiconductor device (hereinbelow referred to as a package stack semiconductor device) as the fourth embodiment according to the present invention is described below.

The semiconductor devices according to the first to third embodiments include the land sections **6** and the land sections **6'** for connecting semiconductor devices, which are provided on the both surfaces of the wiring substrate **1**. This allows the semiconductor devices to be connected electrically by stacking them, regardless of the size and the type of the semiconductor chip **2**, taking into consideration or, for example, by matching the external sizes of the semiconductor devices and the layout of the external connection termi-

nal sections **10**. Two or more semiconductor devices can be used as the one package stack semiconductor device this way.

The package stack semiconductor device includes stacked semiconductor devices as shown in FIG. **8**. On a semiconductor device $\mathbf{21}_1$ placed in the top position, semiconductor device $\mathbf{21}_2$ and $\mathbf{21}_3$ are stacked in this order, with the external connection terminal sections **10** facing upward (toward an installation opening) in a tray **14**. Thereafter, the semiconductor devices $\mathbf{21}_1$ to $\mathbf{21}_3$ are connected to each other by reflow soldering.

The package stack semiconductor device of this type may be used as a stacked semiconductor device as it is, or, after reflow soldering, fixing resin (mentioned below) may be injected into gaps between each semiconductor device, so as to bring about reliability of the semiconductor device.

If the position of each semiconductor device **21** in the package stack semiconductor device is decided in advance before assemblage, it is preferable that a usually employed Sn—Pb solder is used for the external connection terminal sections **10** of a semiconductor device $\mathbf{21}_N$ (N is the number of stacked semiconductor devices) which is placed in the bottom position (i.e., a semiconductor device having the external connection terminal sections **10** which are exposed for extend connection), and a solder having a higher melting point than that of the Sn—Pb solder is used for the semiconductor devices $\mathbf{21}_1$ to $\mathbf{21}_{N-1}$ above the semiconductor device $\mathbf{21}_N$.

In short, the reflow soldering for electrically connecting the stacked semiconductor devices **21** are carried out under temperature conditions according to the solder having a higher melting point, and the reflow soldering of the substrate mounted on the semiconductor device $\mathbf{21}_N$ is carried out under normal conditions. As a result, this method of soldering can minimize melting and bleed of solder when connecting the semiconductor device $\mathbf{21}_1$ to $\mathbf{21}_{N-1}$.

As shown in FIG. **9**, the semiconductor device **21** may be stacked in the form of a collection of semiconductor devices **22** in a frame before being divided into individual pieces. These stacked semiconductor devices may be cut according to the sectional lines shown in FIG. **9**, or, alternatively, gaps between each semiconductor device may be filled with fixing resin, so as to eliminate gaps between the semiconductor devices **21** where they are cut, thus cutting the semiconductor devices more stably and effectively.

FIG. **10**(*a*) shows a cross sectional view of a package stack semiconductor device which is made up of four of the semiconductor devices **21** mentioned above. FIG. **10**(*b*) is a cross sectional view of a form injected with the fixing resin **15**.

In the case where semiconductor devices which have the same type of semiconductor chip **2** are stacked, by setting the external connection terminal sections **10** at the same position between the semiconductor devices **21**, except terminals for chip selection. The signals of the semiconductor devices **21** of the upper stages can be conveyed to an external substrate via the land sections **6'** of the semiconductor devices **21** of the lower stage.

Preferably, each semiconductor device **21** should be provided with terminals for chip selection in order to be identified when used in a package stack semiconductor device.

If the number of the chip selector terminals in the wiring substrate **1** is the same as or more than the number of stacked semiconductor devices **21**, it is possible to stack semiconductor devices **21** manufactured with the same wiring substrate **1** only by changing wire connection. FIG. **11**(*b*) shows an example of four stacked semiconductor devices (for convenience, the lowest semiconductor devices is called "the first" and the second lowest "the second" and the like).

When the semiconductor devices **21** stacked in a package stack have the same type of the semiconductor chip **2**, redesigning of the substrate of each semiconductor device will not be required, and the position of stacking can be changed only by changing a wire bonding position.

If the semiconductor chip **2** and the wiring substrate **1** are connected electrically by a method other than wire bonding, such as the flip-chip connection or inner lead bonding, the connection terminals cannot be changed using the same wiring substrate **1** as in wire bonding.

While, as shown in FIG. **11**(*a*), by providing and setting wiring **23** near the terminal sections **5** for connecting the chip selector terminals on the side of the wiring substrate **1**, a package stack position can be set by providing a cut-out section or a through hole section in the wiring substrate **1** of each semiconductor device **21** and by disconnecting the wiring **23**.

A terminal section **5**A in the figure is wire bonded and the wiring **23** at point C is disconnected when the semiconductor device **21** is used as a tip selector A. On the other hand, the terminal section **5**A is connected and the wiring is disconnected at point D when the semiconductor device **21** is used as a tip selector B.

So, even when the semiconductor devices **21** which have the same type of semiconductor chip **2** and the wiring substrate **1** are stacked, it is possible to identify each semiconductor device **21** in terms of electricity and appearance. The cut-out section or the through hole section may be provided on the wiring substrate **1** while the wiring substrate **1** is being processed, or while the semiconductor device **21** is being divided, or after the semiconductor device **21** is divided.

The wiring substrate **1** like this enables the chips to be identified with fewer terminals than the number of stacked semiconductor devices **21**. Thus, the number of the terminal sections **5** for wire bonding can be decreased. Different appearance of the semiconductor devices **21** also makes it easy to identify the chips.

Where there exist chips which are greatly different in size but having a similar terminal layout, the wiring substrate **1** as shown in FIG. **12** is used and the size of the opening section **13***c* where the chip is mounted is changed. This makes it possible to increase the type of the semiconductor chip **2** which can be adapted to the same wiring substrate **1**, without requiring redesigning of the substrate.

When the size of the semiconductor chip **2** is small, a square surrounded by a solid line in the figure is cut out as the opening section **13***c* and inner terminal sections **5** are used for wire bonding. When the size of the semiconductor chip **2** is large, a square surrounded by a broken line (larger than the square surrounded by solid line) is cut out as the opening section **13***c* and outer terminal sections **5** are used.

As shown in FIG. **13**, one or more reinforcing terminals (reinforcing projection) **16** are provided on the periphery of the wiring substrate **1** where the land sections **6** are not provided. The reinforcing terminals **16** are according to the size (height) which is set for the connection sections of the external connection terminal sections **10** on the land sections **6**, or preferably at the same height as the external connection terminal sections **10**. By this, reliability of connection between each stacked semiconductor device **21** or between the semiconductor device **21** and the mounting substrate can be further improved.

FIG. **14**(*a*) to FIG. **14**(*c*) show a different pattern of stack as in the case of a semiconductor chip **2** for a logic circuit and a semiconductor chip **2** for a memory circuit, wherein the number of the external connection terminal sections **10** differ greatly and the external size of the chip is different as well. FIG. **14**(*a*) is a front view, FIG. **14**(*b*) is a side view, and FIG. **14**(*c*) is a top view. Each figure is a description of the stack mentioned above.

When the semiconductor chip **2** having different terminal layout or different numbers of terminals are stacked as in the combination of the semiconductor chip **2** for a logic circuit and the semiconductor chip **2** for a memory circuit, for example, the wiring substrate **1** as shown in FIG. **7**(*a*) and FIG. **7**(*b*) and a wiring substrate **1** which is larger than the one mentioned above, as shown in FIG. **16**(*a*) and FIG. **16**(*b*) are used together.

Incidentally, the semiconductor chip **2** for a logic circuit has more external connection terminal sections **10** than the semiconductor chip **2** for a memory circuit. Thus, in the semiconductor device which has the semiconductor chip **2** mentioned above, the wiring substrate **1** is provided with the external connection terminal sections **10** on every side of the surface as shown in FIG. **15**. The external connection terminal sections **10** on two of four sides are used only for the logic circuit, and the external connection terminal sections **10** on the other two sides are used for both memory circuit and the logic circuit or used only for the memory circuit.

As shown in FIG. **14**(*a*) to FIG. **14**(*c*), the package stack semiconductor device has a stack structure of a semiconductor device $\mathbf{21}_4$ of the wiring substrate **1** which has the semiconductor chip **2** for the logic circuit placed on the lowest position, and semiconductor device $\mathbf{21}_1$ to $\mathbf{21}_3$ which have the semiconductor chip **2** for the memory circuit provided above the semiconductor device $\mathbf{21}_4$. Thus, the external connection terminal sections **10** of the wiring substrate **1** for the memory circuit are connected to the external mounting substrate via the wiring substrate **1** for the logic circuit.

Another method of fabricating the semiconductor device according to the present invention is described below. After providing the opening section **13***c* where the semiconductor chip is mounted, opening section **13***c* on one side (on side B **13***b*) is covered with the same Cu foil (metallic foil) as the foil used in providing the wiring pattern **4**. FIG. **16**(*b*) shows a cross sectional view of this wiring substrate **1**. The Cu foil **20** is used instead of the film **12** mentioned above. The Cu foil **20** is also provided on the other side of the terminal sections **5** for wire bonding, so as to improve wire bonding.

A process of fabricating the wiring substrate **1** which has the Cu foil **20** is described below. In the first place, the semiconductor chip **2** is mounted on the Cu foil **20** of the opening section **13***c*, and after connecting the semiconductor chip **2** and the terminal sections **5** of the wiring substrate **1** via the Au wires **3** by the wire bonding, the circuit forming surface of the semiconductor chip **2** and the Au wires **3** are sealed with resin. Thereafter, the external connection terminal sections **10** are provided on the land sections **6** making up the external connection terminals.

After that, the wiring substrate **1** in the form of a frame is pasted to a film for dicing connection and is cut into pieces. The Cu foil **20** remains on the back of the semiconductor chip **2** of the semiconductor device which was divided by dicing. The Cu foil **20** not only has the advantage of not requiring the film **12** in assemblage of the semiconductor device, but also has the effect of protecting the back of the semiconductor chip **2**, among other effects such as shielding electromagnetic wave and releasing heat.

Yet another method of fabricating the semiconductor device according to the present invention is described below. A wire bonder equipped with a chip supply device is used in this method, which is described more concretely below, based on FIG. **5**(*a*) to FIG. **5**(*e*).

In the first place, with respect to the wiring substrate **1** which is fixed on a stage section of the wire bonder, the semiconductor chip **2** is supplied to a portion of the stage which is exposed through the opening section **13***c* where the semiconductor chip is to be mounted, and wire bonding is carried out after fixing the semiconductor chip **2** on the stage by vacuum suction. Since the semiconductor chip **2** used in the semiconductor device mentioned above is thin (150 μm or less), it can be held by only the Au wires **3** until they are sealed with resin after wire bonding.

In the first through fourth embodiments, the glass epoxy was used as a material of the wiring substrate **1**. However, not only the glass epoxy but also resin such as polyimide, BT (bismaleimide•etriazine) resin, and aramid can be used.

The Fifth Embodiment

FIG. **17** is a cross sectional view of a semiconductor device according to the fifth embodiment of the present invention. The semiconductor device of the present invention has a structure including two semiconductor chip **2***a* and **2***b* in the semiconductor device of the third embodiment. Each semiconductor chip **2***a* and **2***b* used in the semiconductor device is thinner than the semiconductor chip **2** used in the semiconductor device of the third embodiment.

In the semiconductor device according to the fifth embodiment, the first semiconductor chip **2***a* is provided on the film **12** as in the third embodiment, and the second semiconductor chip **2***b* having a film of a heat bonding type pasted on the back surface is die bonded with the circuit forming surface of the first semiconductor chip **2***a*. Thereafter, each semiconductor chip **2***a* and **2***b* is connected to the wiring substrate **1** via Au wires **3** by wire bonding. Then, they are sealed with resin, and external connection terminal section **10** is provided, and the semiconductor device is cut into pieces.

The second semiconductor chip **2***b* may wire bonded with the wiring substrate **1** directly, or may be electrically connected to the wiring substrate **1** via the first semiconductor chip **2***a* wire bonded with the second semiconductor chip **2***b*. The number of stacked semiconductor chips is not just limited to two stages but they can be stacked in the same manner in three or more stages.

Further, as shown in FIG. **18**, instead of laminating the semiconductor chips **2**, they may be placed side by side on the same plane two-dimensionally. Further, as shown in FIG. **19**, additional semiconductor chips **2***a* and **2***b* may be stacked in a direction of thickness with respect to the semiconductor chips **2***a* and **2***c* which are placed side by side on the same plane. Further, in the wiring substrate **1** of the present invention, the number of layers of the wiring pattern **4** is not just limited to two, but the wiring substrate **1** may have a larger number of layers.

As described, a wiring substrate of the present invention, includes an insulating substrate, a terminal section, provided on a first surface of the insulating substrate by wire bonding; a land section, provided on the insulating substrate, for an external connection terminal; wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section; and

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding.

Another wiring substrate of the present invention, as described above, includes an insulating substrate, a terminal section provided on a first surface of the insulating substrate, for making connection by wire bonding; a first land section provided on the first surface for an external connection terminal; a second land section provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices; wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land; and a support pattern provided on the second surface corresponding in position to the terminal section for improving wire bonding.

Yet another wiring substrate of the present invention, as described above, includes an insulating substrate, a terminal section, provided on a first surface of the insulating substrate, for making flip-chip connection; a first land section, provided on the first surface, for an external connection terminal; a second land section, provided on the second surface on the other side of the first surface, for interconnecting semiconductor devices; wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section; a support pattern, provided on the second surface corresponding in position to the terminal section, for improving reliability of connection.

Yet another wiring substrate of the present invention, as described above, includes an insulating substrate having an opening section for mounting a semiconductor chip in the middle of the insulating substrate; a terminal section, provided on the first surface of the insulating substrate, for connecting to a semiconductor chip by wire bonding; a first land section, provided on the first surface, for an external connection terminal; a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices; wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section; a support pattern, provided on the second surface corresponding in position to the terminal section for improving wire bonding.

According to the arrangements mentioned above, the wiring patterns for making electrical connection between the terminal section and the first and second land sections are provided on the first and second surface, respectively. Thus, the wiring patterns ensure to connect the terminal section and the first and second land sections, even when the semiconductor chip which has many input/output terminals is mounted.

Further, with the foregoing arrangements, when the terminal section is connected by wire bonding or by flip-chip, even when a load is applied on the terminal section in a direction of thickness of the insulating substrate, the support pattern provided on a position corresponding to the terminal section can hold the pressure.

Therefore, with the foregoing arrangement, the support pattern can avoid deformation of the insulating substrate mentioned above. Thus, a load can be applied to the insulating substrate sufficiently in wire bonding and in flip-chip connecting. As a result, reliability of the connection based on wire bonding and flip-chip can be improved.

The wiring substrate which has the opening section may be provided with a heat resistant film for mounting a semiconductor chip, provided so as to cover an opening of the opening section on the second surface. The film makes it easier to provide the opening section with the semiconductor chip.

The wiring substrate which has the opening section may be provided with a metallic foil for mounting the semiconductor chip, provided so as to cover an opening of the opening section on the second surface.

With this arrangement, the metallic foil makes it easier to provide the opening section with the semiconductor chip. Besides, the metallic foil can protect the backside of the semiconductor chip, and can shield electromagnetic wave, and can improve radiating heat.

Preferably, the shape of the support pattern corresponds to the shape of the terminal section in the wiring substrate mentioned above. According to this arrangement, it is further ensured that deformation of the insulating substrate by the support pattern can be avoided in making connection based on wire bonding or flip-chip connection.

In the wiring substrate mentioned above, the support pattern may be connected to the second land section. According to this arrangement, the support pattern can be used as one of the wiring patterns. This simplifies manufacture of the wiring substrate.

The wiring substrate mentioned above may have the wiring patterns in multi-layers. With this arrangement, by the multi-layered wiring pattern, for example, connection among the terminal section, the first land section, and the second land section can be ensured by the wiring patterns, even when the number of input/output terminals of the semiconductor chip is increased.

Preferably, the support pattern is provided according to the height of the wiring pattern on the second surface in the insulating substrate mentioned above. With this arrangement, the support pattern can support the insulating substrate more securely in making connection based on wire bonding and flip-chip connection. As a result, reliability of connection based on wire bonding and flip-chip connection can be improved further.

As described, a semiconductor device of the present invention includes any one of the wiring substrates having the terminal section connected by wire bonding, a semiconductor chip mounted on the wiring substrate, a bonding wire section for making electrical connection between the wiring substrate and the semiconductor chip, a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section, and a conductive member provided on the second land section for connecting the semiconductor chip to outside.

According to the arrangement mentioned above, by the provision of the wiring substrate having the support pattern on a position corresponding to the terminal section, reliability of connection based on wire bonding by the bonding wire section can be improved, thereby improving reliability of the device.

Yet another semiconductor device of the present invention, as described above, includes any one of the wiring substrate for flip-chip connection, a semiconductor chip which is mounted on the wiring substrate by being electrically connected thereto by flip-chip connection, a resin sealing section for sealing the circuit forming surface of the semiconductor chip, and a conductive member, provided on the second land section, for connecting the semiconductor chip to outside.

According to the arrangement mentioned above, by the provision of the wiring substrate having a support pattern on a position corresponding to the terminal section, reliability of connection based on flip-chip connection can be improved, thereby improving reliability of the device.

In the semiconductor device mentioned above, a plurality of semiconductor chips may be provided two dimensionally or three dimensionally. With this arrangement, the wiring patterns are provided respectively on the both surfaces of the insulating substrate. Thus, even when the number of the input/output terminals is increased due to the plurality of the semiconductor chips, it is easy to cope with the increased input/output terminals, and connect the semiconductor chips to the external device, and reliability of electrical connection between the semiconductor chip and outside can be improved.

In the semiconductor device mentioned above, a support projection which corresponds to the external connection terminal may be provided on the wiring substrate.

According to the arrangement mentioned above, when a plurality of semiconductor devices are stacked in a direction of thickness of the wiring substrate, and when the adjoining semiconductor devices are connected by the external connection terminals, the support projection enables the electrical connection of the semiconductor devices to be maintained. As a result, reliability of connection of the semiconductor devices can be improved.

The package stack semiconductor device of the present invention, as described above, has a plurality of semiconductor devices which are stacked by soldering connection.

According to the arrangement mentioned above, a plurality of semiconductor devices are stacked, for example, in a direction of thickness of the wiring substrate, and the external connection terminal sections as the conductive member of the respective semiconductor devices are connected by soldering to each other, thus connecting the semiconductor devices in a stacked form.

Further, since the foregoing arrangement uses the semiconductor device having the wiring substrate with the improved reliability of wire bond connection, reliability of connection can be improved.

In the foregoing package stack semiconductor device, it is preferable that a solder used for an external connection terminal of a semiconductor device which is exposed to outside has a lower melting point than that used for external connection terminals of stacked semiconductor devices to each other.

According to the arrangement mentioned above, the electrical connection between the stacked semiconductor devices can be carried out by reflow soldering at a melting point according to the solder of the electrical connection terminals of the other semiconductor devices.

While, according to the foregoing arrangement, when the exposed external connection terminals of the semiconductor device which are exposed to outside are to be electrically connected, for example, to the external mounting substrate (external device), they can be soldered at lower melting point than terminals of other semiconductor devices. Thus, this can prevent melting of solder between other stacked semiconductor devices, and can connect them electrically.

In the package stack semiconductor device mentioned above, fixing resin may be injected into gaps between adjoining semiconductor devices. With this arrangement, fixing resin prevents deformation and vibration of each semiconductor device, thus further improving reliability of connection.

In the foregoing package stack semiconductor device, it is preferable that the layout of the external connection terminals of each semiconductor device, at least the common external connection terminals, are designed according to the position of each terminal.

According to this arrangement, at least common external connection terminals are set, taking into consideration their positions. This further ensures electrical connection between stacked semiconductor devices, in addition to making manufacture of the device easier.

In the foregoing package stack semiconductor device, at least two of the plurality of semiconductor devices have different external size.

According to this arrangement, the semiconductor chip for the logic circuit which has more input/output terminals can be provided on a semiconductor device having a larger external size, and the semiconductor chip for the memory circuit which has fewer input/output terminals can be provided on a semiconductor device having a smaller external size.

It is preferable in the foregoing package stack semiconductor device that a semiconductor device with its external connection terminal exposed to outside is a larger external size than that of other semiconductor devices.

In the arrangement mentioned above, the semiconductor chip for the logic circuit which has more input/output terminals can be provided on the semiconductor device whose external connection terminals are exposed to outside, and the semiconductor chip for the memory circuit which has fewer input/output terminals can be provided on other semiconductor devices.

With this arrangement, a semiconductor device having a larger external size, which can have many terminals, can be exposed to outside, thus ensuring electrical connection between the stacked semiconductor devices and outside.

The invention may be embodied in other specific forms without departing from the spirit or the appended claims thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive.

What is claimed is:

1. A wiring substrate comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;

a land section, provided on the insulating substrate, for an external connection terminal;

wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section; and

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land section.

2. The wiring substrate as set forth in claim **1**, wherein a shape of the support pattern corresponds to a shape of the terminal section.

3. The wiring substrate as set forth in claim **1**, wherein the support pattern is connected to the land section.

4. The wiring substrate as set forth in claim **1**, wherein the wiring patterns are provided in multi/layers.

5. The wiring substrate as set forth in claim **1**, wherein the support pattern is provided according to a height of the

wiring pattern on the second surface of the insulating substrate on the second surface.

6. A wiring substrate comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section; and

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections.

7. A wiring substrate comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making flip-chip connection;

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for electrical connection between the terminal section, the first land section, and the second land section; and

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving reliability of connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections.

8. A wiring substrate comprising:

an insulating substrate having an opening section for mounting a semiconductor chip in the middle of said insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for connecting to the semiconductor chip by wire bonding:

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section for interconnecting semiconductor devices; and

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections.

9. The wiring substrate as set forth in claim **8**, wherein a heat resistant film for mounting the semiconductor chip is provided so as to cover an opening of an opening section on the second surface.

10. The wiring substrate as set forth in claim **8**, wherein a metallic foil for mounting the semiconductor chip is provided so as to cover an opening of the opening section on the second surface.

11. A semiconductor device comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;

a land section, provided on the insulating substrate, for an external connection terminal;

wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section;

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and land section;

a semiconductor chip mounted on the insulating substrate;

a bonding wire section for making electrical connection between the terminal section and the semiconductor chip;

a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section; and

a conductive member, provided on the land section, for connecting the semiconductor chip to outside.

12. The semiconductor device as set forth in claim **11**, wherein said semiconductor chip is provided in plurality on the insulating substrate two-dimensionally or three dimensionally.

13. A semiconductor device comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section;

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections;

a semiconductor chip mounted on the insulating substrate;

a bonding wire section for making electrical connecting between the terminal section and the semiconductor chip;

a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section; and

a conductive member, provided on the second land section, for connecting the semiconductor chip to outside.

14. A semiconductor device comprising:

an insulating substrate having an opening section in the middle of the insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for connecting by wire bonding;

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section;

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections;

a semiconductor chip mounted in the opening section;

a bonding wire section for making electrical connection between the terminal section and the semiconductor chip;

a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section; and

a conductive member, provided on the second land section, for connecting the semiconductor chip to outside.

15. The semiconductor device as set forth in claim **14**, further comprising a heat resistant film for mounting the semiconductor chip which covers a second-surface opening of the opening section.

16. The semiconductor device as set forth in claim **14**, further comprising a metallic foil for mounting the semiconductor chip, which is provided so as to cover an opening of the opening section on the second surface.

17. The semiconductor device set forth in claim **14**, further comprising a support projection, provided on the insulating substrate, corresponding to the external connection terminal.

18. A semiconductor device comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making flip-chip connection;

a first land section, provided on the first surface, for an external connection terminal;

a second land section, provided on a second surface on the other side of the first surface, for interconnecting semiconductor devices;

wiring patterns, respectively provided on the first surface and the second surface, for making electrical connection between the terminal section, the first land section, and the second land section;

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving reliability of connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land sections;

a semiconductor chip connected to the terminal section electrically by flip-chip connection;

a resin sealing section for sealing a circuit forming surface of the semiconductor chip; and

a conductive member, provided on the second land section, for connecting the semiconductor chip to outside.

19. The semiconductor device as set forth in claim **18**, wherein said semiconductor chip is provided in plurality on the insulating substrate two dimensionally or three dimensionally.

20. A package stack semiconductor device which includes a plurality of semiconductor devices, which are stacked by soldering,

each of semiconductor device, comprising:

an insulating substrate;

a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;

a land section, provided on the insulating substrate, for an external connection terminal;

wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section;

a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and land section;

a semiconductor chip mounted on the insulating substrate;

a bonding wire section for making electrical connection between the terminal section and the semiconductor chip;

a resin sealing section for sealing a circuit forming surface of the semiconductor chip and the bonding wire section; and

a conductive member, provided on the land section, for connecting the semiconductor chip to outside.

21. The package stack semiconductor device as set forth in claim **20**, wherein a solder used for an external connection terminal of a semiconductor device which is exposed to outside has a lower melting point than that used for external connection terminals of other semiconductor devices.

22. The package stack semiconductor device as set forth in claim **20**, wherein fixing resin is injected to gaps between adjoining semiconductor devices.

23. The package stack semiconductor device as set forth in claim **20**, wherein external connection terminals of respective semiconductor devices are positioned, taking into consideration their positions, at least for those external terminals which are common among the semiconductor devices.

24. The package stack semiconductor device as set forth in claim **20**, wherein at least two of said plurality of semiconductor devices have different external size.

25. The package stack semiconductor device as set forth in claim **24**, wherein a semiconductor device with its external connection terminal exposed to outside has a larger external size than that of other semiconductor devices.

* * * * *

CERTIFICATE OF SERVICE

I hereby certify that, on February 22, 2024, all counsel of record were served with a true and correct copy of the foregoing CORRECTED OPENING BRIEF OF APPELLANTS KATANA SILICON TECHNOLOGIES LLC and LONGHORN IP, LLC through the Court's electronic filing system.

/s/ Scott W. Breedlove
Scott W. Breedlove

CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B)(i), as modified by Federal Circuit Rule 32(b)(1).

The brief contains 13,143 words, excluding the parts of the brief exempted by Federal Rule of Appellate Procedure 32(f) and Federal Circuit Rule 32(b)(2).

2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6). The brief has been prepared in a proportionally spaced typeface using Microsoft Word for Mac version 16.81 in a 14-point Times New Roman font.

/s/ Scott W. Breedlove
Scott W. Breedlove