No. 2022-1906

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VLSI TECHNOLOGY LLC,

Plaintiff-Appellee,

v.

INTEL CORPORATION,

Defendant-Appellant.

On Appeal from the United States District Court for the Western District of Texas in Case No. 6:21-cv-00057-ADA, Judge Alan D. Albright

DEFENDANT-APPELLANT INTEL CORPORATION'S COMBINED PETITION FOR PANEL REHEARING AND REHEARING EN BANC

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February 2, 2024

CERTIFICATE OF INTEREST

Counsel for Defendant-Appellant Intel Corporation certifies the following:

1. Represented Entities. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

Intel Corporation.

2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

None.

3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

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5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

[X] Yes (file separate notice; see below) [ ] No [ ] N/A (amicus/movant)

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). Please do not duplicate information. This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

Filed previously.

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None.

Dated: February 2, 2024

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STATEMENT OF COUNSEL

Based on my professional judgment, I believe the panel decision is contrary to the following precedent of this Court: *Wisconsin Alumni Research Foundation v. Apple Inc.*, 905 F.3d 1341 (Fed. Cir. 2018), which held that "[g]iving a [claim] term its plain and ordinary meaning does not leave the term devoid of any meaning whatsoever." *Id.* at 1348.

/s/ William F. Lee
WILLIAM F. LEE

POINTS OVERLOOKED OR MISAPPREHENDED BY THE PANEL

The panel misapprehended or overlooked the following points of law or fact:

1. The panel affirmed the literal-infringement judgment for the '373 patent because it concluded that the jury could have reasonably found that the voltage source for the C6SRAM memory in Intel's products "switches ***at the time that*** VCCR voltage drops below the minimum for C6 SRAM's data retention—RING_RETENTION_VOLTAGE." Op. 13 (emphasis added). In so ruling, however, the panel overlooked the undisputed evidence demonstrating that Intel's C6SRAM voltage source switches ***before*** the VCCR voltage drops below RING_RETENTION_VOLTAGE. As explained in Intel's panel briefing and below, this timing distinction means that Intel's products cannot literally satisfy the "when" claim limitations—including under the panel's understanding of the claim

language's plain meaning—and therefore cannot infringe. *See* Blue Br. 35; Gray Br. 4; *infra* pp. 12-14.

2. The panel also misapprehended Intel's non-infringement argument with respect to the "when" claim limitations. The panel stated that "Intel's argument turns entirely on its contention that the claims require that falling below the minimum operating voltage be the ***causal trigger*** for switching from one voltage source to a different one." Op. 12 (emphasis added). But Intel never made that argument. Instead, Intel merely contended that—consistent with the plain meaning of the "when" limitations—the claimed "minimum operating voltage" must be involved somehow in determining which voltage to provide to the memory. *See* Blue Br. 33-36; Gray Br. 2-5; Oral Arg. 10:20-10:30. As explained below, the panel's misapprehension of Intel's argument prevented it from fully or correctly analyzing the non-infringement issue for the "when" limitations. *See infra* pp. 14-16.

INTRODUCTION

The panel's opinion in this appeal addressed multiple issues involving two patents asserted against Intel Corporation ("Intel") in the Western District of Texas. Intel seeks rehearing with respect to only the portion of the panel's decision that affirmed the infringement judgment for U.S. Patent No. 7,523,373 ("the '373 patent").

Panel rehearing is warranted because the panel made two errors in concluding that the jury could have reasonably found that Intel's products literally satisfy the "when" claim limitations. First, the panel overlooked ***undisputed*** evidence concerning the sequence of events that occurs in Intel's accused products. This evidence conclusively demonstrated that Intel's products switch the voltage source supplied to the accused memory ***before*** the VCCR voltage level drops below the alleged "minimum operating voltage," rather than ***"at the time that"*** the voltage drop occurs as the panel found, Op. 12-13 (emphasis added). This difference in timing means that Intel's products cannot literally satisfy the "when" claim limitations.

Second, the panel misapprehended Intel's non-infringement argument. The panel's analysis started from the premise that Intel was making a claim construction argument it had not presented to the district court—namely, "that the claims require that falling below the minimum operating voltage be the ***causal trigger*** for switching from one voltage source to a different one." Op. 12 (emphasis added). But Intel

never made that argument. Instead, consistent with the plain claim language, Intel contended that the claimed "minimum operating voltage" must merely be involved in some way in determining which voltage to provide to the memory. The panel's misapprehension of Intel's argument prevented it from fully or correctly analyzing the non-infringement issue for the "when" limitations.

Alternatively, en banc rehearing is warranted because the panel's decision violates the rule that "[g]iving a [claim] term its plain and ordinary meaning does not leave the term devoid of any meaning whatsoever." *Wisconsin Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1348 (Fed. Cir. 2018) ("*WARF*"). In concluding that the jury could have reasonably found literal infringement, the panel narrowly focused on a single word in the claims (i.e., "when") instead of comparing the accused products to the specific conditions established by the "when" limitations as a whole (i.e., that a first voltage is provided to the memory "when" that first voltage is "at least" the memory's "minimum operating voltage," and that a second voltage is provided "when" the first voltage is "below" the "minimum operating voltage"). A proper reading of the "when" claim limitations in their entirety, which gives meaning to every word, makes clear that Intel's products do not follow the exact conditions claimed in the patent—and that there can be no literal infringement.

BACKGROUND

VLSI Technology LLC ("VLSI") was formed in 2016 by Fortress Investment Group LLC, a New York-based hedge fund represented by VLSI's counsel. Appx3860; Appx4061; Appx4952-4953. Three days after its formation, VLSI began acquiring patents from NXP Semiconductors ("NXP"). Appx3981-3983. Over the next few years, VLSI purchased more than 170 NXP patents. Appx13952-14079; Appx1729-1739. To date, VLSI's only business has been asserting nearly two dozen former NXP patents against Intel across multiple jurisdictions—though nearly all of VLSI's asserted patents have now been found invalid and/or not infringed or have been dismissed from VLSI's lawsuits. This petition relates to VLSI's assertion of the '373 patent against Intel in the Western District of Texas.

A. The '373 Patent

The '373 patent is titled "Minimum Memory Operating Voltage Technique" and relates to a technique for selecting a power supply voltage for a memory. Appx101; Appx105(1:6-9). A memory is an electronic component that stores data, and it must be provided with a power supply voltage to operate. Appx1383; Appx1914-1916. A "minimum operating voltage" is the lowest voltage at which the memory can reliably operate (e.g., write, read, or retain data). Appx1403; Appx1917-1920; Appx2730-2731.

The '373 patent describes a specific technique intended to ensure that the voltage supplied to a memory does not fall below the memory's "minimum operating voltage." Appx101 (abstract). The claimed approach involves first determining the memory's "minimum operating voltage" and storing that value. *Id.* As the patent's abstract explains, "[t]his minimum operating voltage information can then be used in determining when an alternative power supply voltage may be switched to the memory[.]" *Id.*; *see also* Appx106(3:30-44, 3:54-4:7).

More specifically, the claims specify which of two voltages to supply to the memory depending on whether the first voltage is above or below the memory's "minimum operating voltage." Appx111(13:7-28, 13:59-14:15). When the first voltage is "at least" the value of the memory's minimum operating voltage, that first voltage is provided to the memory. Appx111(13:20-22, 14:8-11). Conversely, when the first voltage is "less than" or "below" the memory's minimum operating voltage, a second voltage (which is greater than the first voltage) is instead provided to the memory. Appx111(13:23-25, 14:11-13).

VLSI asserted claims 1, 5, 6, 9, and 11. Representative claim 1 provides:

1. A method, comprising:

providing an integrated circuit with a memory;

operating the memory with an operating voltage;

determining a value of a minimum operating voltage of the memory;

providing a non-volatile memory (NVM) location;

storing the value of the minimum operating voltage of the memory in the NVM location;

providing a functional circuit on the integrated circuit exclusive of the memory;

providing a first regulated voltage to the functional circuit;

providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;

providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and

providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

Appx111(13:7-28) (emphases added).

Independent claim 9 is similar. It recites a "power supply selector" that supplies either a "first regulated voltage" or a "second regulated voltage" to the memory based on the same relationship between the first regulated voltage and the memory's "minimum operating voltage" as in claim 1. Appx111(13:59-14:15).

B. Intel's Accused Products

VLSI accused certain Intel microprocessors of infringing the '373 patent. Appx1447. A microprocessor is like the "brain" of a computer system and may be used, for example, in a desktop or laptop computer. Appx1913. Each Intel

microprocessor chip includes multiple processor cores, which perform computations and operate in different "states" depending on performance needs, plus various memories and other components. Appx1841-1845; Appx1913.

VLSI's infringement claim focused on the C6SRAM component in the accused microprocessors. Appx1453. The C6SRAM is a small memory that, along with other components, collectively form the "ring" domain. Appx1842-1845; Appx2726-2727; Appx15344. The C6SRAM serves one purpose: it stores information about the state of a processor core when that core is turned off (or "sleeping"). Appx1833-1834. The core then uses that stored information to resume operations when it "wake[s] back up." Appx1834; *see also* Appx1395; Appx1938.

Under most circumstances, the ring components (including the C6SRAM) receive a voltage from the "VCCR" supply. Appx1845; Appx1939. During operational states when the chip's processor cores are awake, the VCCR voltage level is set to one of three voltage levels: RING_VF_VOLTAGE_0, RING_VF_VOLTAGE_1, or RING_VF_VOLTAGE_2. Appx1850-1855; Appx1949-1950; Appx2757-2760; Appx15343. During certain states when some processor cores are asleep, the VCCR voltage level is instead set to a voltage level called "RING_RETENTION_VOLTAGE." Appx1859-1861; Appx1951.

Whenever the chip enters a deep sleep state called "Package C7" (i.e., when all processor cores are asleep (Appx1388)), a multiplexer switches the C6SRAM's

voltage supply from VCCR to a second supply called "VCCIO" and the ring components other than the C6SRAM are essentially turned off. Appx1845-1849; Appx1862-1865; Appx1939-1940; Appx1960; Appx2669-2670. RING_RETENTION_VOLTAGE is not involved in this voltage-switching process. Appx1862; Appx2744-2747.

C. District Court Proceedings

Neither party requested a claim construction for the '373 patent, as everyone agreed that the claim language's plain meaning should apply. At trial, VLSI's expert Dr. Conte opined that Intel's products infringed the '373 patent literally, but did not present any theory of infringement under the doctrine of equivalents. Appx1451; *see* Appx3807-3808. Dr. Conte testified that RING_RETENTION_VOLTAGE was the claimed "minimum operating voltage" of Intel's C6SRAM memory. Appx1451; Appx2727-2728. He also contended that a multiplexer in Intel's products selects which voltage to provide to the C6SRAM in the claimed manner, despite admitting that the multiplexer does not actually use RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") in any way when making that selection. Appx2735-2736.

The jury found literal infringement and awarded $1.5 billion in damages for the '373 patent. Appx9; Appx13. The district court denied Intel's post-trial motions, added pre-judgment interest, and entered final judgment. Appx98-100.

D. Proceedings Before This Court

On appeal, a panel of this Court affirmed the literal-infringement judgment for the '373 patent. Op. 10-13. First, the panel concluded that substantial evidence supported the jury's finding that RING_RETENTION_VOLTAGE is the claimed "minimum operating voltage" of the C6SRAM memory in Intel's products. Second, and as relevant to this petition, the panel concluded that substantial evidence also supported the jury's finding that Intel's products use a multiplexer to switch the C6SRAM's voltage source in a manner that satisfies the claim limitations that require: (1) providing the first regulated voltage to the memory "when the first regulated voltage is at least the value of the minimum operating voltage"; and (2) providing the second regulated voltage to the memory "when the first regulated voltage is less than [or below] the value of the minimum operating voltage" (collectively, the "when" claim limitations). *Id.*

With respect to the "when" limitations, the panel stated that "Intel's argument turns entirely on its contention that the claims require that falling below the minimum operating voltage be the ***causal trigger*** for switching from one voltage source to a different one." Op. 12 (emphasis added). The panel deemed that a claim construction argument, which Intel had not presented to the district court, and therefore "defer[red] to the jury's view of" the plain claim language in assessing infringement. *Id.* at 12-13. Next, the panel stated that "[t]he 'when' claim language

can reasonably be understood to mean simply 'at the time that.'" *Id.* at 13. Applying that interpretation, the panel concluded that there "was sufficient evidence for the jury to find that the [C6SRAM] voltage source switches ***at the time that*** VCCR voltage drops below the minimum for C6 SRAM's data retention—RING_RETENTION_VOLTAGE." *Id.* (emphasis added). The panel then affirmed the literal-infringement judgment on that basis, stating that "no further explanation" of the mechanism for deciding when to switch the C6SRAM voltage source in Intel's products "[wa]s required." *Id.*

After affirming the infringement judgment, the panel vacated the damages award for the '373 patent—because VLSI's experts had calculated damages using unreliable technical inputs chosen by trying to match data that represented use of non-infringing functionality—and remanded for a new trial on damages. Op. 24-27. The panel also reversed the district court's denial of Intel's motion to amend its answer to add a license defense that arose during the litigation, and remanded to allow Intel the opportunity to pursue that defense to VLSI's infringement claim. *Id.* at 28-33.[1]

[1] Additionally, the panel reversed the infringement judgment for the other patent-in-suit because VLSI failed to present substantial evidence of infringement under the doctrine of equivalents. Op. 13-19.

ARGUMENT

I. PANEL REHEARING IS WARRANTED BECAUSE THE PANEL OVERLOOKED UNDISPUTED EVIDENCE AND MISAPPREHENDED INTEL'S ARGUMENT.

A. The Panel Overlooked The Undisputed Evidence Demonstrating That Intel's Products Switch The C6SRAM's Voltage Supply *Before* The VCCR Voltage Level Drops.

The panel affirmed the literal-infringement judgment for the '373 patent because it concluded there was "sufficient evidence for the jury to find that the voltage source switches ***at the time that*** VCCR voltage drops below the minimum for C6 SRAM's data retention—RING_RETENTION_VOLTAGE." Op. 13 (emphasis added). The panel relied on testimony from VLSI's expert and his discussion of an Intel document stating that "[w]hen VCCR is powered down, the [multiplexer] will switch the [C6SRAM] memory over to the VCCIO supply which never powers down." *Id.* (quoting Appx2666, which discussed Exhibit 1588 (Appx8830-8831), and citing Appx2430-2431; Appx2757-2758; Appx2664-2670).

The panel's analysis, however, overlooked the sequence of events that occurs in Intel's products. It was ***undisputed*** at trial that Intel's multiplexer switches the C6SRAM voltage supply from VCCR to VCCIO ***before*** the VCCR voltage level drops below RING_RETENTION_VOLTAGE. Intel's engineer explained this precise sequence: "it's going to turn that switch from VCCR over to VCCIO, and then it's going to turn that VCCR supply off." Appx1862-1863(862:21-863:9). VLSI's expert Dr. Conte agreed; he confirmed that the "ramp[ing] down" of the

VCCR voltage level occurs "when the mu[ltiplexer] is ***already switched***" to VCCIO. Appx2672-2673(20:3-21:17) (emphasis added)[2]; Appx2671-2672(19:21-20:2) (Dr. Conte: "VCCR … is ramped down. It doesn't turn off simultaneously. So ***after the switch turns***, this thing will slowly ramp down." (emphasis added)); *see also* Red Br. 32 (VLSI admitting that VCCR only "falls below RING_RETENTION_VOLTAGE as it is gradually reduced to zero"). Thus, for at least some period of time after the multiplexer switches the voltage source in Intel's products, VCCIO (the alleged "second regulated voltage") is provided to the C6SRAM memory "when" VCCR (the alleged "first regulated voltage") is still at or above RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage"). That is the ***opposite*** of what the "when" limitations require. *See supra* pp. 6-7; *see generally* Blue Br. 35; Gray Br. 4.

Given this undisputed evidence, the panel erred in concluding that the jury could have reasonably found that the C6SRAM "voltage source switches ***at the time that*** VCCR voltage drops below … RING_RETENTION_VOLTAGE." Op. 13 (emphasis added). Rather, as explained above, the trial record conclusively established that the voltage source switches ***before*** VCCR drops below RING_RETENTION_VOLTAGE. This is not a trivial distinction. It demonstrates

[2] Dr. Conte provided this testimony in the context of describing the same Intel document that the panel relied on. *See* Appx2672(20:3-7) (discussing Exhibit 1588).

that Intel's products do not follow the conditions established by the "when" limitations—including under the panel's understanding of the claim language's plain meaning—and that there can be no literal infringement. *See Litton Sys., Inc. v. Honeywell, Inc.*, 140 F.3d 1449, 1454 (Fed. Cir. 1998) ("Literal infringement requires that the accused device contain each limitation of the claim exactly; any deviation from the claim precludes a finding of literal infringement."); *Johnston v. IVAC Corp.*, 885 F.2d 1574, 1580 (Fed. Cir. 1989) ("Where a claim does not read on an accused device exactly, there can be no literal infringement.").

B. The Panel Misapprehended Intel's Non-Infringement Position With Respect To The "When" Limitations.

In rejecting Intel's non-infringement position concerning the "when" limitations, the panel also stated that "Intel's argument turns entirely on its contention that the claims require that falling below the minimum operating voltage be the ***causal trigger*** for switching from one voltage source to a different one." Op. 12 (emphasis added). But Intel never made that argument. *See* Blue Br. 33-36; Gray Br. 2-5. Moreover, when asked at oral argument, Intel's counsel explained that Intel was not contending that the "when" limitations require falling below the "minimum operating voltage" to be a "trigger" for switching the voltage source. *See* Oral Arg. 08:15-09:28.

Instead, Intel merely argued that the claimed "minimum operating voltage" must be involved in some way in determining which voltage to provide to the

memory. *See* Blue Br. 33-36; Gray Br. 2-5; Oral Arg. 10:20-10:30 (Intel's counsel: "The idea that [the alleged 'minimum operating voltage'] doesn't need to be involved in any way at all, and you can infringe the claim, is inconsistent with the claim on its face."). That is the clear logical implication of the plain claim language, as the "when" limitations—when read in their entirety—specify which of two voltages to provide to the memory based solely on whether the first regulated voltage is (1) "at least" or (2) "less than" the "minimum operating voltage." *See supra* pp. 6-7. Critically, Intel's non-infringement argument did not further limit the manner in which the "minimum operating voltage" must be involved, as the panel assumed.

The panel's misapprehension of Intel's argument prevented it from fully or correctly analyzing the infringement issue with respect to the "when" limitations. It was undisputed that RING_RETENTION_VOLTAGE is not involved in determining "when" to provide which voltage (i.e., VCCR or VCCIO) to the C6SRAM memory in Intel's products. *See* Blue Br. 33-34 (citing trial evidence); Gray Br. 3. Nevertheless, the panel expressly declined to consider any "further explanation of the decision mechanism" in Intel's products because it viewed Intel as urging a "claim construction" that required falling below the minimum operating voltage to be the "causal trigger" for switching voltage sources. Op. 12-13. Consequently, the panel did not consider Intel's full non-infringement argument, which also explained how the accused products do not follow the specific conditions

imposed by the "when" limitations and, in fact, do the ***opposite*** of what the plain claim language requires. *See* Blue Br. 33-36; Gray Br. 2-5; *supra* pp. 12-14.

II. ALTERNATIVELY, EN BANC REHEARING IS WARRANTED BECAUSE THE PANEL'S DECISION CONFLICTS WITH THIS COURT'S PRECEDENT REQUIRING THAT EVERY WORD OF A PATENT CLAIM BE GIVEN MEANING.

As discussed above, the panel concluded that the jury could have reasonably found literal infringement of the '373 patent under the plain and ordinary meaning of the claim language. Op. 12-13. That conclusion, however, violated the rule that "[g]iving a term its plain and ordinary meaning does not leave the term devoid of any meaning whatsoever." *WARF*, 905 F.3d at 1348.

In addressing the "when" limitations, the panel's infringement analysis focused narrowly on the word "when." Even though there was no dispute between the parties as to the plain meaning of that word, the panel stated that "[t]he 'when' claim language can reasonably be understood to mean simply 'at the time that.'" Op. 13. Applying that interpretation, the panel then concluded that there was "sufficient evidence for the jury to find that the voltage source switches ***at the time that*** VCCR voltage drops below the minimum for C6 SRAM's data retention—RING_RETENTION_VOLTAGE." *Id.* (emphasis added). That was the extent of the panel's infringement analysis for the "when" limitations. *See* Op. 13.

Intel's non-infringement argument, however, did not turn on the meaning of the word "when" in isolation. Instead, it relied on the conditions established by the

"when" limitations as a whole. *See* Blue Br. 33-36; Gray Br. 2-5. Considered together, the "when" limitations specify which of two voltages to provide to the memory depending on whether a first regulated voltage is (1) "at least" or (2) "less than" the memory's "minimum operating voltage":

Condition	**Voltage Provided To The Memory**
"when the first regulated voltage is ***at least … the minimum operating voltage***"	"first regulated voltage"
"when the first regulated voltage is ***less than … the minimum operating voltage***"	"second regulated voltage"

Appx111(13:20-27); *see* Appx111(14:8-13). In other words, by their plain language, the "when" limitations dictate exactly which voltage must be provided to the memory at all times. *See* Blue Br. 7-10, 33-34; Gray Br. 2-3, 5. Thus, as even VLSI's expert Dr. Conte acknowledged, these limitations "tell[] you when to use a different voltage" and, in so doing, both "refer to the minimum operating voltage." Appx2733-2734.

By focusing on the word "when" rather than considering the "when" limitations in their entirety, the panel's infringement analysis failed to give meaning to every word in the disputed claim limitations. In fact, the panel never actually considered whether Intel's accused products provide the C6SRAM memory with (1) VCCR (the alleged "first regulated voltage") "when" VCCR is "at least" RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") ***and***

(2) VCCIO (the alleged "second regulated voltage") "when" VCCR is "less than" RING_RETENTION_VOLTAGE. *See* Op. 12-13. Had it done so by reading the "when" claim limitations together and giving meaning to every word contained therein, the panel would have concluded that Intel's products do not follow these exact conditions. Rather, as explained above, the trial evidence showed that VCCIO (the alleged "second regulated voltage") is provided to the C6SRAM memory "when" VCCR (the alleged "first regulated voltage") is still at or above RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage")—the ***opposite*** of what the "when" limitations require. *See supra* pp. 12-14.

Accordingly, under an analysis that gives meaning to every word in the "when" claim limitations, there can be no literal infringement. *See WARF*, 905 F.3d at 1348 (applying the claim language's plain meaning and concluding that there was not substantial evidence of infringement because the patentee's infringement theory failed to give meaning to every claim term).

CONCLUSION

Intel respectfully requests that the Court grant panel or en banc rehearing to reverse the infringement judgment for the '373 patent.

Respectfully submitted,

/s/ William F. Lee

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February 2, 2024

ADDENDUM

United States Court of Appeals for the Federal Circuit

VLSI TECHNOLOGY LLC,
Plaintiff-Appellee

v.

INTEL CORPORATION,
Defendant-Appellant

2022-1906

Appeal from the United States District Court for the Western District of Texas in No. 6:21-cv-00057-ADA, Judge Alan D. Albright.

Decided: December 4, 2023

JEFFREY A. LAMKEN, MoloLamken LLP, Washington, DC, argued for plaintiff-appellee. Also represented by RAYINER HASHEM, MICHAEL GREGORY PATTILLO, JR.; MORGAN CHU, BENJAMIN W. HATTENBACH, ALAN J. HEINRICH, AMY E. PROCTOR, DOMINIK SLUSARCZYK, CHARLOTTE J. WEN, Irell & Manella LLP, Los Angeles, CA; BABAK REDJAIAN, Newport Beach, CA.

WILLIAM F. LEE, Wilmer Cutler Pickering Hale and Dorr LLP, Boston, MA, argued for defendant-appellant. Also represented by ALISON BURTON, LAUREN B. FLETCHER, JOSEPH J. MUELLER; STEVEN JARED HORN, AMANDA L.

MAJOR, Washington, DC; MARY VIRGINIA SOOTER, Denver, CO.

Before LOURIE, DYK, and TARANTO, *Circuit Judges*.

TARANTO, *Circuit Judge*.

VLSI Technology LLC owns U.S. Patent No. 7,523,373, titled "Minimum Memory Operating Voltage Technique" and U.S. Patent No. 7,725,759, titled "System and Method of Managing Clock Speed in an Electronic Device." VLSI sued Intel Corporation, alleging infringement of both patents, and after a trial, the jury found infringement of both patents and awarded separate damages for each. The district court then denied Intel's post-trial motions on various issues concerning infringement and damages. It simultaneously denied Intel's pre-trial motion seeking to add a license defense to the case and to sever that defense from the rest of the case and stay its adjudication.

Intel appeals. We affirm the judgment of infringement of the '373 patent but reverse the judgment of infringement of the '759 patent. We vacate the award of damages for the '373 patent and remand for a new trial limited to damages. We reverse the denial of the motion for leave to amend to add the license defense.

I

On April 11, 2019, VLSI sued Intel for patent infringement. VLSI asserted claims 1, 5, 6, 9, and 11 of the '373 patent and claims 14, 17, 18, and 24 of the '759 patent. After a six-day trial, the jury found that Intel literally infringed all asserted claims of the '373 patent and that Intel infringed all asserted claims of the '759 patent, but only under the doctrine of equivalents.

A

The '373 patent describes, among other things, a featured embodiment in which an integrated circuit has a memory and a processor; the memory has a minimum operating voltage; and when the processor is provided power at a voltage below the memory-minimum level (*e.g.*, when the processor is in a low-power state), the memory is provided power at a higher voltage than the processor. '373 patent, Abstract. Figure 1 illustrates the circuit of that embodiment:

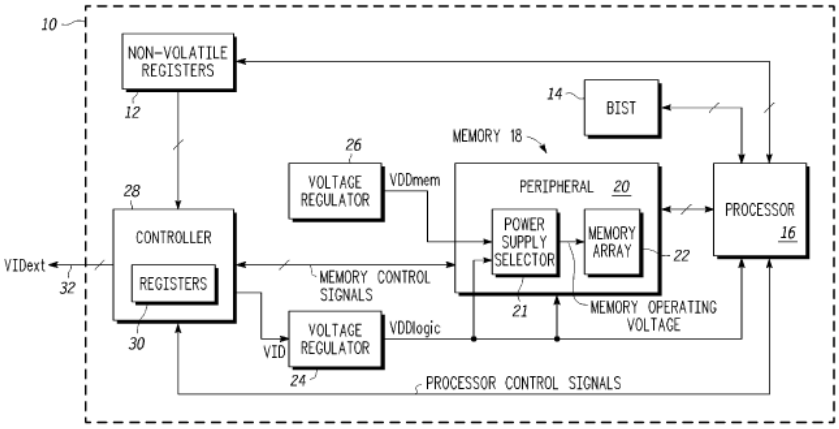

FIG. 1

Figure 1 discloses a memory 18, which has a minimum operating voltage. *Id.*, col. 6, lines 33–36. Figure 1 also discloses two voltage regulators: voltage regulator 24, which provides a scalable power supply voltage, VDDlogic, to both processor 16 and memory 18; and voltage regulator 26, which provides a substantially fixed power supply voltage, VDDmem, just to memory 18. *Id.*, col. 3, lines 21–29. The memory 18 includes a power supply selector 21, which receives both power supply voltages VDDmem and VDDlogic, and provides one of them to memory array 22 as the memory operating voltage. *Id.*, col. 2, lines 50–57. "In one embodiment, while VDDlogic remains above a minimum operating voltage required for successful reads of memory array 22, power supply selector 21 selects VDDlogic as the

memory operating voltage provided to memory array 22 . . . ." *Id.*, col. 3, lines 30–35. "When VDDlogic is scaled to a voltage that is below the minimum memory operating voltage required for reads, power supply selector 21 selects the higher voltage, VDDmem . . . ." *Id.*, col. 3, lines 35–39.

The claims are not limited to the featured embodiment just described. Independent claim 1 claims a method:

> 1. A method, comprising:
>
> providing an integrated circuit with a memory;
>
> operating the memory with an operating voltage;
>
> determining a value of a minimum operating voltage of the memory;
>
> providing a non-volatile memory (NVM) location;
>
> storing the value of the minimum operating voltage of the memory in the NVM location;
>
> providing a functional circuit on the integrated circuit exclusive of the memory;
>
> providing a first regulated voltage to the functional circuit;
>
> providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;
>
> providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and
>
> providing the second regulated voltage as the operating voltage of the memory when

> the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

Id., col. 13, lines 7–28. Independent claim 9 claims a circuit, using non-identical but similar language related to the points in issue on appeal:

> 9. An integrated circuit, comprising:
>
> a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage;
>
> a memory location that stores a value representative of the minimum operating voltage;
>
> a first voltage regulator for supplying a first regulated voltage;
>
> a circuit that provides a function and uses the first regulated voltage;
>
> a second voltage regulator for supplying a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage; and
>
> a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage, wherein while the second regulated voltage is

> supplied as the operating voltage, the circuit uses the first regulated voltage.

Id., col. 13, line 59–col. 14, line 15. Those claims are representative for purposes of this appeal.

The Intel products that are the subject of VLSI's allegations of infringement of the '373 patent are Intel's Haswell and Broadwell microprocessors. Each such microprocessor contains a plurality of processor cores that run computer programs. It also contains a Ring domain, containing other circuitry; the Ring domain is sometimes called a CLR domain, reflecting that the domain contains, though is not limited to, circuitry referred to as ***C***BO circuitry, ***L***ast Level Cache circuitry, and ***R***ing circuitry. The Ring (CLR) domain contains, in addition to the CLR circuitry, a static random access memory, *i.e.*, a C6 SRAM. The C6 SRAM, as long as it is adequately powered, can store information about the state of a core before the core goes into low power mode, enabling the core, when it "wake[s] back up," to use the stored information to "pick up where [it] left off." J.A. 1395.

The accused microprocessors also contain two voltage regulators: VCCR and VCCIO. Ordinarily, the VCCR supplies power to the entire Ring domain, including the C6 SRAM, at variable power supply levels: RING_VF_VOLTAGE_0, RING_VF_VOLTAGE_1, and RING_VF_VOLTAGE_2. Each of these power supply levels is stored in a fuse, a type of memory that retains its data even if power is removed from it. Another fuse stores a different power supply level from the three just mentioned: It stores RING_RETENTION_VOLTAGE, which an Intel document characterizes as the "worst case retention voltage" for the memory device (the C6 SRAM). J.A. 9574, 12642; *see* J.A. 1859, 1951, 2655–57, 2730. If all cores are idle, Intel's accused microprocessors can enter a sleep state called Package C7. In that state, substantial evidence shows, the cores and CLR components of the Ring domain

are put to sleep, the VCCR voltage is brought below the RING_RETENTION_VOLTAGE, and the C6 SRAM receives power not from the VCCR but from the VCCIO, at a voltage higher than the reduced VCCR voltage. *See* J.A. 1388, 1845-49, 1862–63, 1938–40, 2661–66, 3225–26.

B

The '759 patent describes a system in which at least two devices, such as computer processors, are coupled to a bus that can operate at a variety of frequencies (clock speeds); one of the devices, based on its workload (which, *e.g.*, indicates a need for faster operations), asks a clock controller to change a clock frequency; and the controller is programmed to respond by outputting a clock frequency to control the speed of the bus and a second device coupled to the bus. '759 patent, Abstract. Figure 1 illustrates the system:

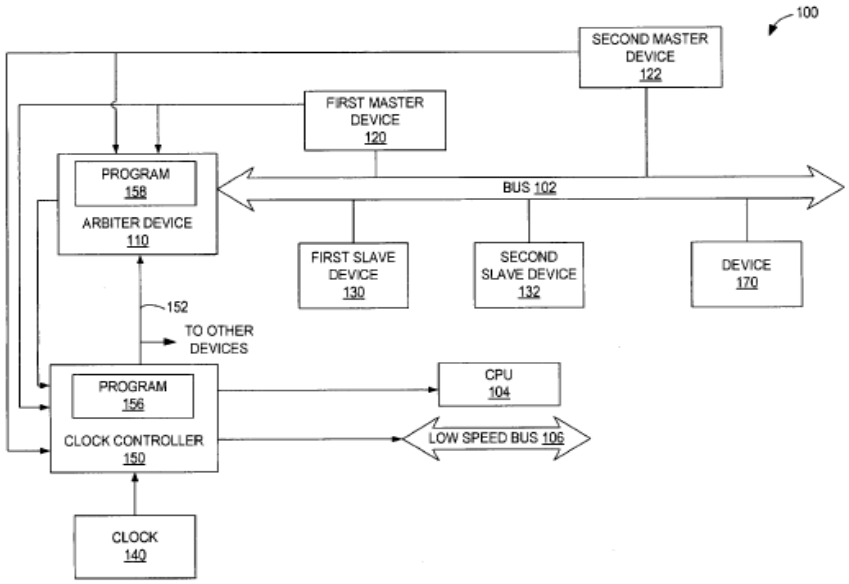

FIG. 1

In Figure 1, master device 120 is coupled to a bus 102. *Id.*, col. 2 line 66–col. 3, line 3 and col. 3, lines 22–25. A programmable clock controller 150 can control the clock 152 to set the frequency of the bus 102 or devices coupled to the bus, including master device 122. *Id.*, col. 3, lines

29–51 and col. 4, lines 20–29. Master device 120 can provide a trigger input to the controller, *e.g.*, in response to a desired increase in device performance, *id.*, col. 3, line 64–col. 4 line 8, and the controller can receive the trigger input and adjust the clock frequency of the bus or of a second master device 122. *Id.*, col. 4, lines 42–47.

Independent claim 14 is representative for present purposes:

> 14. A system comprising:
>
> a bus capable of operation at a variable clock frequency;
>
> a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and
>
> a programmable clock controller having an embedded computer program therein, the computer program including instructions to:
>
> receive the request provided by the first master device;
>
> provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and

> provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

Id., col. 8 line 50–col. 9, line 4.

The Intel products that are the subject of VLSI's allegations of infringement of the '759 patent are various Intel microprocessors with "Lake" in their names. The accused microprocessors feature cores and a Ring bus connecting the cores. As VLSI describes the microprocessors and their operation as relevant here, VLSI Br. at 13–15, 35–39, the microprocessors also include a power control unit (PCU), which is a microcontroller running software called p-code ("programs," VLSI Br. at 13) and which controls the frequency of the cores and the Ring bus. This control is exercised when a core monitors its workload and sends a Core_Active signal to the power control unit. J.A. 2690–92. Based on that signal, core-specific p-code in the power control unit (described as one "module" of p-code) calculates a speed change, to a higher or lower frequency, and provides a request for that speed change to another "module" of the p-code software in the power control unit, namely, a "decision instructions" module. J.A. 2706–09; *see* VLSI Br. at 14, 38–39. The decision instructions module receives the request and in turn outputs a signal from the power control unit to change the frequency of the Ring bus or of another core on the bus. J.A. 2699–703, 2707–10.

C

A jury trial was held in late February and early March 2021. The jury found literal infringement of all the asserted claims of the '373 patent. J.A. 9. For all the asserted claims of the '759 patent, the jury found no literal infringement but found infringement under the doctrine of

equivalents. J.A. 9–10.[1] The jury awarded VLSI nonoverlapping damages for the infringement of the two patents—$1.5 billion for the '373 patent and $675 million for the '759 patent—each award a lump sum payment for all past and future infringement over the life of the patent. J.A. 13–14.

The district court denied various post-trial motions concerning infringement and damages. J.A. 16–64, 74–97. The court also ruled, after the trial, on a motion that Intel had filed in the fall of 2020, a few months before trial, in which Intel (a) sought to amend its answer to assert a defense that it was licensed to practice both VLSI patents but (b) requested that the defense be severed from the rest of the case and its adjudication stayed. The motion was based on a recent change in ownership of Finjan, Inc., which had a license agreement with Intel. Intel argued that the license now covered VLSI's '373 and '759 patents because VLSI and Finjan were now both under the control of Fortress Investment Group LLC. The district court denied the motion. J.A. 65–73.

On April 21, 2022, the district court entered final judgment. J.A. 98–100. Intel timely appealed. We have jurisdiction to hear the appeal under 28 U.S.C. § 1295(a)(1).

II

We first address the appeals of the infringement verdicts. We review the verdicts of infringement for substantial-evidence support. *Lucent Technologies, Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1309–10 (Fed. Cir. 2009).

A

With respect to the '373 patent, Intel argues on two grounds that the evidence is insufficient to support the

---

[1] The jury also found no willfulness on Intel's part and rejected Intel's defense of invalidity for anticipation. J.A. 11–12. Neither ruling is at issue before us.

infringement verdict. First, Intel argues that the RING_RETENTION_VOLTAGE in the accused microprocessors, which is what VLSI contended is the "minimum operating voltage" required by the claims, is not actually the minimum voltage at which the C6 SRAM can retain data and therefore does not come within the several claim limitations requiring a "minimum operating voltage." Second, Intel argues that the RING_RETENTION_VOLTAGE is not used in the microprocessors to determine which voltage to supply to the C6 SRAM (VCCR or VCCIO) and therefore the several "when" limitations (the last two limitations of claim 1, the last limitation of claim 9) are not satisfied. We reject these arguments.

1

There is ample expert testimony, with adequate support in Intel's internal documents, that Intel's RING_RETENTION_VOLTAGE is the minimum operating voltage of the C6 SRAM. At trial, VLSI identified Intel's C6 SRAM as the claimed "memory" and Intel's RING_RETENTION_VOLTAGE as the claimed "minimum operating voltage." J.A. 2661. VLSI's expert, Dr. Conte, pointed to Intel's component specifications for the Haswell and Broadwell microprocessors, which defined the RING_RETENTION_VOLTAGE as the "worst case retention voltage" for the Ring domain, and he explained that this constituted "the lowest voltage for memory to still remember." J.A. 2656–57, 9574, 12642. Dr. Conte made explicit that the worst case retention voltage is the minimum operating voltage for the C6 SRAM, which is in the Ring domain. J.A. 2656–57.

Intel's argument that this evidence does not constitute substantial evidence on the point in dispute is that Intel's C6 SRAM is operational and retains data at a RING_VF_VOLTAGE_0 voltage, even when it is lower than RING_RETENTION_VOLTAGE. Intel relied critically for this argument on a comparison done by its expert,

Dr. Sylvester. *See*, *e.g.*, J.A. 1854–55, 1859–61, 1945–50, 15342–43. But the jury could reasonably credit VLSI's evidence that the comparison presented by Intel was faulty, in that the two voltages compared by Dr. Sylvester were measured under critically different conditions.

Specifically, Dr. Conte testified that Dr. Sylvester's comparison of RING_VF_VOLTAGE_0 and RING_RETENTION_VOLTAGE values does not show that RING_VF_VOLTAGE_0 is ever lower than RING_RETENTION_VOLTAGE under comparable conditions, because the relevant memory's retention voltage is (inversely) dependent on temperature, and Dr. Sylvester had compared RING_VF_VOLTAGE_0 at 100 degrees Celsius to RING_RETENTION_VOLTAGE at 0 degrees Celsius. J.A. 2429–30. Dr. Conte testified: "When you compensate for temperature, [RING_VF_VOLTAGE_0] is going to be always above the RING_RETENTION_VOLTAGE." J.A. 2430. Additionally, Dr. Conte relied on an Intel technical manual containing graphs showing a "Vretention" line and (among other things) a "v/f 0" value, the former lower than the latter. *See* J.A. 19243. Dr. Conte testified that Vretention corresponded to RING_RETENTION_VOLTAGE and v/f 0 corresponded to RING_VF_VOLTAGE_0. J.A. 2426. The jury reasonably could credit this evidence and reject Intel's contention on the point.

Accordingly, substantial evidence supports the jury's verdict in favor of VLSI on this point.

2

Intel's second argument against the sufficiency of the infringement evidence regarding the '373 patent also fails. Intel's argument turns entirely on its contention that the claims require that falling below the minimum operating voltage be the causal trigger for switching from one voltage source to a different one. But that is an argument for a claim construction, and Intel sought no claim construction

on this point. When a claim phrase is not construed, we defer to the jury's view of the claim element unless that view is contrary to the only reasonable view of the claim element. *Avid Technology, Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1048–49 (Fed. Cir. 2016); *Hewlett-Packard Co. v. Mustek Systems, Inc.*, 340 F.3d 1314, 1320–21 (Fed. Cir. 2003). And under that standard, Intel cannot succeed on appeal.

The "when" claim language can reasonably be understood to mean simply "at the time that." Dr. Conte testified, with support from the Intel "Vretention" document, that VCCR is the power source for the C6 SRAM at the time that VCCR voltage is above RING_RETENTION_VOLTAGE and that "[w]hen VCCR is powered down, the [multiplexer] will switch the [C6 SRAM] memory over to the VCCIO supply which never powers down," and thereby ensures that the C6 SRAM has sufficient voltage to retain data. J.A. 2666; *see* J.A. 2430–31, 2757–58, 2664–70. This was sufficient evidence for the jury to find that the voltage source switches at the time that VCCR voltage drops below the minimum for C6 SRAM's data retention—RING_RETENTION_VOLTAGE. Intel did not present evidence requiring a contrary finding on those points. And no further explanation of the decision mechanism is required in the absence of the claim construction that Intel now effectively urges but did not seek in the district court.

Accordingly, substantial evidence supports the jury's verdict on this point—and, hence, on infringement of the '373 patent. The judgment of infringement of the '373 patent is therefore affirmed.

B

With respect to the '759 patent, Intel argues on two grounds that the verdict of infringement—under the doctrine of equivalents—must be reversed. First, Intel argues that prosecution history estoppel bars VLSI's theory of

equivalents. Second, Intel argues that VLSI's evidence of equivalents was legally insufficient. We agree with the second argument and do not reach the first.

1

The doctrine of equivalents provides a limited exception to the principle that claim meaning defines the scope of the exclusivity right in our patent system: "Applied more broadly, the doctrine [of equivalents] would conflict with the primacy of the claims in defining the scope of a patentee's exclusive rights." *Sage Products, Inc. v. Devon Industries, Inc.*, 126 F.3d 1420, 1424 (Fed. Cir. 1997); *see Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 29 (1997); *Aro Manufacturing Co. v. Convertible Top Replacement Co.*, 365 U.S. 336, 339 (1961); *Johnson & Johnston Associates Inc. v. R.E. Service Co.*, 285 F.3d 1046, 1052 (Fed. Cir. 2002) (en banc); *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1356 (Fed. Cir. 2012). The limits reflect a familiar balance among the importance of preserving the public's ability to rely on claims' meaning to define patent scope, the ability of patentees to protect their inventions through their claim drafting, and (yet) the occasional need to recognize some non-literal scope of protection to avoid undermining the exclusivity rights authorized by Congress to incentivize certain innovations. *See Mahn v. Harwood*, 112 U.S. 354, 361 (1884) ("The public is notified and informed . . . that [the patentee's] claim to invention is for such and such an element or combination, and for nothing more."); *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 731 (2002) ("If patents were always interpreted by their literal terms, their value would be greatly diminished. Unimportant and insubstantial substitutes . . . could defeat the patent[.]"); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 373–74 (1996); *Graver Tank & Mfg. Co. v. Linde Air Products Co.*, 339 U.S. 605, 607 (1950). We have explained that liability under the doctrine is "exceptional," *Honeywell International, Inc. v. Hamilton Sundstrand Corp.*, 523 F.3d 1304,

1313 (Fed. Cir. 2008), and "[w]e have emphasized . . . that the doctrine of equivalents is the exception, however, not the rule," *Eli Lilly & Co. v. Hospira, Inc.*, 933 F.3d 1320, 1330 (Fed. Cir. 2019) (internal quotation marks omitted).

The exceptional character of the doctrine's use is maintained by closely related demands that restrict the availability of liability under the doctrine. Among them are the following. First, proof of equivalents must be limitation specific, not focused only on the claim as a whole, though the limitation-specific inquiry of equivalence may be informed by the "role played by each element in the context of the specific patent claim." *Warner-Jenkinson*, 520 U.S. at 40; *see DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1017 (Fed. Cir. 2006); *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.,* 149 F.3d 1309, 1315 (Fed. Cir. 1998); *Dawn Equipment Co. v. Kentucky Farms Inc.*, 140 F.3d 1009, 1015 (Fed. Cir. 1998). Second, for the determination of whether a substitute element is only insubstantially different from a claimed element and hence an equivalent, a traditional formulation—appropriate for this case, as VLSI's use of it indicates—asks "whether a substitute element matches the function, way, and result of the claimed element." *Warner-Jenkinson*, 520 U.S. at 40. Such matching requires that each of function, way, and result be "substantially the same," *see Spectrum Pharmaceuticals, Inc. v. Sandoz Inc.*, 802 F.3d 1326, 1337 (Fed. Cir. 2015), with the "way" requirement of particular importance, as a practical matter, in keeping the doctrine properly limited. *See Warner-Jenkinson*, 520 U.S. at 35, 39; *Union Paper-Bag Machine Co. v. Murphy*, 97 U.S. 120, 125 (1877) (stressing the crucial importance of "way"); *Advanced Steel Recovery, LLC v. X-Body Equipment, Inc.*, 808 F.3d 1313, 1320 (Fed. Cir. 2015) (similar); *Zygo Corp. v. Wyko Corp.*, 79 F.3d 1563, 1569 (Fed. Cir. 1996) (similar); *Slimfold Manufacturing Co. v. Kinkead Industries, Inc.*, 932 F.2d 1453, 1457–58 (Fed. Cir. 1991) (similar). Third, we have long demanded specificity and completeness of

proof as crucial to enforcing the limits on the doctrine: The patentee must provide "particularized testimony and linking argument as to the insubstantiality of the differences between the claimed invention and the accused device." *Akzo Nobel Coatings, Inc. v. Dow Chemical Co.*, 811 F.3d 1334, 1342 (Fed. Cir. 2016) (internal quotation marks omitted); *see Gemalto S.A. v. HTC Corp.*, 754 F.3d 1364, 1374 (Fed. Cir. 2014); *Texas Instruments Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1566–67 (Fed. Cir. 1996); *Lear Siegler, Inc. v. Sealy Mattress Co. of Michigan*, 873 F.2d 1422, 1426 (Fed. Cir. 1989).

2

VLSI's proof of equivalence for the '759 patent, though limitation specific, was insufficient under those principles.

VLSI's equivalents contention is best understood in light of its literal-infringement case (which the jury rejected). VLSI's expert, Dr. Conte, testified that a specified core in the accused microprocessors is the "first master device" under the claim, the Core_Active signal is the required "request to change a clock frequency," and the power control unit is the "programmable clock controller"—to which the core "provide[s]" the request (the Core_Active signal) and which "receive[s]" that request (the Core_Active signal). J.A. 2694–99. That mapping of claim terms onto the accused microprocessors embodied the ordinary notion of signals (carrying messages) going from one physical component to another. But there was evidence that the signal sent by the specified cores is not a request to change frequency based on changes the cores identified in their own performance, because it is only software running on the (receiving) power control unit that, based on observations of system conditions, calls for a frequency change. *See* J.A. 2083–85, 2188–89, 2748–51. And the jury eventually found no literal infringement. J.A. 9.

VLSI's alternative infringement theory, invoking the doctrine of equivalents, sought to accommodate the

evidence of the role played by the power control unit in making the claim-required request. Under this theory, the equivalent of the "first master device" as the provider of the "request to change a clock frequency" is the combination of (a) the core and (b) the core-specific p-code (a software module) residing on the power control unit that makes the frequency-change request, and the equivalent of the "programmable clock controller" is a different software module residing on the same power control unit, namely, the "decision instructions," with this software module receiving the request sent by the first software module, both software modules being within the power control unit. J.A. 2705–09. The jury found infringement under the doctrine of equivalents. J.A. 10.

Dr. Conte presented his evidence for equivalence using the function, way, result framework, *see* J.A. 2705, 2707, and the appropriateness of that framework is not disputed here. *See*, *e.g.*, *Brilliant Instruments, Inc. v. GuideTech, LLC*, 707 F.3d 1342, 1346–47 (Fed. Cir. 2013). Using that framework, VLSI had to show that the core and certain code, which resides on the power control unit, together perform substantially the same function, in substantially the same way, to achieve substantially the same result as the claimed "first master device" and that certain other instructions on the same power control unit perform substantially the same function, in substantially the same way, to achieve substantially the same result as the claimed "programmable clock controller." And VLSI had to present particularized testimony and linking argument to make that showing.

On the crucial point, Dr. Conte testified as follows:

> MR. HEINRICH (ATTORNEY FOR VLSI). Okay. So now, let's go back to your Doctrine of Equivalents analysis. Did you apply the function/[way]/result test?

> DR. CONTE. I did. So let's put a box around the core and the Core 1's [p]-code. And then this provides the same function as required by the claim, that is to provide a request.
>
> Q. And does it provide a request in substantially the same way as the claim?
>
> A. Yeah. The claims says[,] "the first master device provides a request." Now, it's the first master device and its [p]-code that provides the request.
>
> Q. And how do you characterize the difference between those two?
>
> A. It's just a difference of where an engineer draws this data line.
>
> Q. Is it a design choice?
>
> A. It's a design choice.
>
> Q. And what's the result?
>
> A. Well, the result is that a request is provided.
>
> Q. And is it the same result in each case?
>
> A. Yes. No, not really. So[,] each will provide a different—you mean in terms of—
>
> Q. That was a bad question. So[,] is the result of the core and its [p]-code sending a request to the [power control unit] the same result as what's required by the claim?
>
> A. Oh, I see. I misunderstood your question. Yes, it's the same result as required by the claim.

J.A. 2707–08.

That testimony is insufficient. It contains no meaningful explanation of why the way in which the request is made is substantially the same as what the claim prescribes. The question is not whether, in a schematic

drawing used to illustrate functions, an engineer could "draw[] . . . [a] line" in different places. The question is about actual functionality-location differences. It is not enough, moreover, to say that the different functionality-location placements were a "design choice." That label does not indicate whether, or begin to explain why, the options in the choice are substantially different or substantially the same: In both circumstances, the choice between the options is a design choice. The question that must be addressed is whether the difference in the way the functionalities are actually allocated between devices is an insubstantial one.

Here, the claim requires that the request function be performed by one component (master device) and the receipt and output functions be performed by a distinct component (programmable clock controller). According to VLSI itself, what occurs in Intel's accused microprocessors is that the request function is split between two physical components (core and power control unit), with the request complete only in the second component, and receipt and output occur within the second component as well. The request provision and the receipt/output are performed not by distinct physical components but by different software "modules"—one p-code module or a second instruction module. VLSI had to prove—with particularized testimony and linking argument—that the elements of the Intel arrangement were substantially the same as the elements of the claimed arrangement. But VLSI offered no meaningful testimony doing so. The above testimony says nothing remotely sufficient, especially in light of Intel's evidence about the significance of using the power control unit, rather than other particular components such as cores within the system, for making frequency decisions based on workload information. *See*, *e.g.*, J.A. 2146–47, 2195–96.

Based on the evidence presented, VLSI's doctrine of equivalents theory fails as a matter of law. The judgment of infringement of the '759 patent is therefore reversed.

III

Intel challenges the award of damages for infringement of the '373 patent.[2] In a pretrial motion under Federal Rule of Evidence 702, Intel challenged various aspects of the damages analysis set forth by VLSI's damages expert, and it made similar arguments in seeking a new trial after the jury verdict. *See* J.A. 1–2, 3533, 4107–09. As relevant here, the district court's denial of both motions is reviewable for abuse of discretion. *General Electric Co. v. Joiner*, 522 U.S. 136, 141 (1997); *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1202 (Fed. Cir. 2010); *Fornesa v. Fifth Third Mortgage Co.*, 897 F.3d 624, 627 (5th Cir. 2018). An abuse of discretion exists, for purposes of this appeal, if the damages analysis departed from an economically sound methodology under the legal principles governing royalty damages, overall and as applied, and if that departure cannot be deemed harmless. *See Summit 6, LLC v. Samsung Electronics Co.*, 802 F.3d 1283, 1295–96 (Fed. Cir. 2015); *VirnetX, Inc. v. Cisco Systems, Inc.*, 767 F.3d 1308, 1328 (Fed. Cir. 2014).

A

Certain well-established principles are relevant to Intel's challenge to the damages award at issue on appeal—which is a (lump-sum life-of-patent) reasonable-royalty award designed to compensate "for the use made of the invention by the infringer." 35 U.S.C. § 284. "The 'value of what was taken'—the value of the use of the patented technology—measures the royalty." *Aqua Shield v. Inter Pool Cover Team*, 774 F.3d 766, 770 (Fed. Cir. 2014) (quoting *Dowagiac Manufacturing Co. v. Minnesota Moline Plow*

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[2] Although Intel also challenges the award of damages for infringement of the '759 patent, we need not address that challenge because we hold that judgment of non-infringement of that patent is required.

Co., 235 U.S. 641, 648 (1915)). Any reasonable royalty must seek to measure the value of the patented technology—it must be "apportion[ed]" to that value—by separating out and excluding other value in economic products or practices. *See Finjan, Inc. v. Blue Coat Systems, Inc.*, 879 F.3d 1299, 1309 (Fed. Cir. 2018); *see also Garretson v. Clark*, 111 U.S. 120, 121 (1884); *Omega Patents, LLC v. CalAmp Corp.*, 13 F.4th 1361, 1376 (Fed. Cir. 2021); *Power Integrations, Inc. v. Fairchild Semiconductor International, Inc.*, 904 F.3d 965, 977 (Fed. Cir. 2018); *Commonwealth Scientific & Industrial Research Organization v. Cisco Systems, Inc.*, 809 F.3d 1295, 1301 (Fed. Cir. 2015); *Ericsson, Inc. v. D-Link Systems, Inc.*, 773 F.3d 1201, 1226 (Fed. Cir. 2014).

An economically sensible, commonly used method for determining this market value posits a "hypothetical negotiation" between the parties (based on certain assumptions, including validity of the patent) to "attempt[] to ascertain the royalty upon which the parties would have agreed had they successfully negotiated an agreement just before infringement began." *Lucent Technologies*, 580 F.3d at 1324. The analysis must be one that "tries, as best as possible, to recreate the *ex ante* licensing negotiation scenario and to describe the resulting agreement," recognizing that some steps in a sound analysis may involve unavoidable "approximation and uncertainty." *Id.* at 1325 (internal quotations omitted); *see Dowagiac*, 235 U.S. at 647. Substantively, subject to conditions not in dispute here, "the core economic question is what the infringer" in the hypothetical negotiation "would have anticipated the profit-making potential of use of the patented technology to be, compared to using non-infringing alternatives." *Aqua Shield*, 774 F.3d at 770 (italicization of "anticipated" removed); *see Carnegie Mellon University v. Marvell Technology Group, Ltd.*, 807 F.3d 1283, 1304 (Fed. Cir. 2015) ("A key inquiry in the analysis is what it would have been worth to the defendant, as it saw things at the time, to obtain the authority to use

the patented technology, considering the benefits it would expect to receive from using the technology and the alternatives it might have pursued.").

Also of relevance to the appeal before us is what we have said about the use of licenses in a royalty analysis. We have recognized that prices paid in actual licenses may have a proper role to play in valuing the patented technology at issue in a case, *see Apple Inc. v. Wi-LAN Inc.*, 25 F.4th 960, 971 (Fed. Cir. 2022); *Prism Technologies LLC v. Sprint Spectrum L.P.*, 849 F.3d 1360, 1368–69 (Fed. Cir. 2017), but the basic evidentiary precondition is that such licenses be "sufficient[ly] comparab[le]" to the royalty proposed by a party for the technology at issue, *Apple*, 25 F.4th at 971 n.5 (citing *Elbit Systems Land & C41 Ltd. v. Hughes Network Systems, LLC*, 927 F.3d 1292, 1299 (Fed. Cir. 2019)). That requirement often precludes use of other licenses that involve (only or even partly) technology other than the patented technology at issue in the case at hand, *e.g.*, where there is an inadequate basis for soundly extracting from such licenses information that is truly informative about the value of the technology in the case at hand. *See*, *e.g.*, *Apple,* 25 F.4th at 973–74; *LaserDynamics, Inc. v. Quanta Computer, Inc.*, 694 F.3d 51, 81 (Fed. Cir. 2012); *ResQNet.com, Inc. v. Lansa, Inc.*, 594 F.3d 860, 872–73 (Fed. Cir. 2010).

B

In the present case, Intel, for its part, presented a damages theory based on a comparable-license analysis, J.A. 2776–84, but we have no issue before us about whether Intel's analysis met the requirement of comparability in terms of the basic economic inquiry into value over alternatives, which could differ from technology to technology. Rather, what is before us is VLSI's damages proof, which led to a figure close to what the jury awarded. Intel's principal challenge to that proof is to the analysis developed by VLSI's experts, which, in four steps, sought, without

reliance on licenses, to identify the incremental value over non-infringing alternatives added to Intel's accused products by use of the asserted patents and the share of that value that Intel and VLSI would have agreed Intel would pay in a start-of-infringement hypothetical negotiation.

The first step in VLSI's royalty calculation, as applied to the '373 patent, was to quantify the effect of use of the '373 patent technology on the speed of Intel's Broadwell and Haswell microprocessors, derived from quantifying its effect on power savings. J.A. 3446. This quantification was based on testing done by one of VLSI's experts, Dr. Annavaram. *See* J.A. 1525–87. He tested Intel's Broadwell and Haswell microprocessors and determined that the power savings attributable to the '373 patent technology was 5.45%. J.A. 1593, 2681–82. Dr. Conte (the VLSI expert whose testimony on equivalents was discussed *supra*) then translated this power savings benefit into a speed benefit, finding a one-to-one ratio for Intel's Broadwell and Haswell microprocessors, so that the 5.45% power savings from use of '373 patent technology provided a 5.45% speed benefit. J.A. 2682–83.

Next, VLSI calculated the effect of a speed improvement on the price Intel could fetch for its products, including in its study a number of Intel products, not only the Broadwell and Haswell microprocessors. VLSI's damages expert, Dr. Sullivan, used a regression model to measure this effect of a speed improvement on price. J.A. 1609–13. Dr. Sullivan found that, as relevant here, each 1% improvement in speed was associated with a 0.764% increase in price for Intel's products. J.A. 1613–14, 15277–78.

Then, based on the quantified effect of the '373 patent technology on the speed of Intel's Broadwell and Haswell microprocessors and the calculated effect of a speed improvement on price for Intel's products, VLSI made a calculation of the incremental revenue attributable to Intel's use of the '373 patent technology in its Broadwell and

Haswell microprocessors. Specifically, Dr. Sullivan multiplied the 5.45% speed benefit, by the 0.764% price benefit, by the known total infringing revenues for Intel's Haswell and Broadwell microprocessors. J.A. 1655–1656, 15290. Dr. Sullivan determined the incremental revenue attributable to use of the '373 patent technology to be $2,115,862,744. J.A. 15290.

Finally, VLSI had to determine how Intel and VLSI would have divided up the calculated incremental revenues to set a royalty Intel would have paid VLSI for the right to use the patent technology. Reflecting the role of profits (not revenues per se) in the inquiry, J.A. 1658–59, 3449, Dr. Sullivan concluded that there were no incremental manufacturing costs incurred by adopting the technology, only other small, incremental costs, *e.g.*, costs of making sales, J.A. 1659–60, 3450–51. He then inquired into the "relative contributions" of Intel and VLSI to the production of the incremental revenues (and hence profits). J.A. 1660; *see* J.A. 3452–53. He did so by considering Intel's "total spending," including sales and marketing, research and development (R&D), and general and administrative (G&A) costs, seemingly allocating a proportionate share to the products at issue, and on that basis making "a reasonable estimate of Intel's contribution for purposes of the contribution apportionment." J.A. 3453, 1661–62; *see* J.A. 3461. The Intel contribution figure was 23.8% of total revenue for the two products, with a 76.2% contribution figure for VLSI (actually, VLSI's predecessor in interest, Freescale). J.A. 1662, 3461–62. Multiplying the VLSI figure by the incremental revenue gave the reasonably royalty. J.A. 1662–64, 3461–62, 15301–03. The net result was a proposed royalty of $1,611,609,964. J.A 15303. The jury awarded $1.5 billion. J.A. 13.

C

Intel challenges several aspects of the foregoing analysis, but it suffices for vacatur of the award that, in

determining the power savings attributable to use of the '373 patent, Dr. Annavaram made a readily identifiable error. The step at issue departed from the essential logic of the value-of-the-patented-technology assessment. It is not a matter of choosing one reasonable step over another or of estimation in the face of acceptable imprecision or uncertainty.

VLSI's damages model required VLSI to calculate the incremental technical benefit attributable to Intel's infringement. For the '373 patent, Dr. Annavaram purported to calculate this benefit by calculating the power-savings benefit attributable to the accused processor function of using the multiplexer to change the source of voltage to the C6 SRAM (allowing all cores to go to sleep without loss of re-startup data, thereby saving power)—what the parties before us call using the C6 SRAM. J.A. 1557–58. It is undisputed that when Intel's accused microprocessor enters the Package C7 sleep state, in which all cores are asleep, that function is performed (the C6 SRAM is used), but that it is not performed when Intel's accused microprocessor enters the Core C7 sleep state, in which individual cores are asleep. J.A. 1559–60. Thus, Core C7 and Package C7 are different states, and only the latter reflects the benefits of the infringement at issue. Nevertheless, Dr. Annavaram made use of Core C7 state residency data—data on how much time a processor spends in a given state—in making a choice of inputs into his calculation.

Specifically, he ran experiments on six Intel devices, two with accused Broadwell processors (the other four not accused of infringement of the '373 patent), to collect data on the residency of the devices in particular states when he put them through selected workloads. He compiled the results in a table, one line of which showed residency in the Core C7 state, while another line residency in the Package C7 state. *See* J.A. 3132–33. The residency figures for the former (where any core is shut down, J.A. 18670–71) were close to double those of the latter (where all cores are shut

down, J.A. 18671–72). Then, in the next stage of his analysis, which was to employ an Intel analytic tool (Power Model) that estimates power use (and hence power savings) under specified conditions (including residency and workload), Dr. Annavaram used at least the Core C7 figures, and perhaps also the Package C7 figures, in carrying out some kind of "match[ing]" process in order "to select the residency and workload settings in the Intel Power Model." J.A. 1580–81; *see* J.A. 1533–34, 1555–61, 3137–41.[3]

The results of using the Power Model with the selected inputs were the power savings that were crucial to VLSI's damages calculation. Yet to produce the power-savings results, Dr. Annavaram used inputs that he chose by trying to match (only or in part) data not from use of infringing functionality. That step undermines the reliability of the results as a calculation of power savings from use of the infringing functionality.

We cannot say that this error "could not have changed the result," namely, the precise amount of damages, so as to render it harmless. *See* Wright & Miller § 2886; *Voda v. Cordis Corp.*, 536 F.3d 1311, 1328 (Fed. Cir. 2008); *CytoLogix Corp. v. Ventana Medical Systems, Inc.*, 424 F.3d 1168, 1174 (Fed. Cir. 2005); *Ecolab, Inc. v. Paraclipse, Inc.*, 285 F.3d 1362, 1374 (Fed. Cir. 2002). The difference between the Core C7 residency data and the Package C7 residency data is on its face significant—75.86% and 75.95% for the Core C7 state versus 41.01% and 57.49% for the Package C7 state. J.A. 3132. Residency in particular states matters to the power savings, *see* J.A. 3138, and residency inputs chosen in an effort to match non-infringing-

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[3] Dr. Annavaram stated at least once that the Core C7 state was "the one" state he used from his experiment-results table. J.A. 1579–81. The problem we identify exists even if Dr. Annavaram used that state along with the Package C7 state (or others).

state numbers (at least in part) could well affect the bottom line. *See also* J.A. 1975–76, 1994 (testimony of Intel's expert, Dr. Sylvester). On this record, we cannot deem this step in the damages calculation harmless as to the bottom-line amount of damages. The damages award must be set aside, without our adjudicating Intel's other allegations of error bearing on the damages.

D

The proper relief is a remand for a new trial on the issue of damages. We see no sound basis, given the nature of the error found or of the other errors alleged, for denying VLSI an opportunity to provide a corrected damages case. Nor do we see a sound basis, in the error found or the other errors alleged, for setting aside the liability verdict as infected by the damages verdict.

We do not address Intel's other allegations of error in VLSI's damages case, except to state the following, which bears on what should occur on remand. First, Intel challenges VLSI's introduction of certain concededly noncomparable licenses in the trial, which were not part of the experts' damages calculation described *supra*. Given the conceded noncomparability, the law restricting use of noncomparable licenses, *see supra* p. 22, would clearly bar admission of that evidence unless admission of the evidence could be justified on the ground—which VLSI urges here and which we read the district court as having adopted—that the evidence was a proper response to Intel's presentation, through cross-examination of VLSI's expert, of prices at which certain sports teams were sold. *See* J.A. 2328–29; J.A. 17. The Intel line of questioning was allowed over VLSI's objection and unavoidably conveyed a message of relevance of the sheer size of the proposed award, through facts (about sports teams) self-evidently unconnected to the question of the value of the specific technology at issue. We do not decide whether VLSI's evidence of noncomparable licenses, itself focusing only on sheer size

(in VLSI's case, of license payments Intel made for other technology), could be admitted as a response to Intel's presentation. And we need not do so. We expect that, on remand, there will be no recurrence of comparable references, to sports-team prices or other facts about size of a proposed award alone (one way or the other), not focused on answering the question of the value of the specific technology at issue.

Second, we similarly do not adjudicate the merits of Intel's other challenges to VLSI's damages-calculation methodology. We note only this: Intel, in this court, has not persuasively shown that the regression analysis used to determine price effects of speed improvements is an improper or unreasonable one, and VLSI has not adequately elucidated how the last-step cost-and-contribution analysis (*see supra*, section III.B) reasonably establishes the choice Intel and VLSI would have made in the hypothetical negotiation about the sharing of the incremental benefits of implementation of the patent technology. On remand, the opportunity to provide better explanations should be made available.

IV

We address, finally, Intel's license defense.

On September 4, 2020, as the case was approaching trial (which began in late February 2021), Intel filed a motion to stay the litigation, arguing that it had newly acquired a license defense to the alleged infringement. Intel alleged that it had a license to practice VLSI's asserted patents because, as relevant, (a) in 2012, Intel entered into an agreement with Finjan, in which Finjan granted Intel a perpetual and irrevocable license to patents owned and controlled by Finjan's "affiliates" and (b) in July 2020, Fortress acquired "control" of Finjan, through funds Fortress manages, making VLSI and Finjan "affiliates" under the license agreement. J.A. 3005–06; *see* J.A. 65–66. On November 10, 2020, Intel filed the motion now at issue: It

sought leave to amend its answer in this case to add the license defense, and it requested that the defense be severed from the rest of the case and its adjudication stayed. J.A. 3635–36. The district court ruled on the motion only after trial, denying it on March 18, 2022. J.A. 65. We now reverse that denial.

The license agreement invoked by Intel was entered into on November 20, 2012, between Intel, on one side, and Finjan Software, Inc. and Finjan, Inc., on the other, and in the license agreement "Finjan" granted to Intel a broad license to "Finjan's Patents." J.A. 3684–96. The license agreement defines "Finjan" as Finjan Software, Inc., Finjan, Inc., and their "Affiliates"; it defines "Affiliates" as "any Person that, now or hereafter, directly or indirectly through one or more entities, controls or is controlled by, or is under common control with" "Finjan"; and it defines "control" to mean "the possession, direct or indirect, of the power to direct the management and policies of a Person, whether through the ownership of any percentage of voting interests of such Person, through contract or otherwise." J.A. 3684. The license agreement also broadly defines "Finjan's Patents" as "all Patent Rights that are owned or controlled at any time on or after November 6, 2012[,] by Finjan." J.A. 3685. Intel alleged that on July 24, 2020, Fortress "funds acquired Finjan, Inc., causing Finjan and VLSI to be under the common control of Fortress, and therefore 'affiliates' under the provisions of the license." J.A. 3635.

Addressing Intel's motion, the district court applied the four-factor approach set forth in *Meaux Surface Protection, Inc. v. Fogleman*, 607 F.3d 161, 167 (5th Cir. 2010), considering (1) the explanation for the failure to timely move for leave to amend; (2) the importance of the amendment; (3) potential prejudice in allowing the amendment; and (4) the availability of a continuance to cure such prejudice. J.A. 67–72. The district court denied the motion on the grounds

of untimeliness, prejudice, and—most significantly—unimportance because of the futility of the defense. *Id.*

We follow regional circuit law in reviewing the denial of a motion to amend, *Healthier Choices Management Corp. v. Philip Morris USA, Inc.*, 65 F.4th 667, 675 (Fed. Cir. 2023), and Fifth Circuit law provides for review here for abuse of discretion, *Meaux*, 607 F.3d at 167. A district court abuses its discretion if it bases its ruling on an erroneous view of the law or on a clearly erroneous assessment of the evidence. *Cooter & Gell v. Hartmarx Corp.*, 496 U.S. 384, 405 (1990). We find such an abuse of discretion.

We conclude that the district court's conclusion that Intel unduly delayed filing its motion—between the time of the July 24 acquisition and the filing of the November 10 motion—was an abuse of discretion. Intel was required by the 2012 license agreement to follow certain procedures, J.A. 3694, and Intel acted with diligence in doing so. On August 17, 2020, in accordance with the process requirements, Intel sent a letter to Finjan, VLSI, and Fortress stating that Intel holds a license to VLSI's patents under the 2012 Intel-Finjan license agreement and that Intel would like to begin the dispute resolution process. J.A. 3018. Then, on September 2, 2020, Intel filed its motion to stay in light of the new license defense. J.A. 3001. This motion to stay was in accordance with the contract's choice of law and venue provisions. J.A. 3696. VLSI opposed the motion on September 18, 2020, *see* J.A. 156, and when the district court had not ruled by early November, Intel filed the motion now at issue on November 10, 2020, stating that it moved to amend its answer "[t]o avoid any doubt that Intel has preserved its defense of license in this case." J.A. 3635. Considering timing alone, we see no reasonable basis for a determination of undue delay.

Regarding prejudice, the district court, which expressly considered its futility conclusion in addressing this factor, did not conclude that, even if the defense was meritorious,

it would deny the motion because of prejudice to VLSI alone. J.A. 71. And we see no basis on which prejudice alone could support denial of the motion. Intel requested severance of the defense from the rest of the case and a stay of its adjudication, so trial of the other issues was not to be delayed. Although entry of a final judgment in the district court for appeal might have been delayed, the district court said nothing about how long such a delay would have been. The court said that having a district court judgment sooner rather than later (subject to appeal) would help VLSI secure licenses, but it offered no basis for that conclusion that is independent of the merits of the defense. Nor did the district court consider that it was Fortress (with its close relationship to VLSI), not Intel, that was responsible for the action creating the possibility of the license defense: "Fortress acquired Finjan," J.A. 70. The district court considered relevant to the prejudice factor Intel's interest in not being liable if its defense is valid, but it dismissed that interest only by an unelaborated reference to the possibility of a contract action by Intel against Finjan as an alternative remedy for Intel, without explaining why that was a meaningful avenue (legally or practically) for recovering from Finjan the damages Intel would pay in this case (incorrectly if the license defense was valid). For such reasons, we see no basis on which, futility aside, prejudice could sustain the denial of Intel's motion.

What is determinative, then, is the soundness of the district court's conclusion that the record developed makes the license defense so clearly meritless that allowing it even to be pleaded is a futile act. We hold that conclusion to be wrong as a matter of law. This is a very narrow holding. We do not conclude that the license defense is meritorious. We conclude only that the governing law is such that the defense requires additional litigation of the sort that begins once it is added to the case, whether that process is a fully developed motion to dismiss, with fuller analysis of the governing law than has yet occurred, or more fact-

based litigation. Intel might well fail to sustain the defense, but we do not see failure as foreordained on the material supplied to date.

The district court turned to Delaware law, which, subject to any overriding federal law, is the applicable law chosen by the 2012 license agreement. J.A. 3696. The district court stated, without qualifiers, that "Delaware law provides that a non-party to a contract is not bound by that contract." J.A. 70. But the precedential authority cited in support states the principle as only "the ordinary rule," subject to exceptions for "unusual circumstances." *Alliance Data Systems Corp. v. Blackstone Capital Partners V L.P.*, 963 A.2d 746, 760 & n.47 (Del. Ch. 2009), aff'd, 976 A.2d 170 (Del. 2009) (footnote quoting statement from *Wallace ex rel. Cencom Cable Income Partners II, Inc., v. Wood*, 752 A.2d 1175, 1180 (Del. Ch. 1999), that this is "a general principle"). Three cited nonprecedential decisions are to the same effect. *Sheehan v. AssuredPartners, Inc.*, No. 2019-0333-AML, 2020 WL 2838575, at *9 (Del. Ch. May 29, 2020) ("'ordinary rule,'" quoting *Alliance Data*, 963 A.2d at 760–61); *Wenske v. Blue Bell Creameries, Inc.*, No. 2017-0699-JRS, 2018 WL 5994971, at *3 (Del. Ch. Nov. 13, 2018) ("ordinarily"); *Kuroda v. SPJS Holdings, L.L.C.*, No. 4030-CC, 2010 WL 4880659, at *3 (Del. Ch. Nov. 30, 2010) ("[g]enerally").

In 2019, the Delaware Supreme Court stated that "[c]ontracts may impose obligations on affiliates" in certain contexts, and it affirmed the Delaware Chancery Court's determination that the case before it involved such a context. *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, 213 A.3d 39, 57 (Del. 2019). In so ruling, the Delaware Supreme Court cited, *id.* at 57 n.86, two nonprecedential decisions of the Delaware Chancery Court that are to the same effect, describing them as involving contract provisions covering certain affiliates and non-signatories who were, or came to be, owned or under the control of a signatory party. *Medicalgorithmics S.A. v. AMI*

Monitoring, Inc., No. 10948-CB, 2016 WL 4401038, at *18 (Del. Ch. Aug. 18, 2016); *MicroStrategy Inc. v. Acacia Research Corp.*, No. 5735-VCP, 2010 WL 5550455, at *12 (Del. Ch. Dec. 30, 2010).

This case law does not definitively enough answer questions of potential significance here to make the license defense proposed by Intel futile. Perhaps it makes a difference whether the affiliate sought to be bound was an affiliate at the time of contract or whether it controlled or was controlled by the signatory, rather than merely under common control, even when the contractual definition of "affiliate" includes the common-control situation. Under the authorities presented and arguments made on whether VLSI, as a non-party, could be bound by the 2012 license agreement, we do not think that there is a sufficiently clear answer for there to be a determination of futility. *See Stripling v. Jordan Production Co., LLC*, 234 F.3d 863, 872–73 (5th Cir. 2000).

In so concluding, we do not prejudge the answer to that question or the answer to other questions about whether VLSI's particular circumstances bring it within the contract's terms. Nor do we prejudge the appropriate processes for deciding the merits of the license defense, *e.g.*, whether a motion to dismiss may suffice, whether discovery is warranted, or whether summary judgment may be justified. Nor do we prejudge whether certification of a legal question to the Delaware Supreme Court is appropriate or whether any federal patent-law question is involved. *See*, *e.g.*, 35 U.S.C. § 261. We hold only that it was error to deny the motion to add the license defense to the case.

V

The judgment of infringement of the '373 patent is affirmed. The judgment of infringement of the '759 patent is reversed. The damages award for the '373 patent is vacated. The denial of the motion for leave to amend is

reversed. The matter is remanded for further proceedings consistent with this opinion.

The parties shall bear their own costs.

AFFIRMED IN PART, REVERSED IN PART, VACATED IN PART, AND REMANDED

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February 2, 2024