2022-1292

United States Court of Appeals for the Federal Circuit

In re: CELLECT, LLC,
Appellant,

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in *Ex Parte* Reexamination Control No. 90/014,452

OPENING BRIEF FOR APPELLANT CELLECT, LLC

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PATENT CLAIM AT ISSUE PURSUANT TO FED. CIR. R. 28(A)(12)

U.S. Patent No. 6,982,740

1. A reduced area imaging device comprising:

an image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a first circuit board lying in a second plane and communicating with said image sensor by at least one pre-video conductor inner-connecting said image sensor and said first circuit board, said first circuit board including circuitry means for converting said pre-video signal to a post-video signal for reception by a standard video device;

a power supply coupled with said image sensor for driving said array of pixels and said timing and control means, and electrically coupled to said first circuit board for driving said first circuit board; and

a time select switch electrically communicating with said first circuit board and remote from said first circuit board for selectively varying integration periods to produce an image of a desired brightness, said switch having a plurality of settings enabling selective control to produce the image of a desired brightness.

2. A device, as claimed in claim 1, wherein:

said array of pixels includes an array of CMOS pixels.

CERTIFICATE OF INTEREST

Counsel for Appellant Cellect, LLC certifies the following:

1. The full name of every party represented by us is:

Cellect, LLC

2. The name of the real party in interest represented by us is:

None.

3. All parent corporations and any other publicly held companies that own 10 percent or more of the stock of the party:

Micro-Imaging Solutions LLC

4. The names of all law firms and the partners or associates that appeared for Cellect, LLC before the Patent Trial and Appeal Board or are expected to appear in this court (and who have not or will not enter an appearance in this case) are:

None.

5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal:

- *In re: Cellect, LLC*, Nos. 22-1293, -1294, -1295, -1296 (Fed. Cir.); *Cellect, LLC v. Samsung Electronics Co., Ltd., et al.*, No. 1:19-cv-00438-CMA-MEH (D. Co.).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6):

Not applicable.

Dated: May 2, 2022

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Cellect, LLC, states that:

(1) no appeal other than the current appeal has been taken in or from the United States Patent and Trademark Office, Patent Trial and Appeal Board's decision in *Ex Parte* Reexamination Control No. 90/014,452;

(2) Cellect, LLC is a party to *In re: Cellect*, 22-1293 (LEAD), 22-1294, 22-1295, 22-1296 (Fed. Cir.); *Cellect, LLC v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.*, 22-1100 (LEAD), 22-1101, 22-1272, 22-1273 (Fed. Cir.). Lead appeals 22-1100, 22-1292 and 22-0293 are considered companion cases and assigned to the same merits panel. Dkt. No. 5.

(3) the following case may be directly affected by the Court's decision in this appeal: *In re: Cellect, LLC*, Nos. 22-1293, -1294, -1295, -1296 (Fed. Cir.); *Cellect, LLC v. Samsung Electronics Co., Ltd., et al.*, No. 1:19-cv-00438-CMA-MEH (D. Co.).

JURISDICTION

The Patent Trial and Appeal Board (the "Board") issued on December 1, 2021, a Decision on Appeal in Reexamination Control No. 90/014,452 ("the '452 Board Decision") (Appx1-28). Patent Owner, Cellect, LLC, timely filed a Notice of Appeal on December 21, 2021 (Appx1272-1277). This Court has jurisdiction over this appeal pursuant to 28 U.S.C. § 1295(a)(4)(A).

INTRODUCTION

The ’740 Patent describes and claims reduced area (i.e., small) imaging devices, including techniques for improving the quality of images produced by the devices and making the devices smaller. Two important aspects of asserted claims 1 and 2 of the ’740 Patent (i.e., the “Asserted Claims”) include (i) a “time select switch . . . for selectively varying integration periods” that allows a user to select the amount of time an image receiver collects light (i.e., the integration period) in order to enhance the brightness of an image; and (ii) that the time select switch, in order to assist in reducing the size of the overall imaging device, is remote from other processing circuitry (for example, circuitry that relates to processing the image for video display). The Board’s analysis in the final decision below fails to account for either of these key aspects of the Asserted Claims. As a result, the Board’s decision should be reversed.

The Board’s error is two-fold. First, the Board erred by construing the term “time select switch . . . for selectively varying integration periods” as not requiring the associated circuitry that functions to allow the variation of integration periods. It is this function, however, that makes the switch the claimed “time select switch,” as opposed to any other generic switch or knob (akin to, for example, a light switch that merely turns a circuit on or off). Second, the Board compounded its error by using this erroneous flawed construction in its obviousness analysis. Because the

Board determined that any generic switch may constitute the claimed "time select switch . . . for selectively varying integration periods," it concluded that a simple knob from a prior art reference (i.e., the *Tomoyasu* reference, described in detail below) satisfied the claim element, notwithstanding that the knob does not include the circuitry that allows for the variation of integration periods and, when properly construed, is not remote from the first circuit board, as required by the Asserted Claims.

STATEMENT OF THE ISSUES

1. Did the Board err by disregarding the plain meaning of the claims in light of the claim language and specification that require the claimed "time select switch . . . for selectively varying integration periods" to include the circuitry that performs the function of varying integration periods (which is what makes the switch a "time select switch . . . for selectively varying integration periods")?

2. Did the Board err by applying its flawed construction of the "time select switch" term to its obviousness analysis, which resulted the Board rejecting the Asserted Claims based on a reference that does not include a "time select switch . . . for selectively varying integration periods" that also is remote from a first circuit board as required by the Asserted Claims?

STATEMENT OF THE CASE AND FACTS

This appeal is taken from the Decision on Appeal regarding the *ex parte* review ("EPR") of U.S. Patent No. 6,982,740 ("the '740 Patent") (Appx36-64) in Reexamination Control No. 90/014,452. Appx1-28 (the "Decision"). Appellant Cellect, LLC ("Cellect") appeals the Board's Decision affirming the final rejection of Claims 1 and 2 of the '740 Patent on the ground of non-statutory, obvious-type double patenting, including the Board's construction of the terms in the Decision and the Board's conclusions regarding statements made during *inter partes* review ("IPR") proceedings.

I. BACKGROUND OF THE '740 PATENT

The '740 Patent specification describes reduced area imaging devices (for example, an imager for a small diameter endoscope used to view a particular surgical area) that uses variable charge integration periods and configured for minimum size. Appx54 ('740 Patent at 1:20-23, 27-34). The charge integration period generally refers to the amount of time light is collected by pixels in the image sensor, which can enhance the quality of an image.

Important for purposes of this appeal, the '740 Patent discloses and claims an imaging device including (i) a remote time select switch that allows a user to selectively vary integration periods in order to enhance brightness or intensity of an image, and (ii) using techniques for customizing the form factor (e.g., the

configuration, shape, and size) of the imaging sensor device to reduce its profile. Appx36 ('740 Patent at Abstract).

A. The Asserted Claims Recite a Remote Time Select Switch with the Function of Varying Integration Periods

Each of the Asserted Claims requires a reduced area imaging device with a remote "time select switch . . . for selectively varying integration periods to produce an image of a desired brightness." Appx63-64 ('740 Patent at Claims 1, 2). The function of the claimed time select switch is to allow the user to vary the integration period, which permits greater amounts of light to be collected by the pixels, to produce a better quality image – for example, by overcoming low light conditions. Appx56 ('740 Patent at 5:35-6:61).

Indeed, the Asserted Claims expressly recite a "remote" time select switch to produce "an image of a desired brightness" that has "a plurality of settings enabling selective control to produce the image of desired brightness." Appx63-64 ('740 Patent at Claims 1, 2). The '740 Patent specification describes how the time select switch's variation of the integration period can be used to improve the brightness of an image:

- "For each of the embodiments, selected charge integration periods may be used to enhance the image to a desired brightness or intensity." Appx56 ('740 Patent at 5:28-34);

- Describing types of image sensor devices that "can be modified to include an imager integration time select switch which allows an operator to preselect a desired integration period which maximizes observable fluorescence." Appx56 ('740 Patent at 5:54-6:43);
- "As seen in FIG. 9, the intensity or brightness of an image may be enhanced by a CMOS-CID imager which has a variable charge integration capability." Appx62-63 ('740 Patent at 18:49-19:36).

Importantly, the '740 Patent describes the remote time select switch for selectively varying integration periods as including circuitry required for the user to select the integration period. Appx63 ('740 Patent at 19:42-45) ("In order to incorporate variable charge integration capability, imager readout clock select circuitry 318 is added which communicates with one or more of the video processor boards 50."). For example, Figure 10 describes an imager and its processing circuitry that incorporates variable charge integration capability. *Id.* ('740 Patent at 19:37-39). As depicted, the knob for the "imager integration – time select switch" (320) includes the "imager readout clock select circuitry" (318) that is necessary to "incorporate variable charge integration capability." *Id.* ('740 Patent at 19:37-57), Appx53 at Fig. 10. Additionally, Figures 4 and 4a depict the imager and "timing and control circuits," which also are remote from the video processor and operate with the time select switch, inlcuding circuitry 318, to release an image before the

integration period is complete. Appx63 (’740 Patent at 19:21-28). The time select switch requires circuitry 318 to provide the ability to control and generate different timing signals that allow a user to select the integration time and desired brightness as shown in Figure 9. Appx41-42, Appx52 (’740 Patent at Figs. 4, 4a, 9), Appx63 at 19:41-45.

The ’740 Patent further describes different types of common imaging devices including: charged coupled devices (CCD), charge injection devices (CID) and complementary metal oxide semi-conductors (CMOS). Appx54 (’740 Patent at 1:44-52). Because the imaging device of the ’740 Patent is capable of enabling a user to select an integration period to enhance an image to a desired level of brightness using various configurations, it is referred to in the specification as a CMOS-CID device. Appx36 (’740 Patent at Abstract), Appx 56 at 6:26-43. As explained in the ’740 Patent, a CMOS-CID imaging device allows a user to see (i.e., read out) the image while the sensor continues to collect photons until an image with a desired brightness is achieved. *Id.*

This approach in the ’740 Patent is different from other types of imaging devices, including CCD devices, that are not capable of the claimed varying integration periods. Rather, those devices employ, for example, a “destructive readout” where multiple images must be taken while the user continuously adjusts the integration time until the desired brightness is found. Appx56 (’740 Patent at

5:35-65). In other words, an image is taken without knowing if it has the desired brightness, and the integration time is varied through a trial and error process that may or may not result in the image achieving the desired brightness. The '740 Patent describes this significant drawback overcome by the Asserted Claims. *Id.*

- "Most commonly available fluorescence microscopes include CCD type imagers which are not capable of the variable charge integration." Appx56 ('740 Patent at 5:38-41);
- "Because of the construction of CCD devices, these exposure times cannot be manipulated for charge integration because CCD imagers have destructive readout." *Id.* ('740 Patent at 5:44-65);
- Describing that CCD devices do not provide the same benefit of CMOS-CID devices that allow for continued integration and monitoring to produce an image of a desired brightness. Appx63 ('740 Patent at 19:9-26).

Thus, the claimed remote time select switch for selectively varying integration periods includes circuitry that allows the user to vary the charge integration period.

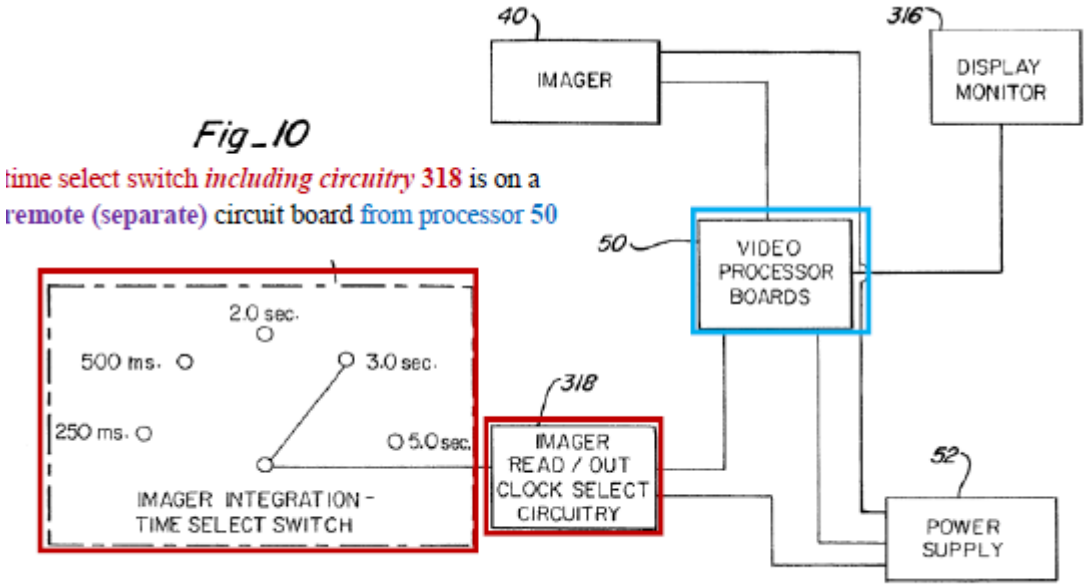
B. The Asserted Claims Recite a Time Select Switch and Circuitry that is Remote from Other Video Processing Circuitry

The Asserted Claims also uniquely separate various components of the claimed reduced area imaging device, including that the claimed time select switch for selectively varying integration periods, which includes the aforementioned

processing circuitry, must be remote from the "first circuit board." Appx63-64 ('740 Patent at Claims 1, 2). The "first circuit board" includes, for example, the circuitry and components related to video processing. *Id.* ("said first circuit board including circuitry means for converting said pre-video signal to a post-video signal for reception by a standard video device").

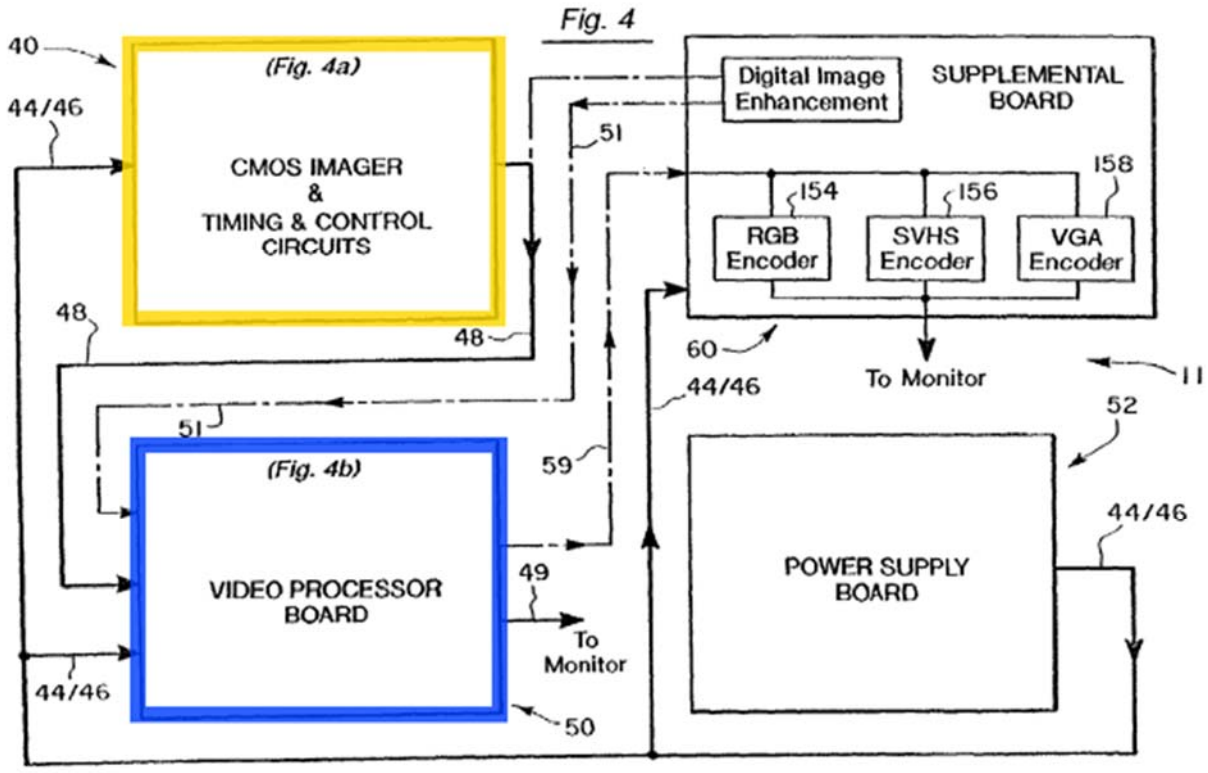
The '740 Patent is replete with descriptions confirming that the time select switch for selectively varying integration periods must be remote from the video processing circuitry – including the explicit language of the Asserted Claims: "***time select switch*** electrically communicating with said first circuit board ***and remote from said first circuit board*** for selectively varying integration periods to produce an image of a desired brightness, said switch having a plurality of settings enabling selective control to produce the image of a desired brightness." Appx64 ('740 Patent at Claims 1, 2) (emphasis added).

In addition, Figure 10 (included below with color and text added) depicts "an imager and its processing circuitry" that incorporates the variable charge integration capability. Appx63 ('740 Patent at 19:37-39). The specification specifically describes the "imager readout clock select circuitry" (318) that is necessary to "incorporate variable charge integration capability" as included with the "imager integration – time select switch" (320) and is illustrated in Figure 10 as separate from the "video processor boards." Appx63 ('740 Patent at 19:37-57).



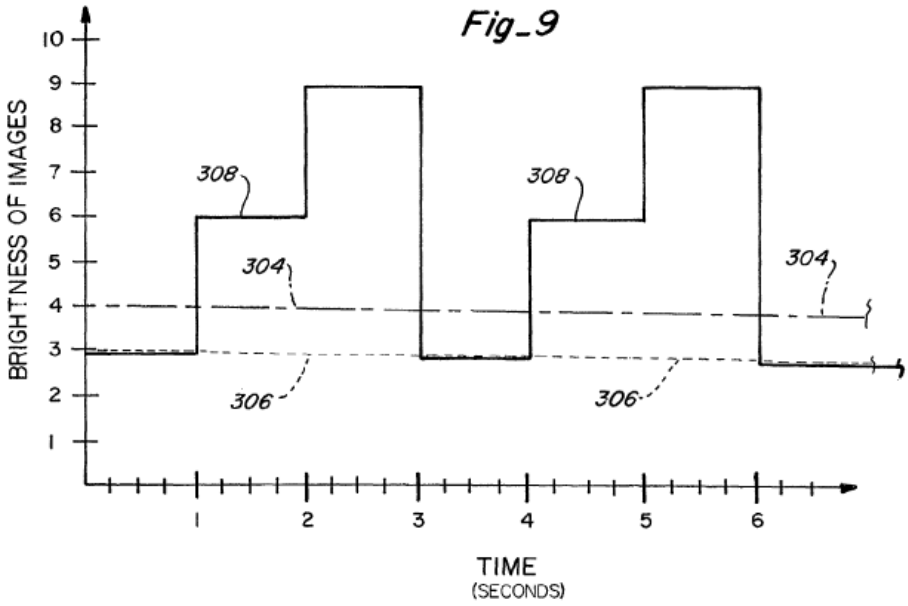
Appx53 ('740 Patent at Fig. 10) (highlighting and text added).

Moreover, Figures 4 and 4a depict the "CMOS Imager & Timing & Control Circuits" (4a) (shown in yellow highlighting below) (which include timing and control circuitry) that are controlled by the time select switch shown in Figure 10 when the variable charge integration capability is implemented. Appx41-42, Appx53 ('740 Patent at Figs. 4, 4a, 10), Appx63 at 19:37-53. Here again, the timing and control circuitry controlled by the time select switch, which requires circuitry 318 as described above is shown and described as being remote from from the "Video Processor Board" (4b) (shown in blue highlighting below):



Appx41-42 ('740 Patent at Figs. 4, 4a) (highlighting added), Appx63 at 19:37-52.

Moreover, the time select switch requires circuitry 318 to select the integration time which then generates a signal shown in Figure 9 (copied below) used by the timing and control circuitry shown in Figure 4 and 4a, which are remote from the video processing. The signal is used by timing and control circuits shown in Figure 4a to release or dump the image at the end of the integration period and also at intermediate points, so that the image can be shown on a monitor until the desired brightness is achieved. Appx63 ('740 Patent at 19:17-52). The ability to display images at intermediate points with increasing brightness are shown in Figure 9 (copied below) as a "stepped" pattern.



Appx52 ('740 Patent at Fig. 9).

Thus, the '740 Patent discloses a time select switch for selectively varying integration periods and circuitry that is remote from the first circuit board including video processing circuitry.

C. Cellect's Statements During *Inter Partes* Review

In addition to this reexamination proceeding, Cellect submitted a preliminary response during an *inter partes* review ("IPR") proceeding regarding the '740 Patent (i.e., IPR2020-00474). There, Cellect noted that in a pending district court action it proposed the following construction for the term "time select switch": "feature for selectively varying integration periods to produce an image of desired brightness." Appx1209-1210 (3/11/2021 Second Advisory Action at 2-3).

The Examiner in this reexamination proceeding noted that Cellect's arguments during IPR explicitly included that (i) "a POSITA would understand that the '740 Patent describes a remote switch, including circuitry that can be used to select a desired frequency, for selectively varying integration periods to produce an image of a desired brightness" and (ii) "the '740 Patent explains that the time select switch 45 cannot work without the readout clock select circuitry 318." Appx1247 (6/10/2021 Examiner's Answer at 7). Thus, Cellect's positions remained consistent among the district court, IPR and re-examination proceedings—namely, that the time select switch includes the circuitry that permits variation of integration periods (i.e., circuitry 318).

The Examiner, however, disregarded Cellect's arguments and found that Cellect's proposed construction did not "state that the claimed 'time select switch' cannot work without 'readout clock select circuitry.'" Appx1249 (6/10/2021 Examiner's Answer at 9). The Examiner also determined that because the Asserted Claims are not governed by a means-plus-function interpretation, then the claimed time select switch does not include the readout clock select circuitry 318 as described in the specification. *Id.*

D. The Examiner Misapplied Its Erroneous Construction of the Time Select Switch Term in its Obviousness Analysis

In rejecting Claims 1 and 2 of the '740 Patent, the Examiner misapplied its erroneous construction of the "time select switch . . . for selectively varying integration periods" term.

In particular, the Examiner rejected the Asserted Claims on the ground of non-statutory, obviousness-type double patenting ("OTDP") as being unpatentable over Claim 1 of Cellect's related patent (i.e., U.S. Patent No. 6,043,839) in view of Japanese Patent Publication No. JP H07275198 to Tomoyasu et al. ("*Tomoyasu*") (Appx1772-1799).

Notably, the Examiner in its First Advisory Action agreed with Cellect that the claimed time select switch required the associated circuitry (i.e., the imager readout clock select circuitry 318) and, as a result, determined the Asserted Claims were not obvious in view of *Tomoyasu*. Appx1182-1183. After receiving the First Advisory Action, Cellect cancelled a different claim that is not at issue on this appeal (i.e., Claim 13 which was not indicated as allowable in the First Advisory Action) in order to expedite issuance of an *Ex Parte* Reexamination Certificate for the '740 Patent. Appx1199-1200. However, with no triggering action by Cellect, the Examiner reversed course after Cellect cancelled Claim 13, applying a different construction and reinstated the rejection of Claims 1 and 2 in the Second Advisory Action. Appx1209-1210.

The Examiner's final rejection misapplied its flawed construction of the time select switch term. First, the Examiner determined that the Asserted Claims do not require that the time select switch itself include the circuitry (i.e., the readout clock circuitry 318) to vary integration periods, but rather that the switch is used to allow an operator to manually select the desired the integration period and other components will perform any required operation. Appx1142 ("The examiner maintains that the specification does not say that the switch itself produces an image or maximizes a brightness. Rather, the switch is simply a switch. There is no disclosed processing that occurs within the switch."). Applying this erroneous construction, the Examiner determined that the control knob in *Tomoyasu*, which is just a knob with no supporting circuitry for varying the integration periods, satisfies the time select switch because it is used to indicate the operators desired setting. Appx1142-1143.

Second, because the Examiner construed the "time select switch . . . for selectively varying integration periods" term as not requiring the performance of actually varying integration periods, he determined that the control knob of *Tomoyasu* satisfies the "remote" requirement of the claim language. Appx1143 (11/23/2020 Final Rejection at 8). Using that reasoning, the Examiner disregarded that the circuitry that actually performs the varying of the integration period in

Tomoyasu is not remote from the first circuit board—as required by the claim —but actually resides on the first circuit board. *Id.*

E. The Board's Decision on Appeal

The Board upheld the Examiner's rejection of Claims 1 and 2. First, the Board did not construe the Asserted Claims to require variable integration control circuitry as part of the claimed "time select switch . . . for selectively varying integration periods." Appx22-23. According to the Board, the sole function performed by circuitry 318 is basic communication signaling and, therefore, the Board declined to read circuitry 318 into the claim language. *Id*.

The Board upheld the Examiner's determination that Cellect somehow took an inconsistent between the IPR and reexamination proceedings because Cellect's proposed construction in the IPR proceeding purportedly did not include "circuitry 318." Appx18. The Board, however, failed to address Cellect's argument, detailed above, that consistently asserted that the claimed time select switch includes the readout clock select circuitry 318.

Second, using this flawed construction, the Board determined that various components of *Tomoyasu* that constitute the time select switch are both remote from the first circuit board and contain supporting circuitry for varying the integration periods. Appx24.

SUMMARY OF THE ARGUMENT

First, the Board erred in construing the claimed "time select switch. . . for selectively varying integration periods" as not requiring the circuitry that performs the variation of interval periods (i.e., circuitry 318). Appx22-24. The Board's construction is contrary to the plain language of the claims, which require a time select switch "for selectively varying integration periods to produce an image of desired brightness" and "having a plurality of settings enabling selective control to produce the image of a desired brightness." Appx64 ('740 Patent at Claims 1, 2). The Board's error is apparent because the claims require the time select switch to be more than just a simple switch, but to actually perform the expressly recited function of selectively varying integration periods to achieve a desired image brightness.

Contrary to the Board's finding, nothing in the IPR proceedings—including Cellect's proposed construction of the time select switch term—contradicts its position in this reexamination that the "time select switch . . . for selectively varying integration periods" includes the circuitry that allows for the varying of integration periods. Rather, Cellect consistently maintained that a time select switch is more than just a simple switch or knob, but must include circuitry or feature for selectively varying integration periods to produce an image of desired brightness. There is no basis to reject the Asserted Claims based on this purported inconsistency—which, as explained herein, does not exist.

Second, the Board compounded its error by applying its incorrect construction to its obviousness analysis. Because the Board found that a simple knob that does not contain circuitry to perform integration period variation satisfies the claimed time select switch limitation, it determined that the simple knob in *Tomoyasu* satsifed the claim requirement of being "remote" from the first circuit board. Appx24. Thus, the Board erred in finding obvious the remote time select switch limitation even though it mapped this limitation to circuitry in *Tomoyasu* that undisputedly resides on, and not remote from, the first circuit board as the claims require.

As a result, the Decision should be vacated.

ARGUMENT

I. THE BOARD ERRED BY CONSTRUING THE REMOTE TIME SELECT SWITCH AS NOT REQUIRING CIRCUITRY FOR VARYING INTEGRATION PERIODS

The Board erred by construing the "time select switch . . . for selectively varying integration periods" limitation to not include the associated circuitry that allows the selection of integration periods. Appx22-24. The Board's erroneous construction disregards the plain language of the Asserted Claims and the specification that require both the switch and circuitry that allows performance of the function in order for a switch to be a "time select switch." And it is the Board's construction, not Cellect's arguments, that cannot be reconciled with the IPR

proceedings insomuch as Cellect consistenly maintained that circuitry (318) is required in order for the claimed time select switch to function in the claimed manner. Appx63 ('740 Patent at 19:42-45).

A. Standard of Review – This Court Applies De Novo Review to Claim Constructions

This Court reviews without deference the Board's claim construction, which formed the basis for invalidating the '740 Patent. In particular, the Board's claim constructions are determinations of law reviewed *de novo* where based on intrinsic evidence, with any Board findings about facts extrinsic to the patent record reviewed for substantial-evidence support. *HTC Corp. v. Cellular Commc'ns Equip., LLC,* 877 F.3d 1361, 1367 (Fed. Cir. 2017) ("Claim construction is a question of law that may be based on underlying factual determinations.") (citations omitted). The Board applies the same claim construction standard as that applied in federal courts. 37 C.F.R. § 42.100(b) (2018); *see also Celgene Corp. v. Peter*, 931 F.3d 1342, 1349 n.8 (Fed. Cir. 2019) (noting the PTO changed the claim construction standard used in IPR proceedings to petitions filed on or after November 13, 2018). In this context, claim terms "are generally given their ordinary and customary meaning" as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.,* 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) (citations omitted).

B. The Plain Language of the Claims Confirm that the Time Select Switch Limitation Includes Associated Circuitry

The plain language of the Asserted Claims and the specification confirm that the remote time select switch includes the processing circuitry (i.e., 318) that allows for variation of integration periods. To construe the term otherwise, as the Board erroneously did here, results in any generic switch satisfying the claim regardless of whether it can perform the very function that makes a time select switch.

Claims 1 and 2 expressly recite that the time select switch selectively varies integration period to enhance the brightness of an image:

> - Claim 1: . . . ***a time select switch*** electrically communicating with said first circuit board and remote from said first circuit board ***for selectively varying integration periods to produce an image of a desired brightness***, ***said switch having a plurality of settings enabling selective control to produce the image of a desired brightness***.

Appx64 ('740 Patent at Claims 1, 2) (emphasis added).

The Board construed the time select switch term, however, to not require the associated circuitry. Appx22 ("We do not construe claim 1 to require integration control circuitry as part of the claimed time select switch."). This construction should be rejected because it is inconsistent with the plain language of the claim insomuch as it does not require the circuitry that enables a time select switch to vary integration periods, which is the very purpose of the time select switch as expressly recited in the claims. *Aventis Pharms. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363,

1373 (Fed. Cir. 2013) ("There is a heavy presumption that claim terms are to be given their ordinary and customary meaning.").

Indeed, the claimed time select switch actually contains six aspects set forth in the claim language: (i) electrically communicating with the first circuit board, (ii) remote from the first circuit board, (iii) for selectively varying integration periods, (iv) producing an image of desired brightness, (v) having a plurality of settings, and (vi) enabling selective control to produce the image of desired brightness. Appx63-64 ('740 Patent at Claims 1, 2).

The Board's construction does not give meaning to the "time select . . . for selectively varying integration periods" aspect of the "time select switch," but instead could replace the entire phrase with just a "switch." This is legal error because, as a matter of claim construction, each term in a claim should be given meaning. *St. Jude Med., LLC v. Snyders Heart Valve LLC*, 977 F.3d 1232, 1241 (Fed. Cir. 2020) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous. Claims are interpreted with an eye toward giving effect to all terms in the claim." (internal citations omitted)); *Akzo Nobel Coatings, Inc. v. Dow Chem. Co.*, 811 F.3d 1334, 1339-40 (Fed. Cir. 2016) (construction of "pressurized collection vessel" to mean a vessel that "receives" the dispersion was improper because it renders the term "collection" superfluous).

C. The Specification Confirms that the "Time Select Switch . . . for Selectively Varying Integration Periods" Limitation Includes Associated Circuitry

In addition to the key function feature of "selectively varying integration periods" being expressly recited in the Asserted Claims, the specification describes how the variation of integration periods by the time select switch enables improvement of an images brightness. Appx56 ('740 Patent at 5:28-34) ("For each of the embodiments, selected charge integration periods may be used to enhance the image to a desired brightness or intensity."); Appx62-63 ('740 Patent at 18:49-19:36), Appx52 at Fig. 9 ("As seen in FIG. 9, the intensity or brightness of an image may be enhanced by a CMOS-CID imager which has a variable charge integration capability.").

The specification further describes and depicts the time select switch as including the associated circuitry for performing the variation of integration periods. For example, the specification describes types of image sensor devices that "can be modified to include an imager integration time select switch which allows an operator to preselect a desired integration period which maximizes observable fluorescence." Appx56 ('740 Patent at 5:54-6:43), Appx41-42, Appx52-53 ('740 Patent at Figs. 4, 4a, 9, 10).

Figure 10 further depicts the "imager integration – time select switch" (320) that includes the "imager readout clock select circuitry" (318) that is necessary to

"incorporate variable charge integration capability." Appx63 ('740 Patent at 19:37-57), Appx53 at Fig. 10. Figure 4 also depicts the imager (40) which includes the time select switch as part of the "timing and control circuits" that are controlled by the time select switch showin in Figure 10 when the variable charge integration capability is implemented. Appx41-42, Appx53 ('740 Patent at Figs. 4, 4a, 10), Appx63 at 19:37-53.

Contrary to the Board's conclusion, including the processing circuitry (i.e., 318) in the construction of time select switch does not read limitations from the specification into the Asserted Claims. Appx22-23. Rather, the specification is entirely consistent with the plain language of the Asserted Claims and further details the scope of the claim. This Court routinely holds that claims should be given "an interpretation that is consistent with the specification." *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382-83 (Fed. Cir. 2017) ("The correct inquiry in giving a claim term its broadest reasonable interpretation in light of the specification . . . is an interpretation that corresponds with what and how the inventor describes his invention in the specification, *i.e.*, an interpretation that is consistent with the specification") (internal quotations and citations omitted); *accord Profectus Tech. LLC v. Huawei Techs. Co.*, 823 F.3d 1375, 1380 (Fed. Cir. 2016) ("[W]e first look to the actual words of the claims and then read them in view of the specification.") (citation omitted).

Because the Board's construction is inconsistent with the specification and claim language, it should be reversed. *On-Line Techs., Inc. v. Bodenseewerk Perkin-Elmer GmbH*, 386 F.3d 1133, 1138 (Fed. Cir. 2004) ("a claim interpretation that excludes a preferred embodiment from the scope of the claim is 'rarely, if ever, correct.'") (citations omitted); *Phillips*, 415 F.3d at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction").

Finally, the Board's statement that the circuitry 318 is "basic communication signal conditioning circuitry" is incorrect. Appx23-24. Figure 10 illustrates that that the "imager readout clock select circuitry" (318) is necessary to "incorporate variable charge integration capability" and to generate a signal shown in Figure 9. Appx63 ('740 Patent at 19:37-57), Appx52-53 at Figs. 9, 10. Nothing in the '740 Patent or the record demonstrates or even suggests that the claimed switch for selectively varying integration periods can be generated by a simple "switch."

Moreover, Figure 4 depicts the imager (which includes the time select switch when the variable charge integration capability is provided) as including "timing and control circuits" that operate with the time select switch to produce an image of a desired brightness. Appx41 ('740 Patent at Fig. 4). Additional structural elements regarding the timing and control circuitry are shown in Figure 4a, which include

"Clock Input," "Run," "Default," and "Data" signal processors. Appx42 ('740 Patent at Fig. 4a). These signal processors operate with readout circuitry (318) and are necessary to produce an image of a desired brightness and are remote from the processor board. Appx63 ('740 Patent at 19:16-31, 19:37-57). Thus, the Board is incorrect that basic and well-known circuitry satisfied this limitation and nothing in the recird supports that finding.

D. Cellect Consistently Maintained that the Time Select Switch Limitation Includes Associated Circuitry

Cellect consistenly maintained across all proceedings—whether in the district court, IPR or this re-examination proceeding—that the time select switch must include the circuitry that allows the variation of integration period. Indeed, in its Patent Owner Response, Cellect argued that petitioner's proposed construction that limited the term "time select switch" to only a "switch" was too narrow. Appx1209-1210. Instead, Cellect proposed a broader construction of a "feature for selectively varying integration periods to produce an image of desired brightness." *Id.*

Cellect's proposed construction seeking a broader construction of the "time select switch . . . for selectively varying integration periods" term to be more than a simple switch, but to include the features that selectively vary integration periods, is entirely consistent with its position in re-examination because it is the recited time select switch and associated circuitry that perform this very function. Cellect did not change its position across proceedings. In fact, the Examiner in the

reexamination proceeding noted that Cellect argued in the IPR that (i) "a POSITA would understand that the '740 Patent describes a remote switch, including circuitry that can be used to select a desired frequency, for selectively varying integration periods to produce an image of a desired brightness" and (ii) "the '740 Patent explains that the time select switch 45 cannot work without the readout clock select circuitry 318." Appx1247.

Thus, the Board is incorrect that there is anything inconsistent with Cellect's proposed construction that Cellect intended to broadly cover circuitry in the claimed time select switch.

II. THE BOARD ERRED IN FINDING THE *TOMOYASU* REFERENCE RENDERED OBVIOUS THE TIME SELECT SWITCH LIMITATION

A. Standard of Review of the Board's Obviousness Conclusions

This Court reviews the Board's decisions under the Administrative Procedure Act ("APA"). *See, e.g., Rovalma, S.A. v. Bohler-Edelstahl GmbH*, 856 F.3d 1019, 1024 (Fed. Cir. 2017). This Court "review[s] the Board's conclusions of law de novo and its findings of fact for substantial evidence." *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1337 (Fed. Cir. 2016) (citations omitted). Obviousness is a question of law based on underlying findings of fact. *Merck & Cie v. Gnosis S.p.A.*, 808 F.3d 829, 833 (Fed. Cir. 2015) (citation omitted).

The substantial evidence standard is a less deferential review of an agency decision and requires "more than a mere scintilla" of evidence. *In re Gartside,* 203 F.3d 1305, 1312 (Fed. Cir. 2000) ("Substantial evidence is more than a mere scintilla.") (citations omitted). Substantial evidence does not exist where, as here, there is inadequate evidence that would allow a reasonable fact finder to arrive at the agency's decision. *Id.* ("[Substantial evidence] means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion . . . . Mere uncorroborated hearsay or rumor does not constitute substantial evidence.") (citations omitted); *see also Arendi S.A.R.L. v. Apple Inc.,* 832 F.3d 1355, 1366-67 (Fed. Cir. 2016) (no substantial evidence of obviousness where record did not support Board's conclusion to supply a claim limitation missing from prior art).

B. The Board Erred by Applying its Flawed Claim Construction in its Obviousness Analysis Over *Tomoyasu*

The Board erred in finding that the '839 Patent in view of the *Tomoyasu* reference rendered obvious the time select switch limitation of the Asserted Claims. These Asserted Claims require that the "time select switch . . . for selectively varying integration periods" (which, as explained in the preceding section, includes the associated circuitry for varying integration periods) must be "remote" from the "first circuit board" that includes, for example, other video processing circuitry. Appx64 ('740 Patent at Claims 1, 2) ("***a time select switch*** electrically communicating with said first circuit board and ***remote from said first circuit board***

for selectively varying integration periods to produce an image of a desired brightness") (emphasis added).

It is only by applying its flawed construction of the time select switch limitation, which the Board concluded did not include associated circuitry, that the Board was able to find that the simple control knob of *Tomoyasu* constituted a time select switch and that the switch was remote from the first circuit board.

First, the Board identified as the time select switch a control knob that does not contain supporting circuitry for varying integration periods. Appx757; Appx1139-1140; Appx24; Appx1259-1260; Appx1246-1247. Specifically, the Board (and the Examiner during the re-examination proceeding) identified as the time select switch in *Tomoyasu* the "Gain Controlling Knob 23." Appx24; Appx1139; Appx1783 (*Tomoyasu* at Fig. 2). The Gain Controlling Knob (23), however, is nothing more then a knob, as can be seen below in *Tomoyasu* Figure 3 where the knob 23 (highlighted in green in the below figure) is not connected to any circuitry for varying integration periods. At most, knob 23 (with variable resistors) merely varies voltage levels—not integration periods. Appx1777 (*Tomoyasu* at [0041]).

For similar reasons, the Board's attempt to show that the Gain Controlling Knob 23 includes circuitry based on the "sensitivity adjusting means" (25) and Figure 1 also fails. Appx24. The sensitivity adjustment means (25) includes no

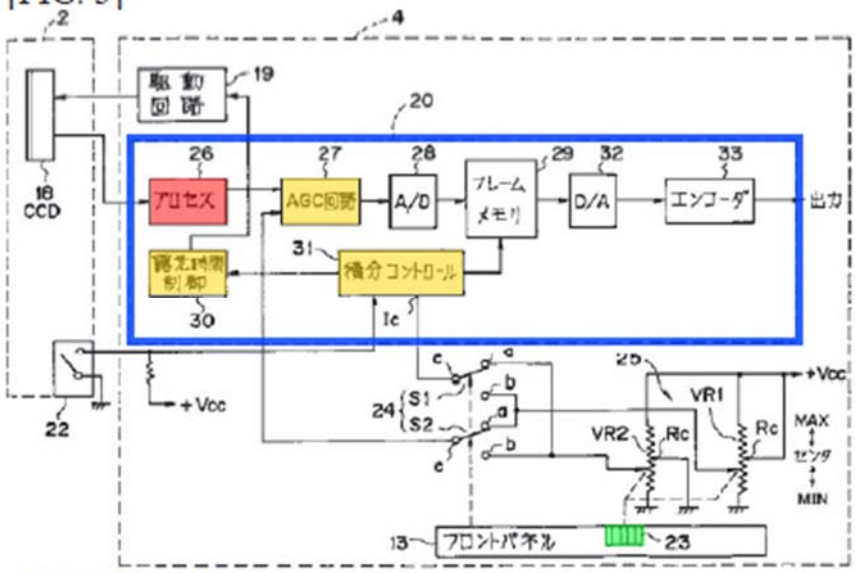
circuitry and is merely a variable resistor that adjusts voltage. Appx1783 (*Tomoyasu* at Fig. 3). In contrast, the circuitry that adjusts the integration period in *Tomoyasu* is control circuit (31), which is on video processor (20) as shown in Figure 3 of *Tomoyasu*. *Id.*; Appx1777 (*Tomoyasu* at [0041]) ("That is, with the gain controlling knob 23 from MIN to center, the voltage of the variable resistance terminal of the variable resistor VRl will change from zero to Vcc, and the ***integration controlling circuit 31*** will carry out integration control depending on the value of the voltage.")[1] (emphasis added). As a result, *Tomoyasu* does not teach or suggest the recited time select switch for selectively varying integration periods.

Second, the purported time select switch in *Tomoyasu* is not remote from the "first circuit board" as required by the Asserted Claims. Specifically, the components in *Tomoyasu* that perform the function of varying the integration period are the Automatic Gain Control ("AGC") circuit (27), Exposure Time Control circuit (30) and Integration Control circuit (31) (collectively, the "*Tomoyasu* Integration Time Select Circuits"). Appx1260. These *Tomoyasu* Integration Time Select Circuits are located with the video processor, and thus are not remote from the video processor as required by the Asserted Claims.

[1] Switch 25 is the combination of knob 23 and variable resistors VR1 and VR2. Appx1775 (*Tomoyasu* at [0017]).

The signal processing circuit is depicted in *Tomoyasu* Figure 3. Appx1783 (*Tomoyasu* at Fig. 3). As Figure 3 illustrates, the Integration Time Select Circuits (which function to vary integration periods) (highlighted in yellow) is located on the same "first circuit board" (20) (highlighted in blue) as other image processing circuitry (26) (identified in red):

[FIG. 3]



19: Driving Circuit
26: Process
30: Exposure Time Control
27: AGC Circuit
31: Integration Control
29: Frame Memory
33: Encoder
[RIGHT OF 33] Output
[LOWER RIGHT] Center
13: Front Panel

Appx1783 (*Tomoyasu* at Fig. 3) (highlighting added).

Thus, under the correct construction of the time select switch term, which includes the circuitry to perform selectively varying integration periods, *Tomoyasu*

lacks this claim element. In particular, *Tomoyasu* lacks the recited remote time select switch because the Integration Time Select Circuits of *Tomoyasu* are on the same first circuit board as other processing circuitry. Indeed, a primary goal of the '740 Patent focuses on separation of circuit board components into different planes and surfaces. The requirement that the time select switch include remote circuitry is expressly recited in the Asserted Claims and consistent with the entirety of the '740 Patent's teaching of separating circuitry into different boards and planes.

The Board's conclusion that Figure 2 of *Tomoyasu* purportedly shows that knob 23 and its supporting circuitry are attached "on the front panel 13" and therefore remote from the signal processing circuit fails for the same reasons discussed above. Appx24. In particular, sensistivty adjusting means (25) comprises knob 23 and a shaft, which is not circuitry for select the integration period and adjusting brightness. Appx1777 (*Tomoyasu* at [0041]).

In addition, the Board's conclusion that the claim may be satisfied by the circuitry in *Tomoyasu* that adjusts the AGC (as opposed to the integration period) to achieve a desired brightness is incorrect. Appx21-22. The claims recite the limitation of "selectively varying integration periods to produce an image of a desired brightness." Appx64 ('740 Patent at Claims 1, 2). The Examiner in its Final Office Action conceded that *Tomoyasu* uses AGC, and not the integration period, to

produce an image with the desired brightness. Appx1139-1141 ("the knob [in *Tomoyasu*] is for increasing/decreasing sensitivity.").

The Board's Decision did not dispute that AGC is used to adjust the brightness, but incorrectly found that the claims do not preclude the use of AGC. Appx21-22 (finding the claim does not preclude use of AGC to produce an image of a desired brightness). The Board's finding is incorrect because the claims explicitly state that the integration periods are varied to produce the image of a desired brightness, not AGC.

Further, the Board raises a new ground that was not raised by Examiner to support its erroneous findings. Specifically, the Board found that "varying the actual integration period independent of the AGC circuit, [] would have been obvious in light of [*Tomoyasu's*] teaching." Appx22. This finding, however, is contrary to the description in *Tomoyasu* which states in the "Problem Solved By The Present Invention" that the benefit of the invention is to link the AGC circuit." Appx1774 (*Tomoyasu* at [0003]-[0006]); Appx1775 (*Tomoyasu* at [0017]) ("sensitivity adjusting means 25, to perform linked adjustment of the gain of the image signal by the signal amplifying means and the sensitivity through the integrating function of the integrating means . . . ."). Notably, the Board acknowledged that varying the AGC, unlike varying integration period, will have an impact on the signal to noise

(i.e., S/N) of an image, even if small. Appx22. At least for these reasons, the Board's obviousness conclusion is unsupported by the *Tomoyasu* reference.

Thus, the Board's conclusion that *Tomoyasu* teaches the claimed "time select switch . . . for selectively varying integration periods" limitation is unsupported by substantial evidence and should be reversed.

CONCLUSION

Cellect respectfully requests that the Court reverse the Board's Decision on Appeal and find patentable Claims 1 and 2 of the '740 Patent.

Respectfully submitted,

Dated: May 2, 2022

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ADDENDUM – TABLE OF CONTENTS

Date	Document Description	Appx No.
12/1/2021	Decision on Appeal	Appx1
	U.S. Patent No. 6,982,740	Appx36

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The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte Cellect, LLC
Patent Owner and Appellant

Appeal 2021-004967
Reexamination Control 90/014,452
Patent 6,982,740 B2
Technology Center 3900

Before JAMESON LEE, ALLEN R. MacDONALD, and MICHAEL J. ENGLE, *Administrative Patent Judges*.

MacDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(b) and 306, Cellect, LLC (Appellant)[1] appeals from the final rejection of claims 1 and 2. Patent claims 3–12, 14, and 15 are not subject to reexamination. Final Act. 19 (PTOL-466). Appellant has cancelled claim 13. February 24, 2021 Response 2. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

[1] Appellant identifies the real party in interest as Cellect LLC, a wholly owned subsidiary of Micro Imaging Solutions LLC. Appeal Br. 2.

CLAIMED SUBJECT MATTER

Claims 1 and 2 are the sole claims on appeal (emphasis, formatting, and bracketed material added):

1. A reduced area imaging device comprising:

[A.] an image sensor lying in a first plane and including an array of pixels for receiving images thereon,

[A.i.] said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels,

[A.ii.] said image sensor producing a pre-video signal;

[B.] a first circuit board lying in a second plane and communicating with said image sensor by at least one pre-video conductor inner-connecting said image sensor and said first circuit board,

[B.i.] said first circuit board including circuitry means for converting said pre-video signal to a post-video signal for reception by a standard video device;

[C.] a power supply[:]

[C.i.] coupled with said image sensor for driving said array of pixels and said timing and control means, and

[C.ii.] electrically coupled to said first circuit board for driving said first circuit board; and

[D.] ***a time select switch***[:]

[D.i.] ***electrically communicating*** with said first circuit board and

[D.ii.] remote from said first circuit board ***for selectively varying integration periods*** to produce an image of a desired brightness,

[D.iii.] said switch having a plurality of settings ***enabling selective control*** to produce the image of a desired brightness.

2. A device, as claimed in claim 1, wherein:

[A.iii.] said array of pixels ***includes*** an array of CMOS pixels.

REJECTION[2]

The Examiner rejects claims 1 and 2 on the ground of nonstatutory (obviousness type) double patenting (OTDP) as being unpatentable over claim 1 of U.S. Patent No. 6,043,839 to Adair et al. (hereinafter "Adair '839") in view of Japanese Patent Publication No. JPH07275198 to Tomoyasu et al. (hereinafter "Tomoyasu"). Final Act. 11–14.

Separate patentability, in compliance with 37 C.F.R. § 41.37(c)(iv), is not argued for claim 2 ("Under each heading identifying the ground of rejection being contested, any claim(s) argued separately or as a subgroup

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[2] Although the Examiner's Final Action includes claim 13, Appellant points out:

> [T]he *First Advisory Action* initially withdrew the rejections of Claims 1 and 2 of the '740 Patent . . . . After receiving the *First Advisory Action*, ***Patent Owner cancelled Claim 13*** in order to expedite issuance of an *Ex Parte* Reexamination Certificate for the '740 Patent. However, . . . the Examiner reversed course, applying a different construction and reinstated the rejection of Claims 1 and 2 in the *Second Advisory Action*.

Appeal Br. 9 (emphasis added). To the extent that Appellant is concerned that the reinstated rejection in the *Second Advisory Action* is now an undesignated new ground of rejection, such an issue is a matter for petition to the Director under 37 C.F.R. § 1.181 and is not appealable to this Board—similar to 37 C.F.R. § 41.40(a) covering examiner's answers:

> Any request to seek review of the primary examiner's failure to designate a rejection as a new ground of rejection in an examiner's answer must be by way of a petition to the Director under § 1.181 of this title.

37 C.F.R. § 41.40(a).

shall be argued under a separate subheading that identifies the claim(s) by number."). Therefore, we select claim 1 as the representative claim for the OTDP rejection of claims 1 and 2. Except for our ultimate decision, we do not address the merits of OTDP rejection of claim 2 further herein.[3]

OPINION

We have reviewed the Examiner's rejections in light of Appellant's arguments (Appeal Brief and Reply Brief) that the Examiner has erred. We disagree with Appellant's conclusions. Except as noted below, we adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellant's Appeal Brief. We concur with the conclusions reached by the Examiner as to the OTDP rejection of claim 1.

A. FIRST ARGUMENT

Appellant raises the following claim construction argument in contending that the Examiner erred in rejecting claim 1 based on OTDP. Appellant argues the Specification of the patent under reexamination

[3] Even if we were to consider Appellant's sole claim 2 argument at page 9 of the Appeal Brief, the argument misinterprets claim 2. Contrary to the argument, claim 2 is not "explicitly limited to CMOS image sensors." Rather, claim 2 requires "said array of pixels ***includes*** an array of CMOS pixels." Emphasis added. Contrary to Appellant's assertion that this is "an issue not addressed by the Examiner's Answer" (Reply Br. 6), the Examiner correctly concludes that claim 2 "doesn't say only CMOS pixels are included." Ans. 5. Claim 2 merely requires the array of pixels of claim 1 now include an array of CMOS pixels as part of array of claim 1. We conclude that nothing in claim 2 requires that the array of claim 1 is now limited to only CMOS pixels.

expressly teaches away from (disparages) Tomoyasu's charge coupled device (CCD) image sensor. Appeal Br. 7–9; Reply Br. 2–6.

A.1. First Argument – Question of Law

Although Appellant and the Examiner (Final Act. 4) use the phrase "teaches away" to describe the "disparagement" issue being argued, we do not find the phrase to be a proper characterization of the "disparagement" issue before us. A "teaches away" determination is a determination as to the teaching of a prior art reference. "What a reference teaches is a question of fact." *In re Beattie*, 974 F.2d 1309, 1311 (Fed. Cir. 1992).

> A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant.

In re Gurley, 27 F.3d 551, 553 (Fed. Cir. 1994).

The "disparagement" issue argued by Appellant concerns claim construction in light of Appellant's Specification. For claim construction, "when the . . . court reviews only evidence intrinsic to the patent (the patent claims and specifications, along with the patent's prosecution history), the judge's determination will amount solely to a determination of law." *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 320 (2015). "The ultimate construction of a claim term is a legal conclusion." *UltimatePointer, L.L.C. v. Nintendo Co., Ltd.*, 816 F.3d 816, 822 (Fed. Cir. 2016).

To the extent that Appellant argues "teaching away" as a factual finding, we treat it as arguing "disparagement" by Appellant's Specification as a legal conclusion as part of claim construction.

A.2. First Argument – Appellant's Contentions

In arguing that the Specification of the patent under reexamination disparages against selectively varying the integration period of a charge coupled device (CCD) such as Tomoyasu's image sensor, Appellant presents the following contentions.

A.2.a. First Argument – Contention 1

> Although the Examiner recognizes there is a distinction between CCD image sensors and CMOS-CID image sensors, the Examiner incorrectly states that the Specification does not teach away from[4] using a CCD image sensors described in Tomoyasu. *Final Office Action* at 3–4. This analysis, however, is demonstrably false, as illustrated above, and legally wrong. *See UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 823 (Fed. Cir. 2016) (finding[5] that the scope of a limitation was narrowed where the patent owner ***repeatedly disparaged and criticized*** a feature in contrast to the claimed invention).

Appeal Br. 8 (additional emphasis added).

> [T]he Specification explains that a CCD image sensor, like the one used in Tomoyasu, cannot vary the integration period to produce an image of a desired brightness because a CCD image sensor uses a fundamentally different (*i.e.*, ***destructive***) ***readout*** mechanism compared to CMOS-CID image sensors. '740 Patent at 5:44–54. . . .

[4] For purposes of this appeal, we treat this "teach away from" as reading "disparage."

[5] For purposes of this appeal, we treat this "finding" as reading "concluding."

> The '740 Patent further describes how CCD image sensors do not work for the claim charge integration period feature:
>
> > While the imager may be used within an endoscopic instrument, it is also contemplated that the image sensor may be incorporated within a microscope, or another imaging device which is used to view cell cultures and the like. ***Most*** commonly available fluorescence microscopes include ***CCD type imagers which are not capable of the variable charge integration***. CCD imagers are charge storage and transfer devices wherein the detector signal produced is representative of the total light impinging or falling upon the pixel array during a ***preset*** exposure time. ***Because of the construction of CCD devices, these exposure times cannot be manipulated for charge integration because CCD imagers have destructive readout***. In other words, each charge is read by transferring the collected charge in each pixel in a serial fashion to a readout amplifier.
>
> '740 Patent at 5:35–49 (emphasis added).

Appeal Br. 7–8 (additional emphasis added).

> The Examiner's Answer also relies on the hybrid CMOS/CCD image sensor in the "Background Art" section of the '740 Patent specification to support the position that Claim 1 covers a CCD image sensor. Examiner's Answer at 5. Here again, this argument misses the mark. The hybrid CMOS/CCD image sensor described in the '740 Patent is part of a common specification in a family of patents owned by Patent Owner and is directed towards another aspect of Patent Owner's invention which is not claimed by the '740 Patent.

Reply Br. 5.

A.2.b. First Argument – Contention 2

> In response to rejection based on Tomoyasu, Patent Owner contrasted this operation of a CCD sensor with the operation of a CMOS or CID sensor. *Response to Office Action* at 6–7; *Response after Final Office* at 2–6 ("In contrast to CCD image sensors which have ***a set predetermined integration period*** (*i.e.*, it ***cannot be varied once readout***), CMOS-CID image sensors permit ***real time monitoring*** (***continual readout***) of the image during the charge integration time period, allowing the charge integration period to continue to collect photons, thus varying the integration period to produce an image with a desired brightness." (citing '740 Patent at 5:35–49)).

Appeal Br. 8 (additional emphasis added).

> Tomoyasu's CCD imager has a destructive readout which is ***incapable of real time readout***. However, the claims require that the desired brightness be obtained within "an image" and thus ***require real-time readout*** possible with a CMOS or CID image sensor, and not adjustment over a series of separate images that would be required using a CCD image sensor.

Reply Br. 2 (emphasis added).

> [T]he Examiner's Answer seeks to ignore the claim language and the express description in the specification by arguing that "the claims do not recite '***real time monitoring*** (or ***continual readout***) of the image during the charge integration time.[']" That argument misses the mark as that "real-time monitoring" or "continual readout" feature is precisely how a POSITA understands the image sensor and time select switch terms in claims 1 and 2.

Reply Br. 4 (emphasis added).

A.3. First Argument – Panel's Analysis

We are unpersuaded by Appellant's argument.

A.3.a. First Argument – Contention 1 – Panel's Analysis

As to Appellant's contention that the Specification disparages and criticizes charge couples device (CCD) image sensors to the point that claim 1 must be read as limited to complementary metal oxide semiconductors-charge injection device (CMOS-CID) image sensors, we disagree. Appellant correctly cites *UltimatePointer*, 816 F.3d 816 as a leading case for claim construction based on disparagement. Appeal Br. 8. However, as an initial matter, Appellant's argument fails because it has not even identified which specific claim limitation should be limited to exclude a CCD.

More importantly, we do not find the patent in the instant appeal to contain the "repeated derogatory statements" (*id.*, 816 F.3d at 822 (citation omitted)) underpinning the claim construction in *UltimatePointer*. For example, the Federal Circuit emphasized the repeated derogatory statements in *UltimatePointer* as follows:

> We agree with Nintendo that the district court did not err in construing "handheld device" as "handheld direct pointing device." The ***specification repeatedly emphasizes*** that the invention is directed to a direct-pointing system. ***The title of the invention explicitly states*** that the invention is an "Easily–Deployable Interactive *Direct Pointing* System . . ." (emphasis added). *See Exxon Chem. Patents, Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1557 (Fed. Cir. 1995) (using patent title to inform claim construction). ***The specification also repeatedly emphasizes*** that the system is for interacting with a presentation in a "direct-pointing" manner, '729 patent, col. 14 ll. 25–28, 33–

> 36, 46–49; col. 15 ll. 3–6; col. 20 ll. 32–35, and even describes the handheld device as a "direct-pointing device," *id.* col. 24 ll. 45–46, 51–53; col. 31 ll. 21–24.
>
> ***The written description also emphasizes*** how direct pointing is superior to indirect pointing. In the "Background of the Invention," the patentee notes that "pointing devices may be classified" as either direct or indirect-pointing devices, *id.* col. 1 ll. 58–60, and that "[i]t needs no argument that direct-pointing systems are more natural to humans, allowing faster and more accurate pointing actions," *id.* col. 2 ll. 1–3.
>
> ***The written description further disparages*** indirect pointing. For example, indirect pointing ***is criticized*** as "less natural" than direct pointing, *id.* col. 2 ll. 35–36, and as not providing "the speed and intuitiveness afforded by direct-pointing systems," *id.* col. 2 ll. 41–43. ***Even a prior art hybrid system***, using both direct and indirect pointing, ***is criticized*** as not "afford[ing] the fast and more accurate interactive pointing actions provided by some other direct-pointing systems," *id.* col. 4 ll. 52–54, and another hybrid system is criticized for not providing "the desired flexibility afforded by truly direct-pointing methods," *id.* col. 5 ll. 1–3. Although the '729 patent does include one embodiment where the handheld device "may include a conventional, indirect pointing device," indirect pointing is only used "where direct pointing is not possible or not desired," *id.* col. 30 ll. 23–26, thus even ***further disparaging*** indirect pointing.
>
> Taken together, the repeated description of the invention as a direct-pointing system, the ***repeated extolling*** of the virtues of direct pointing, and the ***repeated criticism*** of indirect pointing clearly point to the conclusion that the "handheld device" in claims 1, 3, 5, 6, and 12 is limited to a direct-pointing device.

UltimatePointer, 816 F.3d at 823 (emphasis added). Based on the repeated derogatory statements, the court concluded that "the ordinary meaning of 'handheld device,' when read in the specific context of the specification of

the '729 patent, is limited to a direct-pointing device." *UltimatePointer*, 816 F.3d at 824.

Appellant contends varying the integration periods in claim 1 must be read as limited to CMOS-CID image sensors. However, our review of the patent in the instant appeal finds that the title of the invention explicitly states "utilizing selected charge integration periods," but it is silent as to any particular type of image sensor. Also, we find that the Abstract similarly states an "imaging device is provided which utilizes selected charge integration periods" (i.e., the invention requires selected charge integration periods). The Abstract mentions, but does not similarly require, a CMOS-CID device ("[t]he imaging device ***can be*** defined as a CMOS-CID device") (emphasis added).

Further, the Specification repeatedly discusses the importance of utilizing selected charge integration periods without tying the selected charge integration periods to a CMOS-CID device. At column 4, line 65, through column 5, line 27, the Specification introduces four embodiments, none of which include either (a) selected charge integration periods or (b) a CMOS-CID device. Then, without mentioning a CMOS-CID device, the Specification adds four more embodiments by stating:

> For each of the embodiments, ***selected charge integration periods may be used*** to enhance the image to a desired brightness or intensity. Particularly in the field of medical fluorescence detection, the ability to adjust charge integration periods greatly enhances the ability to observe fluorescence from a group of cells which might otherwise be unobservable with normal or preset integration periods.

Spec. column 5, lines 28–34 (emphasis added).

> In addition to use of the imaging device in endoscopy, it is also contemplated that the imaging device of the invention can be incorporated within a microscope which may be used to analyze cell cultures and the like. Although size is not as much of a concern with use of the imaging device within a microscope, there are still great advantages to be obtained by ***providing the imaging device with selected charge integration periods*** to intensify the brightness of an image in fluorescence detection of cell culture media which has no observable fluorescence as observed under standard integration periods.

Spec. column 7, lines 20–30 (emphasis added).

The Specification at column 5, lines 35–49, discusses the limitations of certain CCD imagers in a certain context. However, contrary to Appellant's contention quoting this portion of the Specification (Appeal Br. 7–8), this portion is not a disparagement of all CCD imagers in all contexts. Particularly, the Specification states that "[m]ost commonly available fluorescence microscopes include CCD type imagers which are not capable of the variable charge integration." Claim 1 is not limited to such fluorescence microscopes, but rather is directed more broadly to "[a] reduced area imaging device."

Also, we find Appellant's reading of column 5, lines 41–47 of the Specification to be strained. That portion of the Specification states:

> CCD imagers are charge storage and transfer devices wherein the detector signal produced is representative of the total light impinging or falling upon the pixel array during a ***preset exposure time. Because of the construction of CCD devices, these exposure times cannot be manipulated for charge integration because CCD imagers have destructive readout.***

Spec. column 5, lines 41–47 (emphasis added). While Appellant focuses on the second sentence above and reads this as saying any CCD imager having

destructive readout (the typical construction) cannot include variable charge integration periods, we read the two sentences together as saying any CCD imager having a construction including a preset exposure time and having destructive readout cannot include variable charge integration periods. Contrary to Appellant's argument, it is not "destructive readout" that precludes variable charge integration periods, but rather having a preset exposure time which triggers that destructive readout. The Specification at this portion only disparages CCD imagers having such a preset exposure time and only in the context of fluorescence microscopes. At most, the Specification overgeneralizes about "CCD imagers," but the point remains that what the actual claim language requires is "selectively varying integration periods," which on its face excludes a preset or fixed period but does not necessarily exclude a CCD imager capable of selectively varying integration periods. Therefore, we do not find here the level of disparagement argued by Appellant.

> Also, the Specification at column 13, lines 30–35, states:
>
> [I]t will be clearly understood that ***the invention claimed herein*** is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but ***encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention***.

Spec. column 13, lines 30–35 (emphasis added). Contrary to Appellant's assertion that this is merely background art (Reply Br. 5), we conclude that it speaks to using the invention of "selectively varying integration periods" with "any image sensor."

Finally, the discussions at column 6 and of Figures 9 and 10, at column 18, line 49, through column 20, line 20 of the Specification, do connect the use of variable charge integration and a CMOS-CID imager in a single device. However, Appellant's argument does not point to disparagement in these sections of the Specification, and we do not find therein the disparagement required by *UltimatePointer*.

A.3.b. First Argument – Contention 2 – Panel's Analysis

Appellant contends that "[i]n contrast to CCD image sensors which have a set predetermined integration period (*i.e.*, it cannot be varied ***once readout***), CMOS-CID image sensors permit real time monitoring (continual readout) of the image during the charge integration time period." *Id.* (emphasis added). We do not find Appellant's contention "contrast[ing] operation of a CCD sensor with the operation of a CMOS or CID sensor" (Appeal Br. 8), to be relevant to the rejection before us.

First, Appellant's contention is not commensurate with the scope of the claim language. Appellant's contention focuses on (a) integration variability "once readout" has occurred (i.e., readout occurs prior to varying the integration period) and (b) real time monitoring (continual readout). However, claim 1 recites "selectively varying integration periods to produce an image of a desired brightness" which places no such restrictions on the invention. The Examiner correctly points out that "the claims do not recite 'real time monitoring (or continual readout) of the image during the charge integration time.[']" Ans. 4–5. Nor do we find claim 1 requires real time monitoring or continual readout during any time period. Further, we find nothing in claim 1 that requires the sensor be varied once readout occurs,

that is, nothing in claim 1 precludes varying the integration period prior to the readout.

Second, Appellant's contention overlooks that not all CCD image sensors have a set predetermined integration period, as evidenced by Tomoyasu showing it was known in the art to have a CCD image sensor with an integration period which can be varied before readout.

> [T]he greater the integration controlling voltage, the longer the exposure time, increasing the image integrating function as the integrating means. Note that when the integration controlling voltage is zero, then there will be a constant image exposure time.

Tomoyusa ¶ 23.

B. SECOND ARGUMENT

Also, Appellant raises the following claim construction and procedural arguments in contending that the Examiner erred in rejecting claim 1 based on OTDP.

B.1. Second Argument – Appellant's Contentions

Appellant contends (a) the "time select switch" is not governed by a means plus function interpretation and (b) the Examiner's "reliance on that false premise is a fundamental error that ***warrants*** reversal and ***reinstatement of the previously granted allowance*** of claim[] 1." Appeal Br. 9–10. Appellant further contends:

> The Examiner . . . suggested that Patent Owner provided an ***inconsistent position*** (which it did not) between the related IPR and this reexamination. *Second Advisory Action* at 2–3. However, the Examiner embraced a mistaken understanding of Patent Owner's position - assuming thought Patent Owner's argument was premised on the fact that the time select switch of

> claim 1 was construed as a ***means plus function***. *Id.*; *First Advisory Action* at 6–7. In fact, Patent Owner did not take that position and has not changed its position and is consistent with the related IPR—IPR 2020-00474.

Appeal Br. 9.

B.2. Second Argument – Panel's Analysis

We are unpersuaded by Appellant's arguments. First, the Board lacks authority to order the requested "reinstatement of the previously granted allowance of claim[] 1." Such authority rests with the Director by way of petition.

> The Director shall cause an examination to be made of the application and the alleged new invention; and if on such examination it appears that the applicant is entitled to a patent under the law, the Director shall issue a patent therefor.

35 U.S.C. § 131.

Second, the rejection before us is not premised on the "time select switch" being governed by a means plus function interpretation. While the *First Advisory Action* was so premised, in the *Second Advisory Action* "the Examiner withdraws his previous comments regarding the requirement of circuitry 318 since it creates inconsistencies among the proceedings" (Second Advisory Action 3), and returns to the claim interpretation of the Final Action which does not treat the "time select switch" as being governed by a means plus function interpretation.

> [S]ince the Patent Owner did not assert that the claimed "time select switch" must be constructed under 112 6th paragraph . . . , then the Examiner maintains the same position set forth in the Final Rejection in that the claim term does not require any additional structure and therefore does not require circuitry 318 since it is not a claimed element. For this reason, the double

> patenting rejection of Tomoyasu remains since the Examiner, upon reconsideration, maintains that circuitry 318 is not required for the claimed time select switch.
>
> Therefore, the rejection of claims 1 and 2 will remain for the reasons set forth in the Final Rejection.

Second Advisory Action 3.

> Third, we agree with the Examiner that:
>
> Patent Owner's current construction of the claim term "time select switch" is ***inconsistent*** with [Appellant's proposed] construction in IPR2020-00474 since [Appellant's proposed] construction in the IPR did not include "circuitry 318".

Second Advisory Action 3. Contrary to Appellant's contention, the Examiner does not premise his determination of inconsistent construction on a means plus function interpretation of the "time select switch," but rather on failure of Appellant's proposed IPR construction of the "time select switch" to include circuitry 318.

C. THIRD ARGUMENT

Further, Appellant raises the following prior art teaching argument in contending that the Examiner erred in rejecting claim 1 based on OTDP. Appellant argues Tomoyasu does not disclose the claimed features. Appeal Br. 10–13; Reply Br. 2, 6–10.

C.1. Third Argument – Appellant's Contentions

In arguing that Tomoyasu does not disclose the claimed features, Appellant presents the following contentions.

C.1.a. Third Argument – Contention 1

> [A]s Patent Owner has noted, Tomoyasu uses automatic gain control (AGC) circuitry and ***never allows a user to vary the***

> ***actual integration period*** to produce an image of a desired brightness, ***independent of*** the AGC circuit—the gain control knob for adjusting integration merely gains priority over AGC. Response to Office Action at 6; *Response after Final Office Action* at 6-7; Tomoyasu at [0018], [0040].

Appeal Br. 10 (additional emphasis added).

C.1.b. Third Argument – Contention 2

> The time select switch in ***Tomoyasu is not remote*** from the first circuit board as required by the claims ***because the functionality to adjust the integration period is on the first circuit board*** with the image processing circuit (rather than a remote switch), as shown in Figure 3 of Tomoyasu.

Appeal Br. 10 (additional emphasis added).

> The Examiner's assertion that the claims do not require a time select switch ***with the remote functionality in circuit 318*** is contrary to the Specification and recited claim limitations which require the switch to selectively vary the integration period. See, e.g., Claim 1 ("***said switch*** having a plurality of settings ***enabling*** selective control ***to produce the image of a desired brightness***"). Further, the Specification of the '740 Patent explains that the time select switch . . . ***cannot work without the readout clock select circuitry 318*** which is must be [sic] *remote* from the first circuit board:
>
> > FIG. **10** is a schematic diagram of an imager and its processing circuitry which incorporate variable charge integration capability. Imager **40** is coupled to its video processing circuitry **50**. Power supply **52** supplies power to the 40 imaging device and the additional circuitry to achieve charge integration. ***In order to incorporate variable charge integration capability, imager readout clock select circuitry 318 is added which communicates*** with one or more of the video processor boards **50**. An imager integration time select . . . switch **320** is provided ***enabling an operator to manually select the***

> ***desired integration period***. As shown, the integration periods may be periods of less than one second, or more than one second.

'740 Patent at [19:]37–49 (emphasis added).

> Figure 10, further confirms that circuitry 318 is remote from the first circuit board. . . . Therefore, ***the time select switch includes*** the functional element, ***circuity*** (***318***), and is remote from the first circuit board to vary the integration period.

Appeal Br. 11–12 (additional emphasis added).

> [T]he time select switch element in claim[] 1 . . . recites that this element is "remote from the first circuit board." The Examiner's Answer, however, ***fails to demonstrate*** that the circuitry or components in Tomoyasu that encompass the time select switch element are ***remote*** from the first circuit board. Rather, the ***Tomoyasu*** "time select switch" ***components*** identified in the Examiner's Answer ***are directly on the first circuit board***.

Reply Br. 2 (emphasis added).

> Claim[] 1 . . . . of the '740 Patent require that the time select switch for selectively varying integration periods be ***remote*** from the first circuit board. Tomoyasu fails to meet this limitation because the control knob in Tomoyasu is just that, a ***knob with no supporting circuitry for varying the integration periods*** and thus ***not a remote*** "time select switch." More particularly, as a matter of claim construction, a "time select switch" is not a simple "switch." The "time select switch" ***must include*** the ***functionality to vary*** the integration period and ***must*** be ***remote*** from the first circuit board. The Examiner's Answer rejection of claims 1 and 2, however, is premised on a ***flawed construction that a "time select switch" is synonymous with any kind of "switch"*** and does not require the ***functionality for varying*** the integration periods to be ***remote***. Examiner's Answer at 7–10. This is wrong and under the proper construction, Tomoyasu ***does not disclose*** the claimed ***remote*** "time select switch."

Reply Br. 6–7 (additional emphasis added).

> It is undisputed that the Automatic Gain Control (AGC) circuit 27, ***Exposure Time Control circuit 30 and Integration Control circuit 31*** (collectively referred to as "integration time select circuits") in Tomoyasu, which performs the actual function "varying" the integration period, ***is not remote*** from the first circuit board 20, but in fact is located on the first circuit board with the image processing circuitry 26, as shown in Figure 3 of Tomoyasu[.] . . . Thus, control knob 23, including the integration time select circuits, are not remote from the first circuit board in Tomoyasu.

Reply Br. 7 (emphasis added).

> Based on the specification (and claims), the proper construction for a *remote* "time select switch" requires the ***functionality for varying integration periods be remote.*** *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction."). Under the correct construction, Tomoyasu ***does not disclose a remote*** "time select switch" because AGC 26, ***Time Exposure Control circuit 30 and Integration Control circuit 31*** are all on the same circuit board 20 and ***are not remote*** from circuit board 20.

Reply Br. 9 (emphasis added).

C.2. Third Argument – Panel's Analysis

We are unpersuaded by Appellant's argument.

C.2.a. Third Argument – Contention 1 – Panel's Analysis

Appellant contends that the Examiner errs because Tomoyasu uses automatic gain control (AGC) circuitry and never allows a user to vary the actual integration period independent of the AGC circuit. We disagree.

First, Appellant's contention is not commensurate with the scope of the claim language. Claim 1 does not preclude use of an AGC circuit to vary the actual integration period.

Second, even if claim 1 were construed to require varying the actual integration period independent of the AGC circuit, such would have been obvious in light of Tomoyasu teaching it was known for a still image to "extend[] the integration time of the image sensor" with "little negative effect on the S/N of the image." Tomoyasu ¶¶ 3–5.

C.2.b. Third Argument – Contention 2 – Panel's Analysis

C.2.b.i.

Appellant asserts that Tomoyasu does not disclose the claimed "a remote time select switch" because Tomoyasu's Exposure Time Control circuit 30 and Integration Control circuit 31 perform the actual function of "varying" the integration period, and thus, the functionality to adjust the integration period is on the Tomoyasu's first circuit board (Appeal Br. 10; Reply Br. 7 and 9). We disagree with Appellant's assertion.

We do not construe claim 1 to require integration control circuitry as part of the claimed time select switch. Indeed, claim 1 does not even recite "integration control circuitry." Appellant is conflating the claimed function of "selectively varying integration periods" with the function of performing the actual integration (control circuitry) based on selectively varying the integration period. Claim 1 requires the first function, but not anything that performs the second.

C.2.b.ii.

As to Appellant's assertion that claim 1 must be read as the time select switch including circuitry 318 (Appeal Br. 11–12; Reply Br. 7 and 9), we disagree.

First, the Specification states "[a]n imager integration time select switch 320 is provided enabling an operator to manually ***select*** the desired integration period." Spec. 19:45–47 (emphasis added). That is, the function of "select[ing] the desired integration period" is the sole function recited for time select switch 320 at column 19. Reviewing Figure 10, we also find an electrical communication line shown from near the center of time select switch 320 to a first circuit board (via circuitry 318). We find disclosure of two functions (selecting and electrically communicating) disclosed as performed by time select switch 320.

Second, the description of circuitry 318 states "imager readout clock select circuitry 318 is added which ***communicates*** with one or more of the video processor boards 50." Spec. 19:43–45 (emphasis added). We find the sole function performed by circuitry 318 is communicating. Claim 1 requires time select switch functions of "electrically communicating" and "selectively varying integration period" which the disclosure shows time select switch 320 as performing. We do not find circuitry 318 to be required by claim 1. As Appellant was not required to claim circuitry 318, we will not read it into claim 1. Even if we were to agree with Appellant that claim 1 must be read such that the time select switch includes circuitry 318, given the limited disclosed function of circuitry 318, nothing more would be

required than basic communication signal conditioning circuitry well-known to an artisan.

C.2.b.iii.

As to Appellant's assertion that (a) Tomoyasu's "time select switch" components are directly on Tomoyasu's first circuit board (not remote) and (b) Tomoyasu has only a knob with no supporting circuitry for varying the integration periods (Reply Br. 2 and 6–7), we disagree.

Although Appellant repeatedly references Figure 3 of Tomoyasu (Appeal Br. 10; Reply Br. 7), Appellant overlooks that:

(i) Figure 3 of Tomoyasu, in addition to knob 23, shows supporting circuitry for varying the integration periods at item 25 ("sensitivity adjusting means" para. 17),

(ii) Figure 1 of Tomoyasu shows the supporting circuitry at item 25 is attached to the knob 23, and

(iii) Figure 2 of Tomoyasu shows the knob 23 (and therefore the supporting circuitry) is attached "on the front panel 13" (para. 16) and thus the knob and supporting circuitry are remote from Tomoyasu's signal processing circuit 20 (Figure 3).

D. FOURTH ARGUMENT

Furthermore, Appellant raises the following legal argument in contending that the Examiner erred in rejecting claim 1 based on OTDP. Appeal Br. 13–14.

D.1. Fourth Argument – Appellant's Contention

> Patent Owner reiterates its . . . position that the record is completely devoid of any "unjustified or improper timewise

> extension." Furthermore, the *First Advisory Action* and *Final Office Action* ***fail to identify any acts by Patent Owner*** to support such an allegation since obviousness-type double patenting is a judicial doctrine based on the principle of preventing unfair extensions of patent term, which is not at issue here.
>
> . . .
>
> Obviousness-type double patenting is a judicially created doctrine that is equitable in nature and ***requires some form of gamesmanship by the Patent Owner*** to unjustifiably or improperly extend the term of the patent. Patent Owner respectfully submits that the record is completely devoid of any "unjustified or improper timewise extension," and the *First Advisory Action* and *Final Office Action* ***fail to identify any acts by Patent Owner*** to support such an allegation.
>
> . . .
>
> Moreover, an obviousness-type double patenting rejection was never intended to invalidate a patent-***only to ensure*** there would be no "unjustified or improper" extension of term, which is not present here. . . .
>
> As such, an equitable doctrine should not be applied in a manner that would be inequitable akin to sandbagging and depriving Patent Owner of its property rights due solely to anomalies by the PTO.

Appeal Br. 13–14 (additional emphasis added).

D.2. Fourth Argument – Panel's Analysis

We are unpersuaded by Appellant's arguments. First, Appellant does not support the assertions with any case law showing that more is required than what the Examiner has already shown. That is, Appellant has not shown that demonstrating "gamesmanship" or "acts by Patent Owner" is a requirement on the Examiner to show obviousness-type double patenting. Based on the Examiner's rejection (Final Act. 11–14) and our analysis

supra, we agree with the Examiner that "double patenting is proper under reexamination and cannot be avoided since the claims are not patentably distinct from those in the earlier [Adair '839] Patent and Tomoyasu." Ans. 13.

Second, Appellant does not address that double patenting also applies to prevent harassment by multiple assignees. One goal of double patenting and terminal disclaimers is to preemptively prevent the risk of such harassment:

> Even though both patents are issued to the same patentee or assignee, it (is) possible that ownership of the two will be divided by later transfers and assignments. The possibility of multiple suits against an infringer by assignees of related patents has long been recognized as one of the concerns behind the doctrine of double patenting.

In re Van Ornum, 686 F.2d 937, 944 (CCPA 1982) (quoting Chisum on Patents § 9.04(2)(b) (1981)).

Third, Appellant does not address preserving the public's right to make what is covered by the *earlier* patent after it expired:

> The bar against double patenting was created to preserve that bargained-for right held by the public. *See, e.g., Miller v. Eagle Mfg. Co.*, 151 U.S. 186, 197–98, 202 (1894) . . . *Odiorne v. Amesbury Nail Factory*, 18 F.Cas. 578, 579 (C.C.D.Mass.1819). If an inventor could obtain several sequential patents on the same invention, he could retain for himself the exclusive right to exclude or control the public's right to use the patented invention far beyond the term awarded to him under the patent laws. As Justice Story explained in 1819, "[i]t cannot be" that a patentee can obtain two patents in sequence "substantially for the same invention[] and improvements"; "it would completely destroy the whole consideration derived by the public for the grant of the patent, viz. the right to use the invention at the expiration of the term." *Odiorne*, 18 F.Cas. at 579. Thus, the doctrine of double

> patenting was primarily designed to prevent such harm by limiting a patentee to one patent term per invention or improvement.

Gilead Scis., Inc. v. Natco Pharma Ltd., 753 F.3d 1208, 1212 (Fed. Cir. 2014) (parallel citations omitted).

Fourth, the Federal Circuit has explained that the inequity is Appellant's enjoyment of a second patent's term beyond the expiration of the first patent:

> When the claims of a patent are obvious in light of the claims of an earlier commonly owned patent, the patentee can have no right to exclude others from practicing the invention encompassed by the later patent after the date of the expiration of the earlier patent. But when a patentee does not terminally disclaim the later patent before the expiration of the earlier related patent, the later patent purports to remain in force even after the date on which the patentee no longer has any right to exclude others from practicing the claimed subject matter. By permitting the later patent to remain in force beyond the date of the earlier patent's expiration, the patentee wrongly purports to inform the public that it is precluded from making, using, selling, offering for sale, or importing the claimed invention during a period after the expiration of the earlier patent.
>
> By failing to terminally disclaim a later patent prior to the expiration of an earlier related patent, a patentee enjoys an unjustified advantage—a purported time extension of the right to exclude from the date of the expiration of the earlier patent. The patentee cannot undo this unjustified timewise extension by retroactively disclaiming the term of the later patent because it has *already* enjoyed rights that it seeks to disclaim.

Boehringer Ingelheim Int'l GmbH v. Barr Labs., Inc., 592 F.3d 1340, 1347–48 (Fed. Cir. 2010) (citations omitted); *see also In re Lonardo*, 119 F.3d 960, 965 (Fed. Cir. 1997).

CONCLUSIONS

The Examiner has not erred in rejecting claims 1 and 2 as being unpatentable on the ground of nonstatutory (obviousness type) double patenting.

The Examiner's rejection of claims 1 and 2 as being unpatentable on the ground of nonstatutory (obviousness type) double patenting is **affirmed**.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 2		Nonstatutory (obviousness type) double patenting Adair '839, Tomoyasu	1, 2	
Overall Outcome			1, 2	

REQUESTS FOR EXTENSIONS OF TIME

Requests for extensions of time in this ex parte reexamination proceeding are governed by 37 C.F.R. § 1.550(c). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

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US006982740B2

(12) **United States Patent**
Adair et al.

(10) **Patent No.: US 6,982,740 B2**
(45) **Date of Patent: Jan. 3, 2006**

(54) **REDUCED AREA IMAGING DEVICES UTILIZING SELECTED CHARGE INTEGRATION PERIODS**

(75) Inventors: **Edwin L. Adair**, Castle Pines Village, CO (US); **Jeffrey L. Adair**, Highlands Ranch, CO (US); **Randall S. Adair**, Denver, CO (US)

(73) Assignee: **Micro-Medical Devices, Inc.**, Castle Pines Village, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 765 days.

(21) Appl. No.: **09/971,749**

(22) Filed: **Oct. 4, 2001**

(65) **Prior Publication Data**

US 2002/0080248 A1 Jun. 27, 2002

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/368,246, filed on Aug. 3, 1999, now Pat. No. 6,310,642, which is a continuation-in-part of application No. 08/976,976, filed on Nov. 24, 1997, now Pat. No. 5,986,693, and a continuation-in-part of application No. 09/586,768, filed on Jun. 1, 2000, now Pat. No. 6,316,215.

(51) **Int. Cl.**
H04N 7/18 (2006.01)

(52) **U.S. Cl.** **348/76**; 348/65; 348/68

(58) **Field of Classification Search** 348/65–76; 600/100–120

See application file for complete search history.

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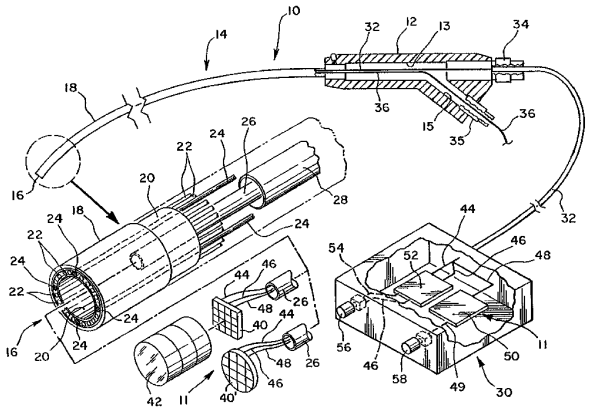
(Continued)

Primary Examiner—Andy Rao
(74) *Attorney, Agent, or Firm*—Sheridan Ross P.C.

(57) **ABSTRACT**

A reduced area imaging device is provided which utilizes selected charge integration periods. Various configurations of the imaging device are provided which locate the elements of the imagine device at desired locations. Regardless of the particular arrangement or configuration of the imaging device, selected charge integration periods are incorporated. The imaging device can be defined as a CMOS-CID device wherein a user may select an appropriate integration period in order to enhance the viewed image to a desired level of brightness. Particularly in fluorescence guided endoscopy and fluorescence assisted surgery, the ability to vary and select particular charge integration periods improves these processes.

15 Claims, 16 Drawing Sheets



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5,980,450	A	11/1999	Thompson	600/112
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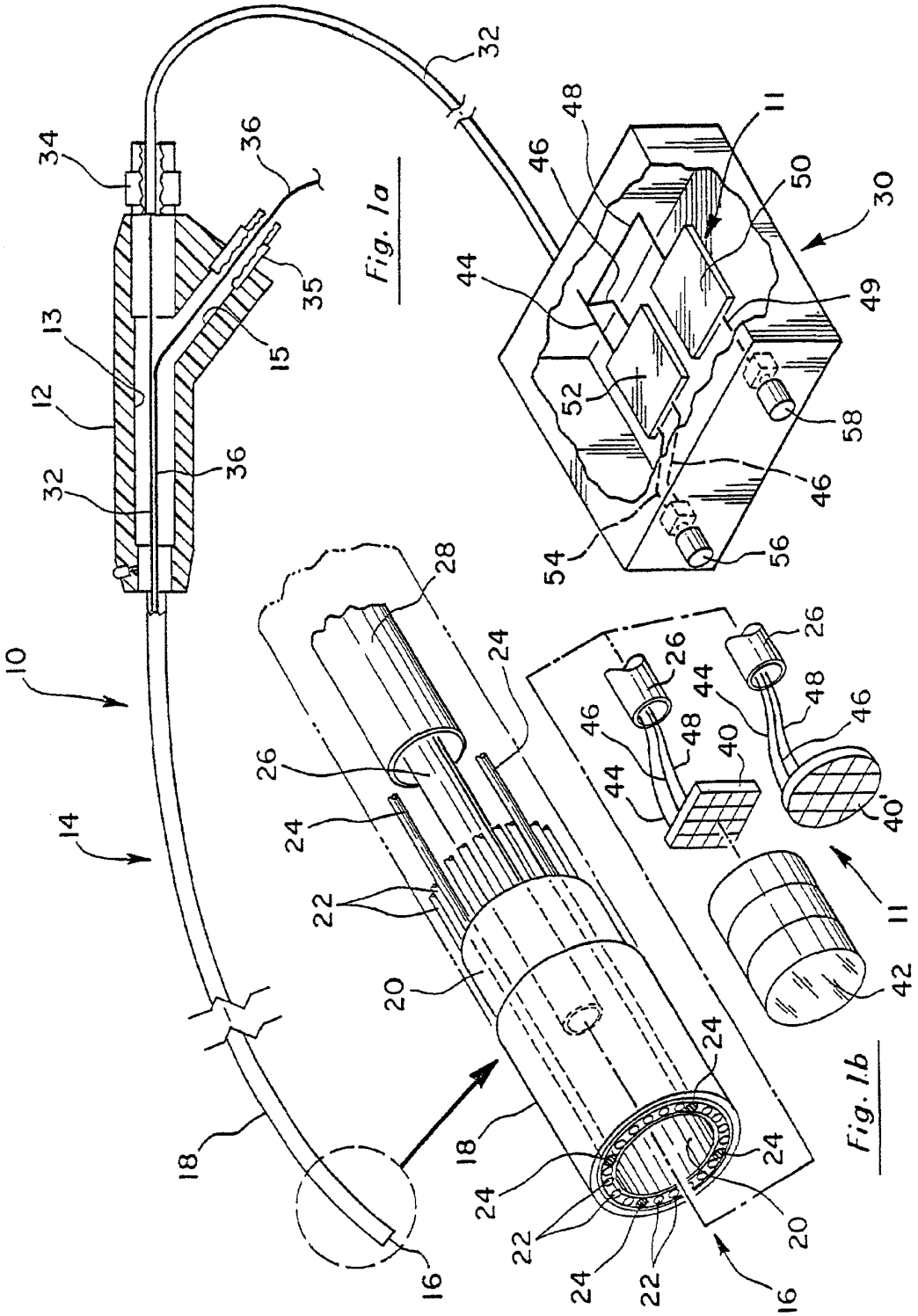

32
34
36
35
15
13
12
32
36
Fig. 1a
48
46
11
50
30
44
49
52
58
46
54
56
28
24
26
24
22
20
18
16
10
14
26
44
48
46
40
40'
11
42
Fig. 1b

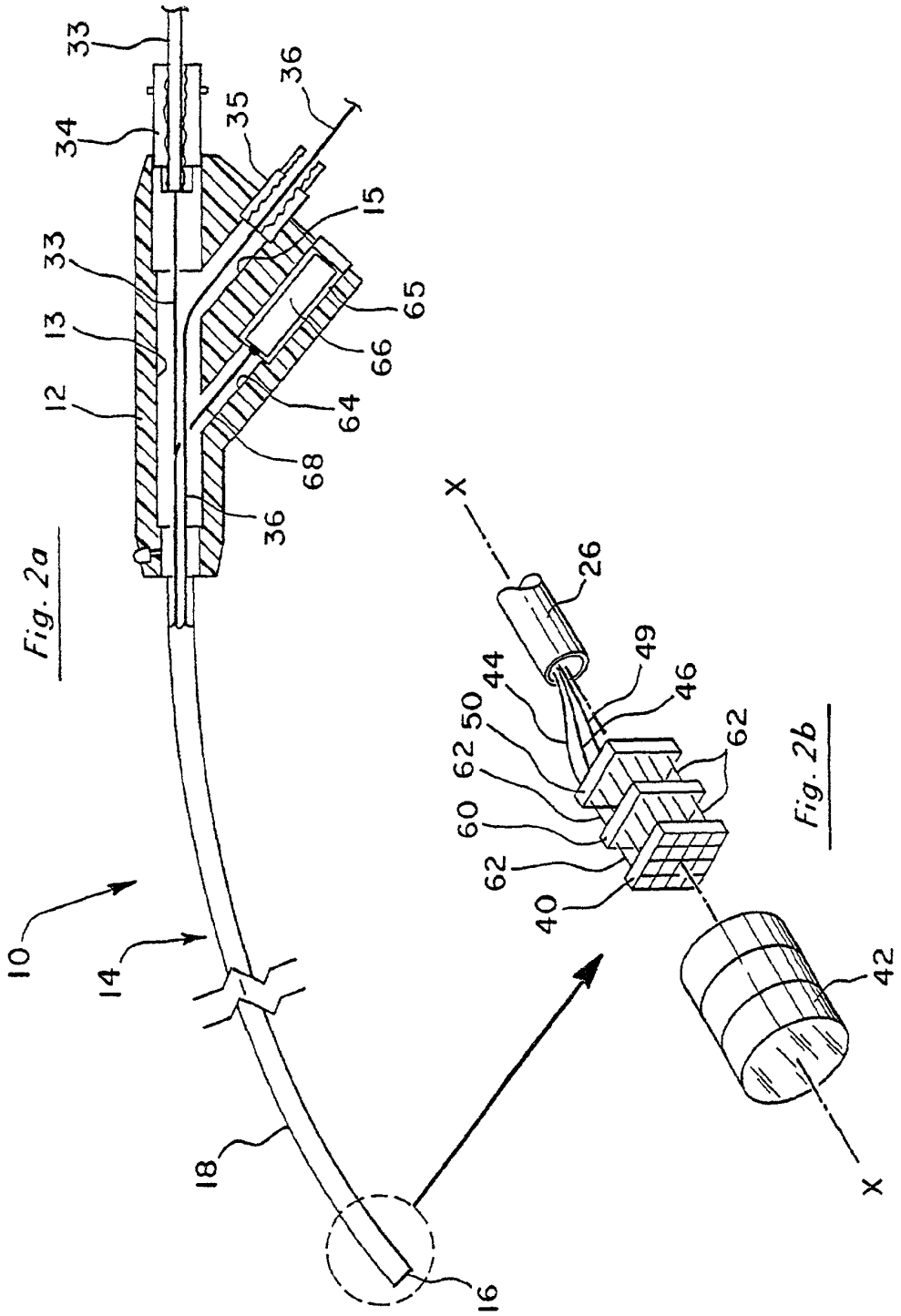
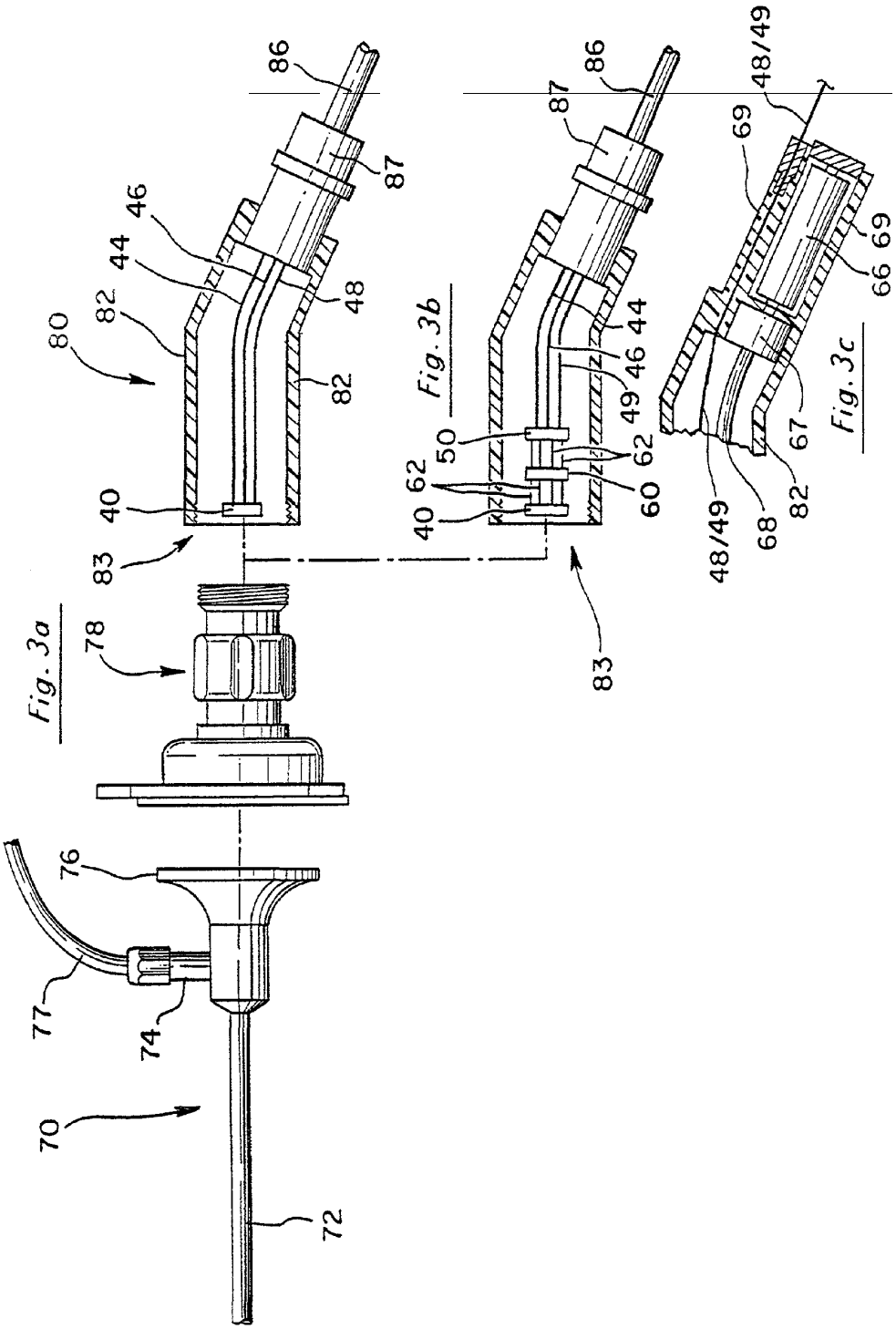

33
34
35
36
15
65
66
64
68
36
33
13
12
10
14
18
16
X
26
49
46
44
50
62
60
62
62
40
42
X

Fig. 2a

Fig. 2b


86
87
46
44
82
80
48
82
40
83
78
76
77
74
70
72
Fig. 3a
86
87
Fig. 3b
48/49
69
69
66
Fig. 3c
44
46
49
50
62
62
60
40
83
48/49
68
82
67

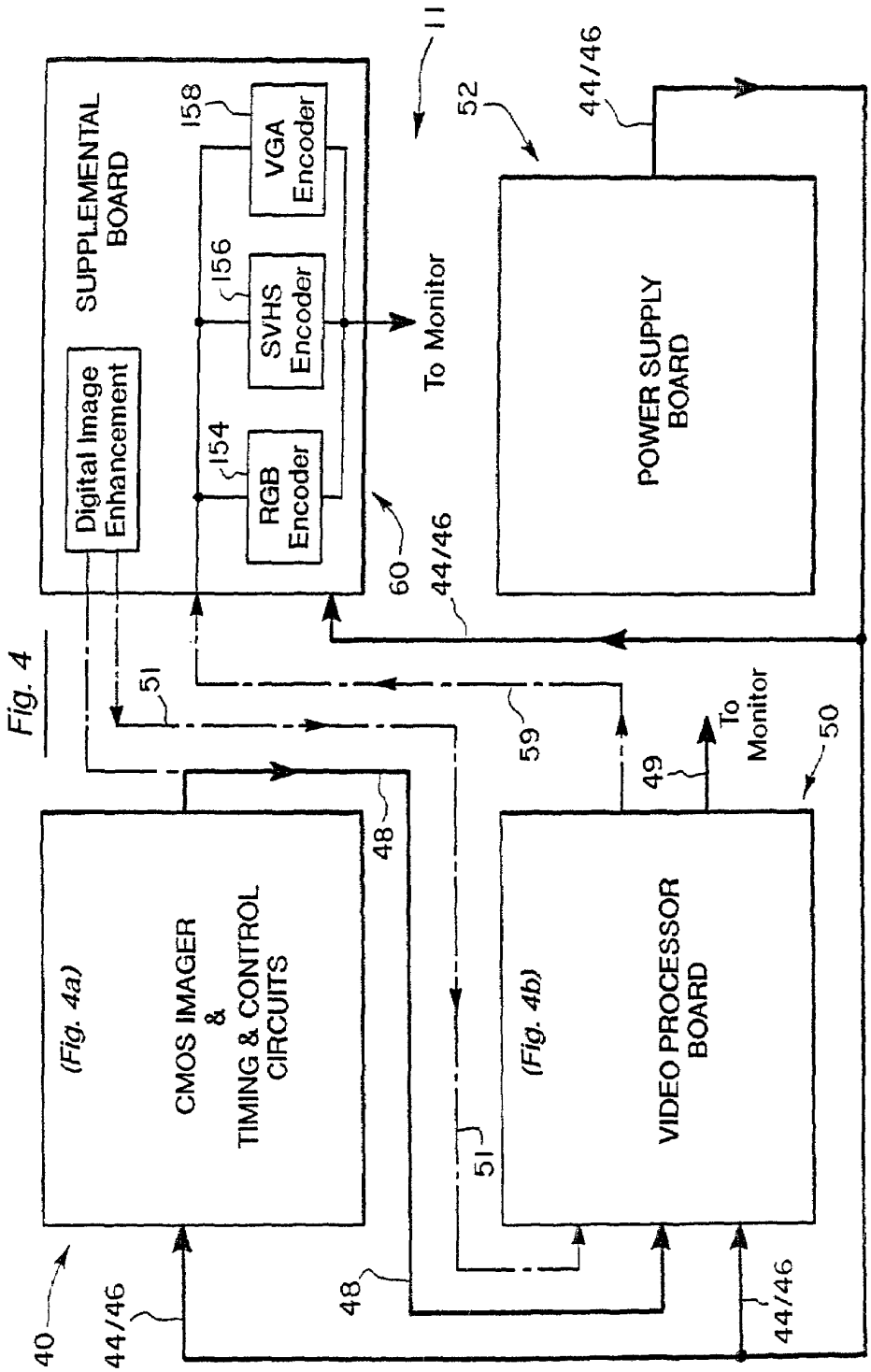

11
52
44/46
158
VGA Encoder
156
SVHS Encoder
154
RGB Encoder
SUPPLEMENTAL BOARD
Digital Image Enhancement
To Monitor
POWER SUPPLY BOARD
60
44/46
51
59
49
To Monitor
50
48
(Fig. 4a)
CMOS IMAGER & TIMING & CONTROL CIRCUITS
(Fig. 4b)
VIDEO PROCESSOR BOARD
51
40
44/46
48
44/46

Fig. 4

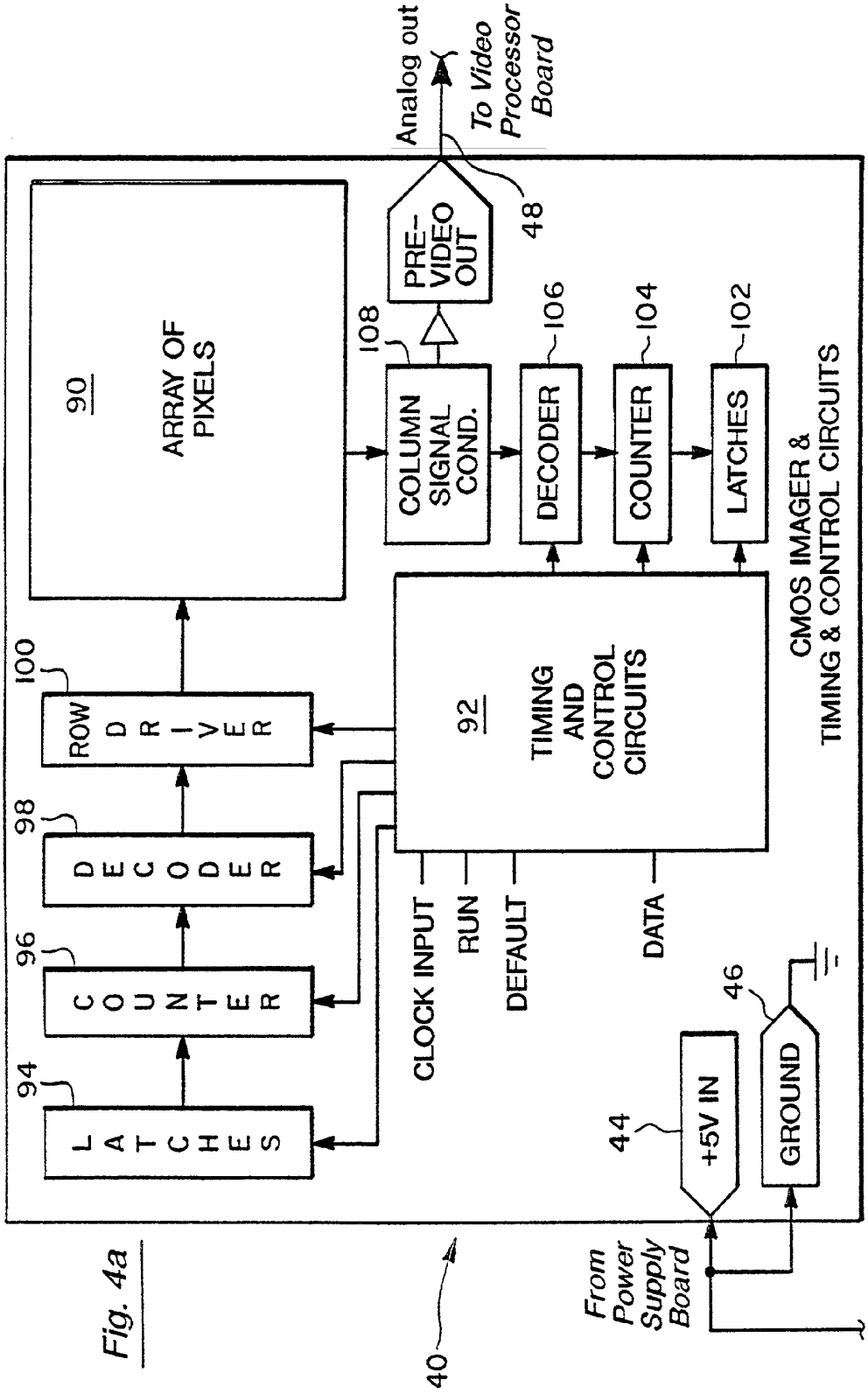

Analog out
To Video Processor Board
48
PRE-VIDEO OUT
108
90
ARRAY OF PIXELS
COLUMN SIGNAL COND.
106
DECODER
104
COUNTER
102
LATCHES
CMOS IMAGER & TIMING & CONTROL CIRCUITS
100
ROW DRIVER
92
TIMING AND CONTROL CIRCUITS
98
DECODER
96
COUNTER
94
LATCHES
CLOCK INPUT
RUN
DEFAULT
DATA
46
44
+5V IN
GROUND
From Power Supply Board
40

Fig. 4a

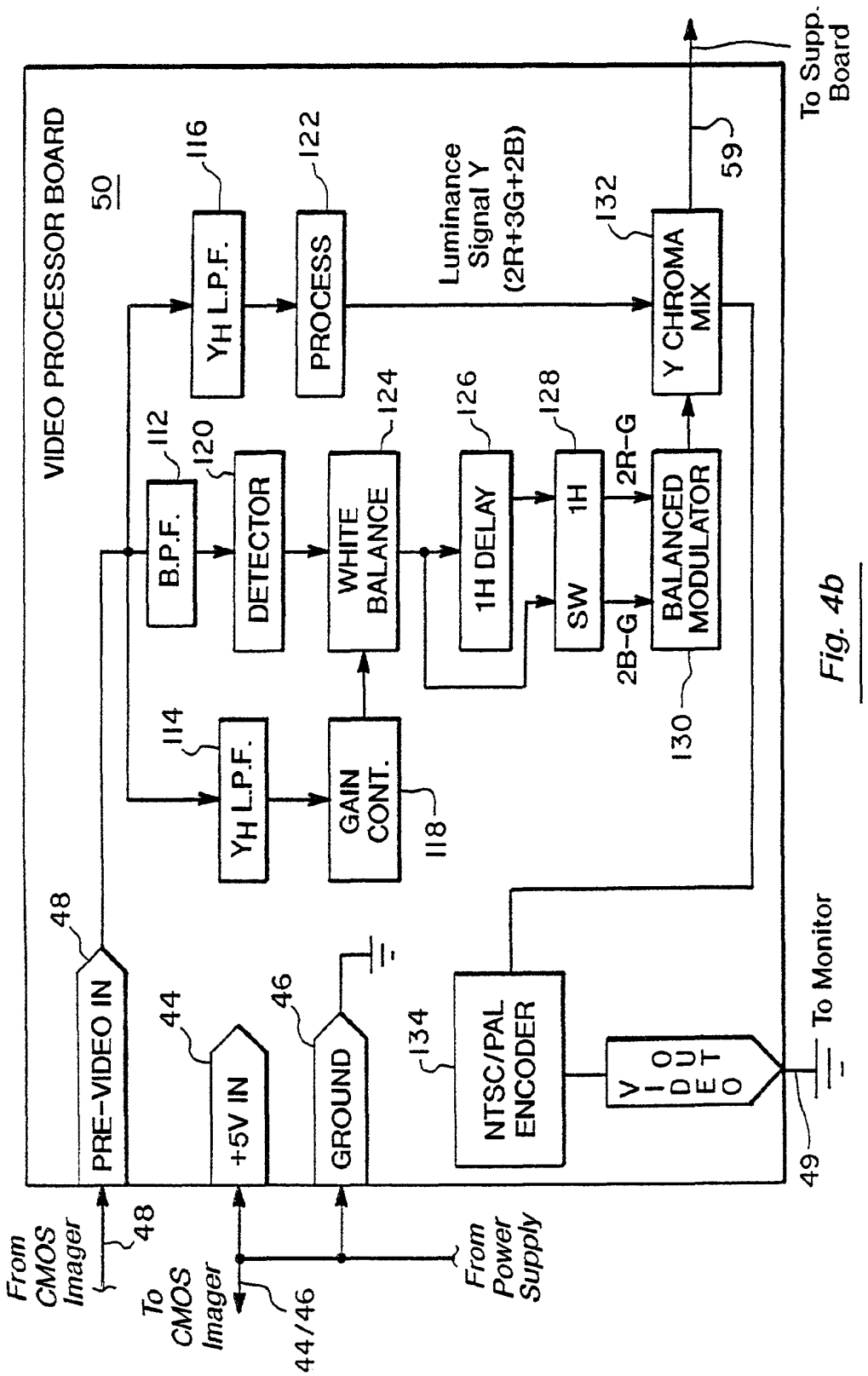

VIDEO PROCESSOR BOARD
50
PRE-VIDEO IN
48
+5V IN
44
GROUND
46
B.P.F.
112
DETECTOR
120
WHITE BALANCE
124
1H DELAY
126
SW 1H
128
2R-G
2B-G
BALANCED MODULATOR
130
Y CHROMA MIX
132
Luminance Signal Y (2R+3G+2B)
PROCESS
122
YH L.P.F.
116
YH L.P.F.
114
GAIN CONT.
118
NTSC/PAL ENCODER
134
VIDEO OUT
To Monitor
49
To Supp. Board
59
From CMOS Imager
48
To CMOS Imager
44/46
From Power Supply

Fig. 4b

Fig. 5a

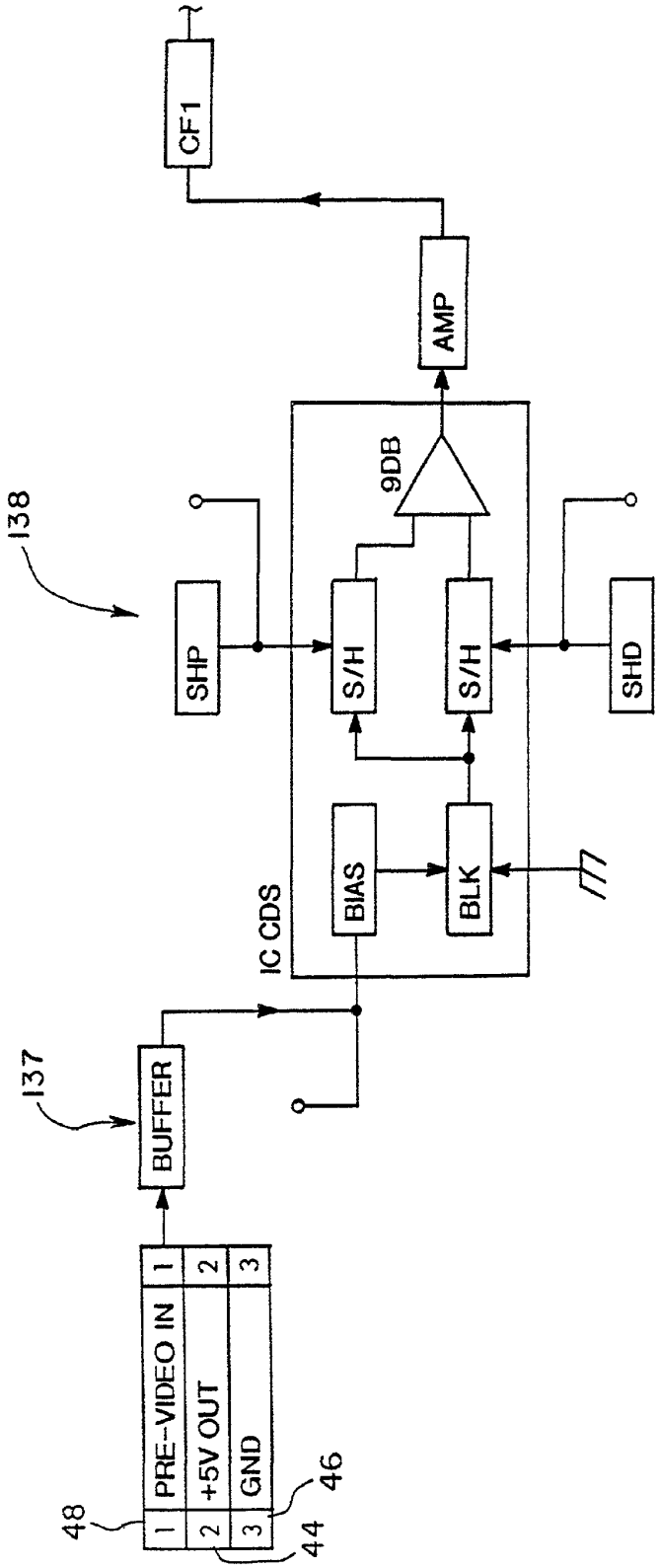

CF1
AMP
9DB
138
SHP
S/H
S/H
SHD
IC CDS
BIAS
BLK
177
137
BUFFER
PRE-VIDEO IN
+5V OUT
GND
1
2
3
48
46
44

Fig. 5b

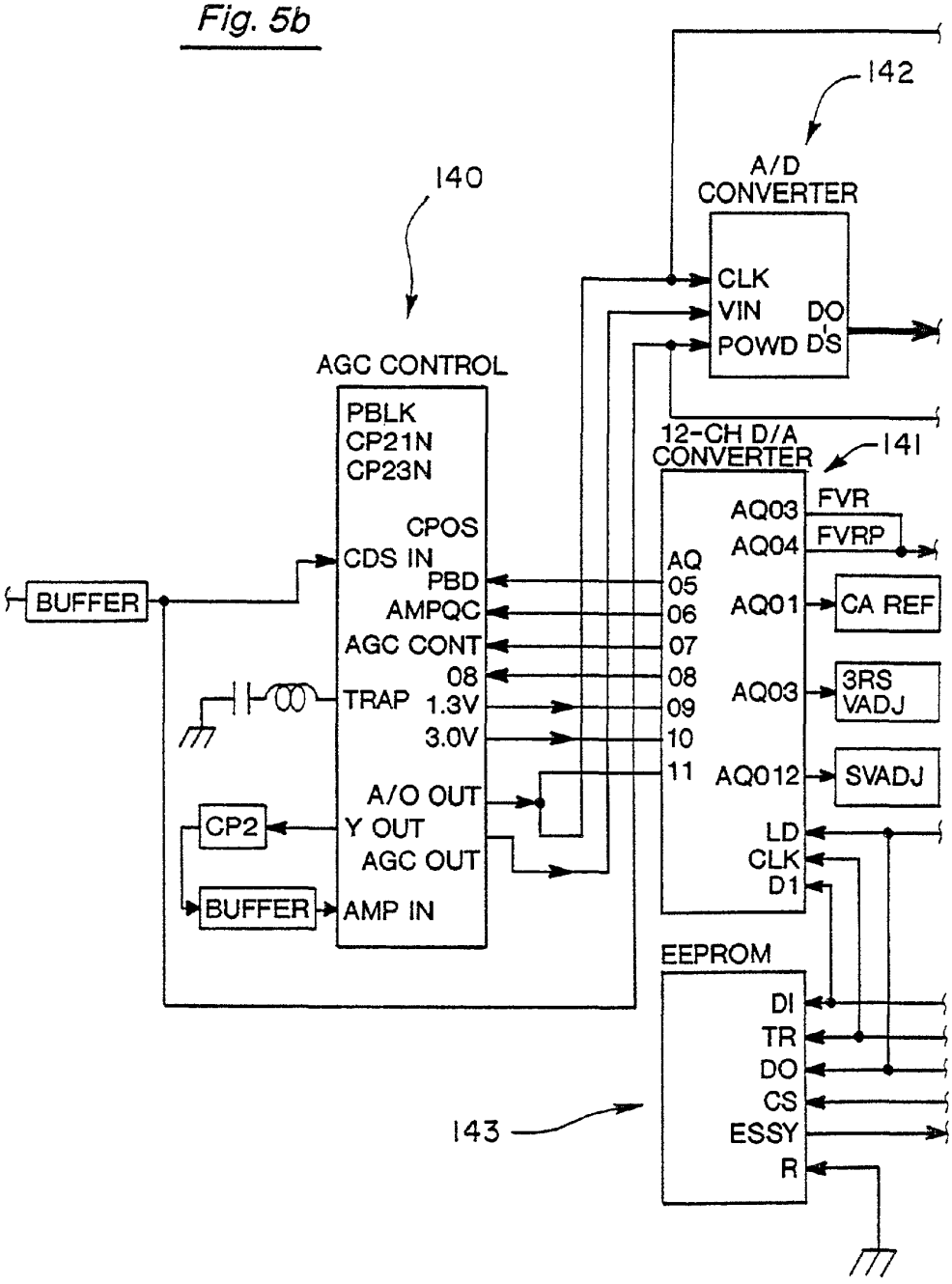
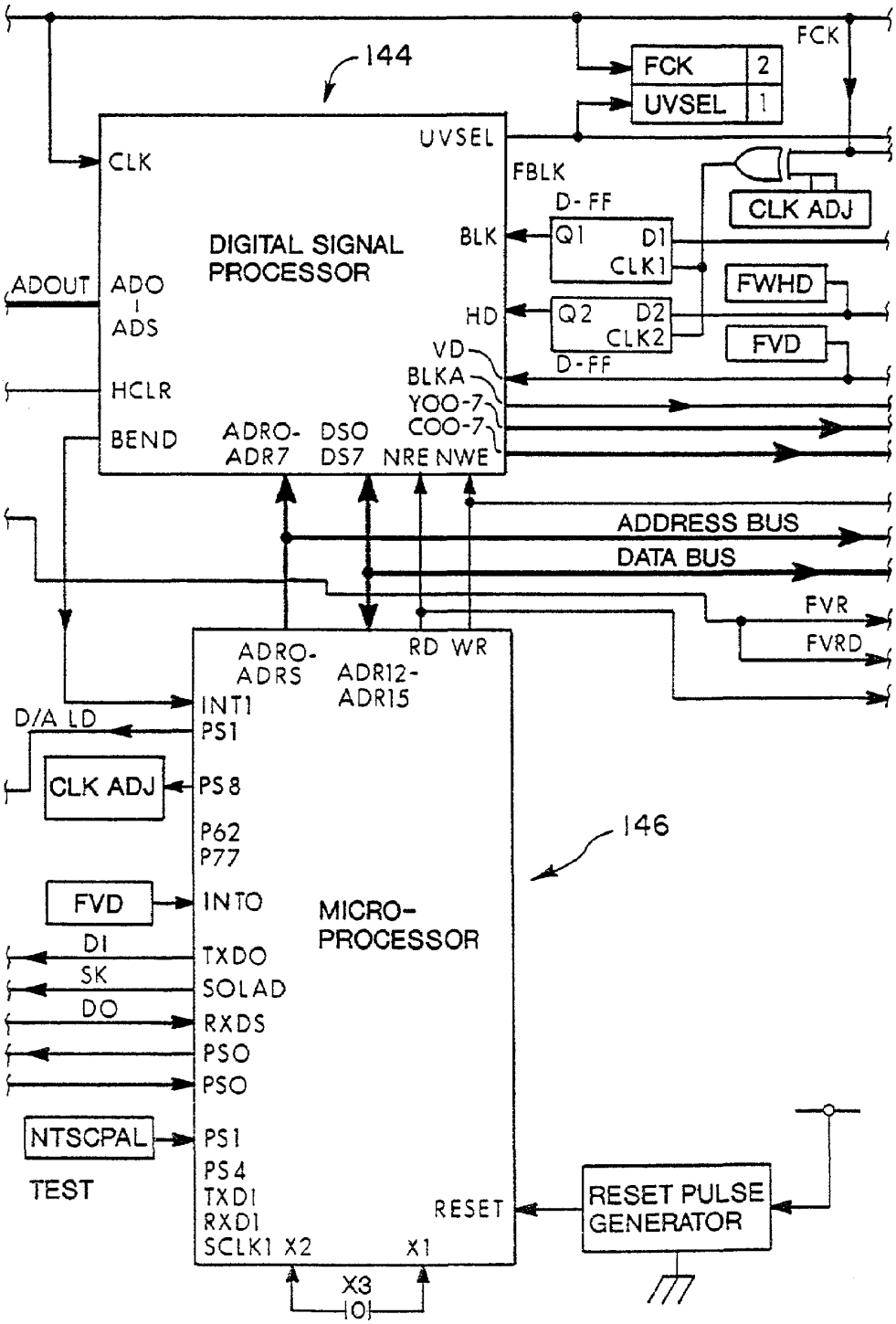

142
A/D CONVERTER
CLK
VIN
POWD
DO
DS
140
AGC CONTROL
PBLK
CP21N
CP23N
CPOS
CDS IN
PBD
AMPQC
AGC CONT
08
TRAP
1.3V
3.0V
A/O OUT
Y OUT
AGC OUT
AMP IN
BUFFER
CP2
BUFFER
12-CH D/A CONVERTER
141
AQ 05
06
07
08
09
10
11
AQ03
AQ04
AQ01
AQ03
AQ012
FVR
FVRP
CA REF
3RS VADJ
SVADJ
LD
CLK
D1
EEPROM
DI
TR
DO
CS
ESSY
R
143

Fig. 5c


144
FCK
FCK 2
UVSEL 1
UVSEL
CLK
FBLK
D-FF
CLK ADJ
DIGITAL SIGNAL PROCESSOR
BLK
Q1 D1 CLK1
FWHD
ADOUT
ADO
ADS
HD
Q2 D2 CLK2
FVD
VD
D-FF
HCLR
BLKA
YOO-7
BEND
ADRO-ADR7
DSO DS7
COO-7
NRE NWE
ADDRESS BUS
DATA BUS
FVR
FVRD
RD WR
ADRO-ADRS
ADR12-ADR15
INT1
D/A LD
PS1
CLK ADJ
PS8
P62
P77
146
FVD
INTO
MICRO-PROCESSOR
DI
TXDO
SK
SOLAD
DO
RXDS
PSO
PSO
NTSCPAL
PS1
PS4
TEST
TXD1
RXD1
RESET
RESET PULSE GENERATOR
SCLK1 X2
X1
X3

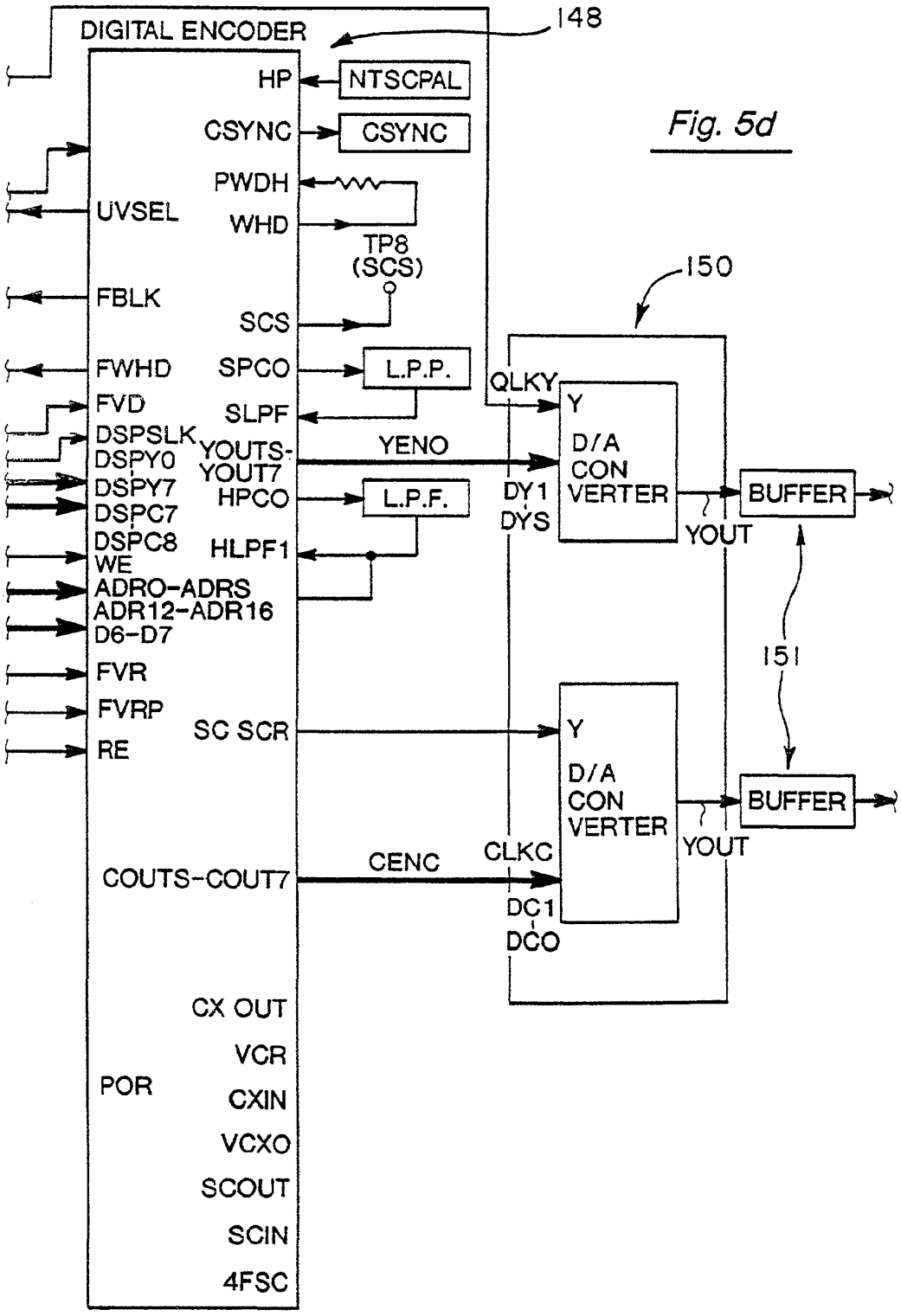

DIGITAL ENCODER
148
HP
NTSCPAL
CSYNC
CSYNC
PWDH
WHD
UVSEL
TP8
(SCS)
FBLK
SCS
150
FWHD
SPCO
L.P.P.
QLKY
FVD
SLPF
Y
DSPSLK
YOUTS-
YOUT7
YENO
D/A
CON
VERTER
DSPY0
DSPY7
DSPC7
HPCO
L.P.F.
DY1
DYS
BUFFER
YOUT
DSPC8
WE
HLPF1
ADRO-ADRS
ADR12-ADR16
D6-D7
151
FVR
FVRP
RE
SC SCR
Y
D/A
CON
VERTER
BUFFER
YOUT
CLKC
CENC
COUTS-COUT7
DC1
DCO
CX OUT
VCR
POR
CXIN
VCXO
SCOUT
SCIN
4FSC

Fig. 5d

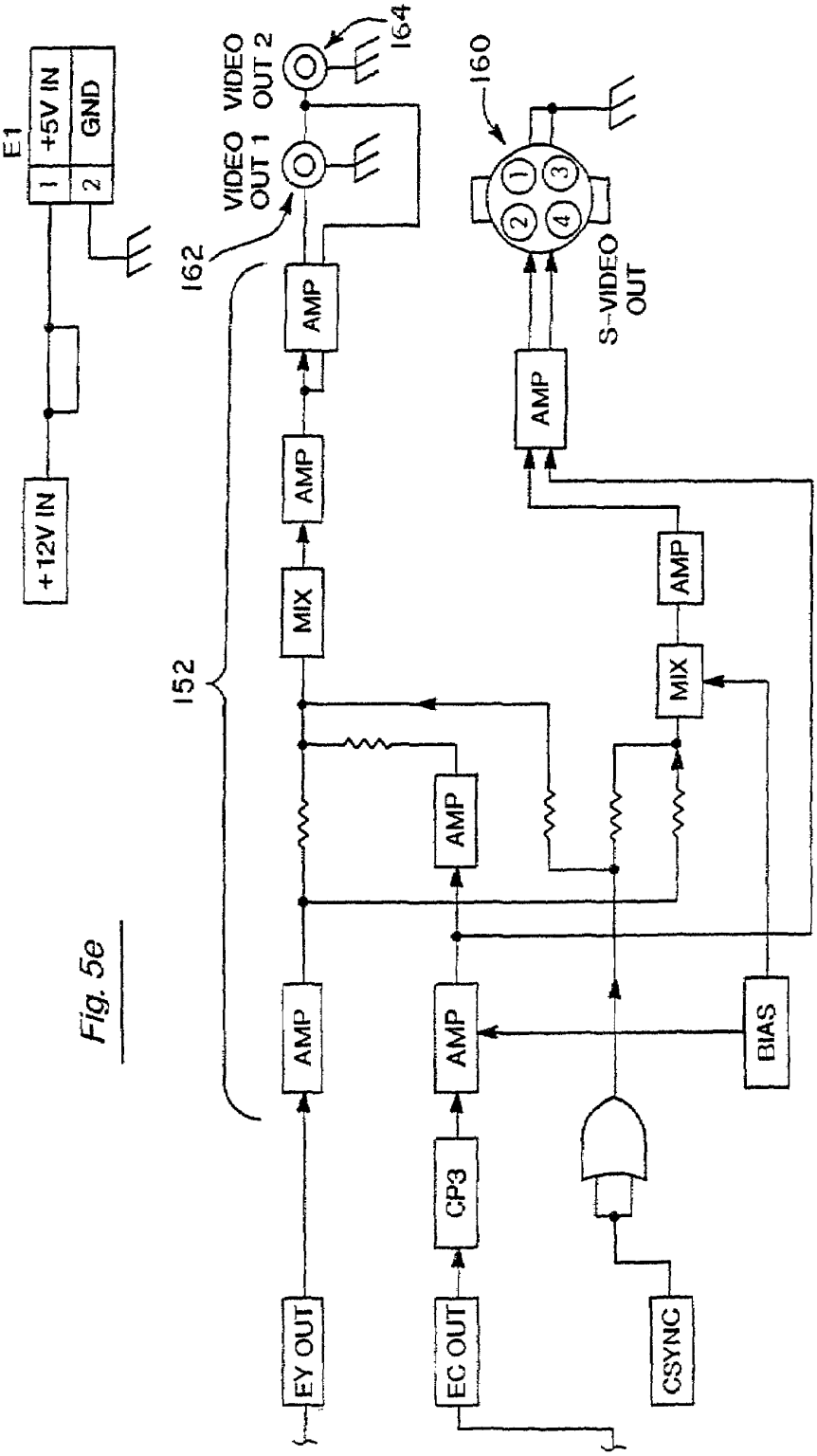

E1
+5V IN
GND
1
2
+12V IN
VIDEO OUT 2
VIDEO OUT 1
164
162
160
S-VIDEO OUT
AMP
MIX
152
BIAS
CP3
EY OUT
EC OUT
CSYNC

Fig. 5e

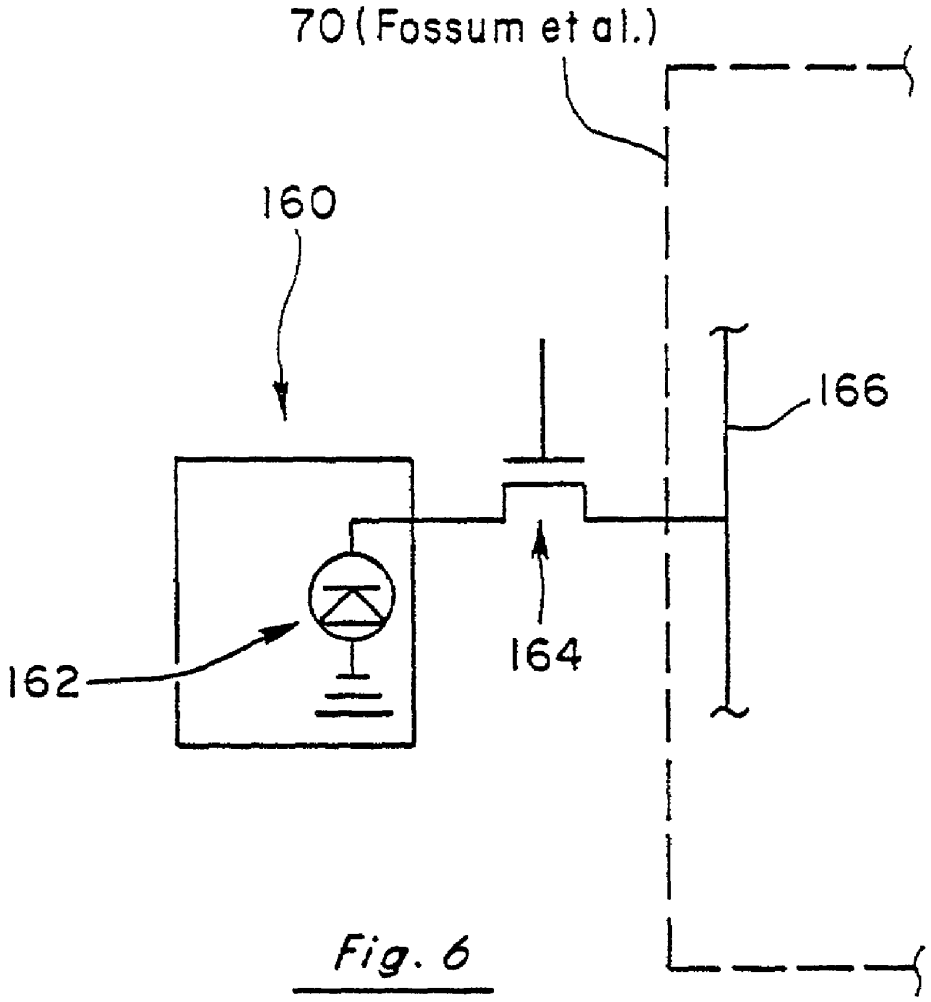


Fig. 6

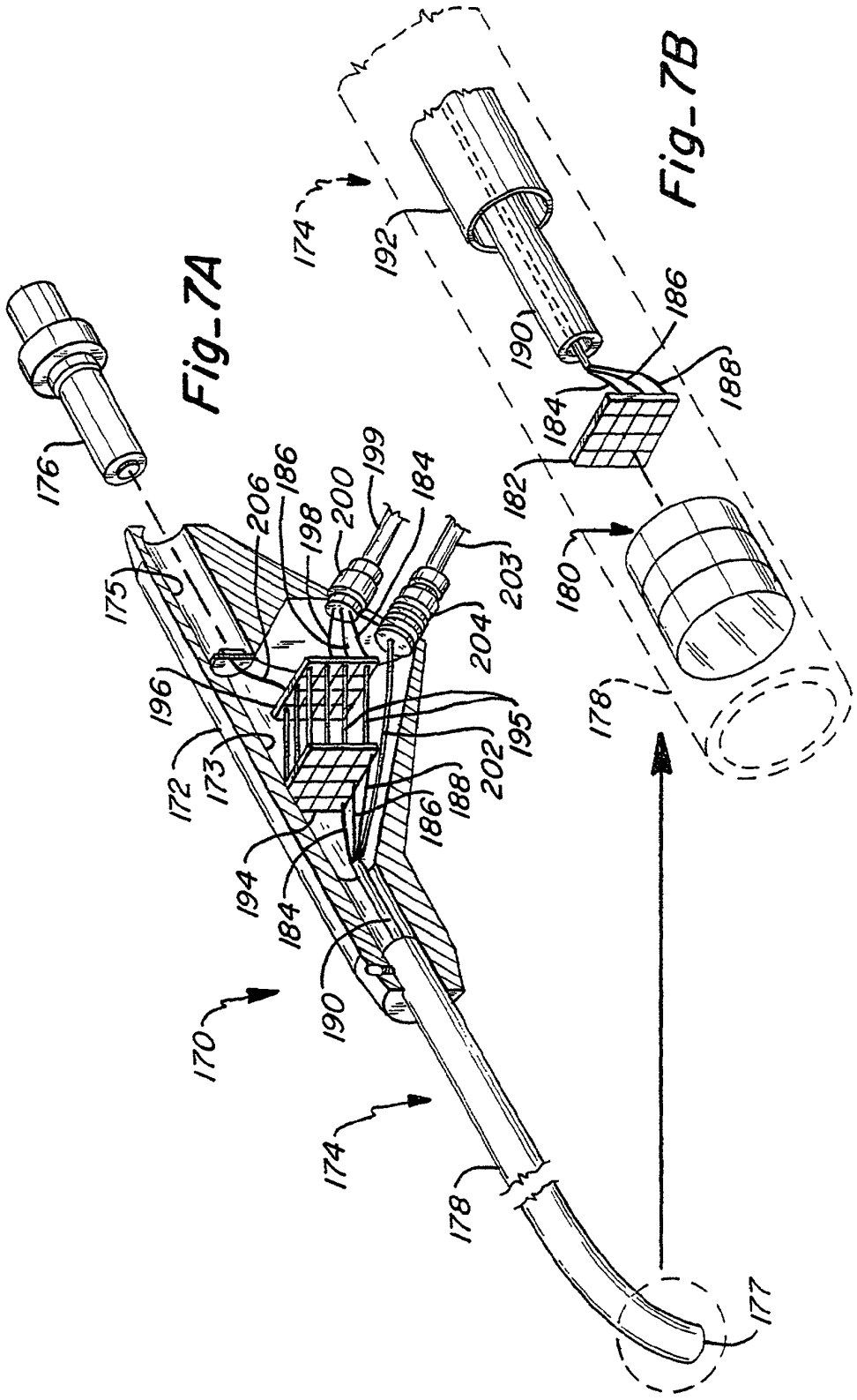


Fig_7A
Fig_7B
174
192
186
190
188
184
182
180
178
176
206
198
200
199
203
204
175
196
172
173
195
202
194
170
177

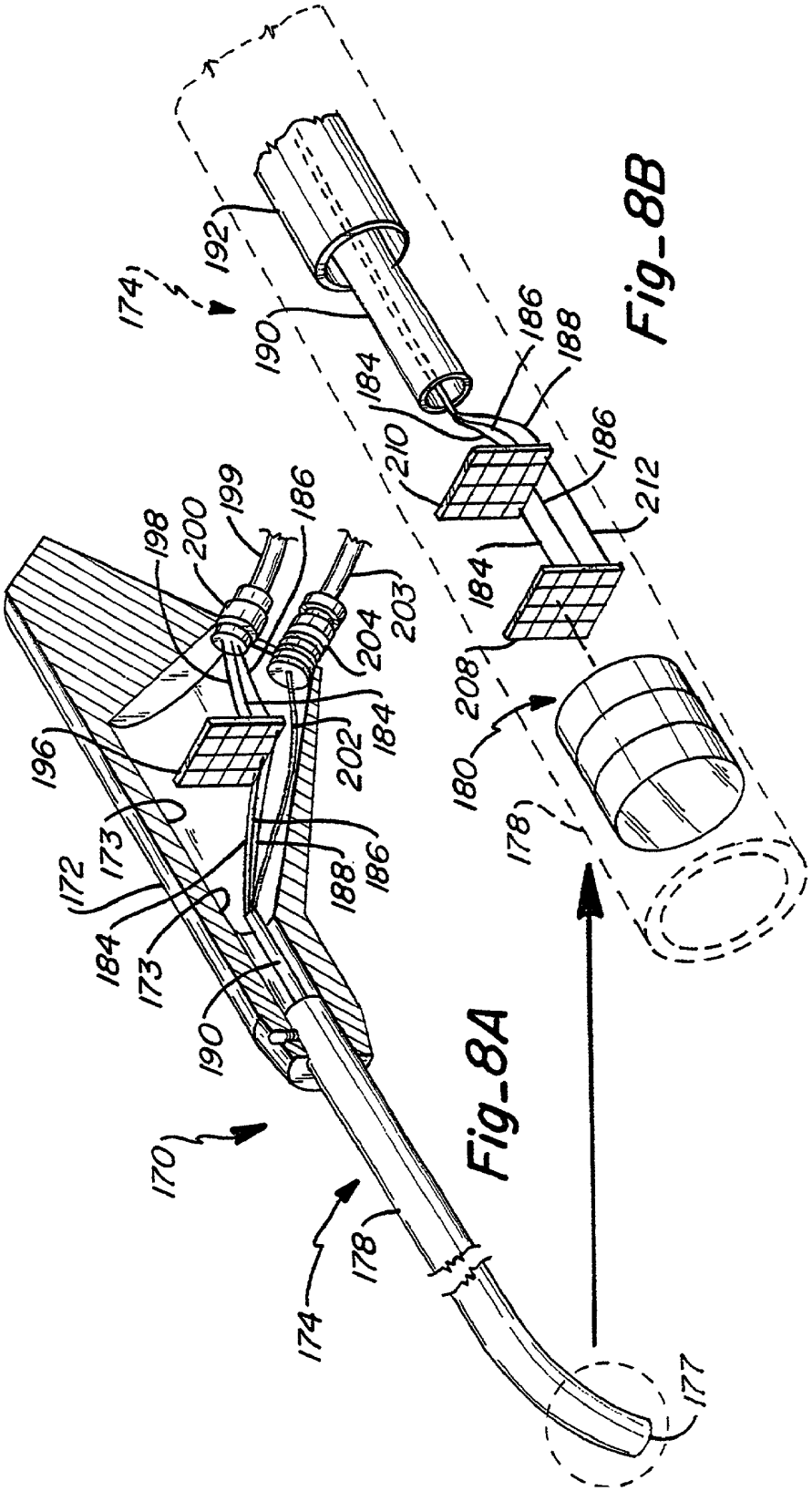

174
192
190
184
186
188
210
212
198
200
199
203
204
196
202
208
180
178
172
173
170
177

Fig_8B

Fig_8A

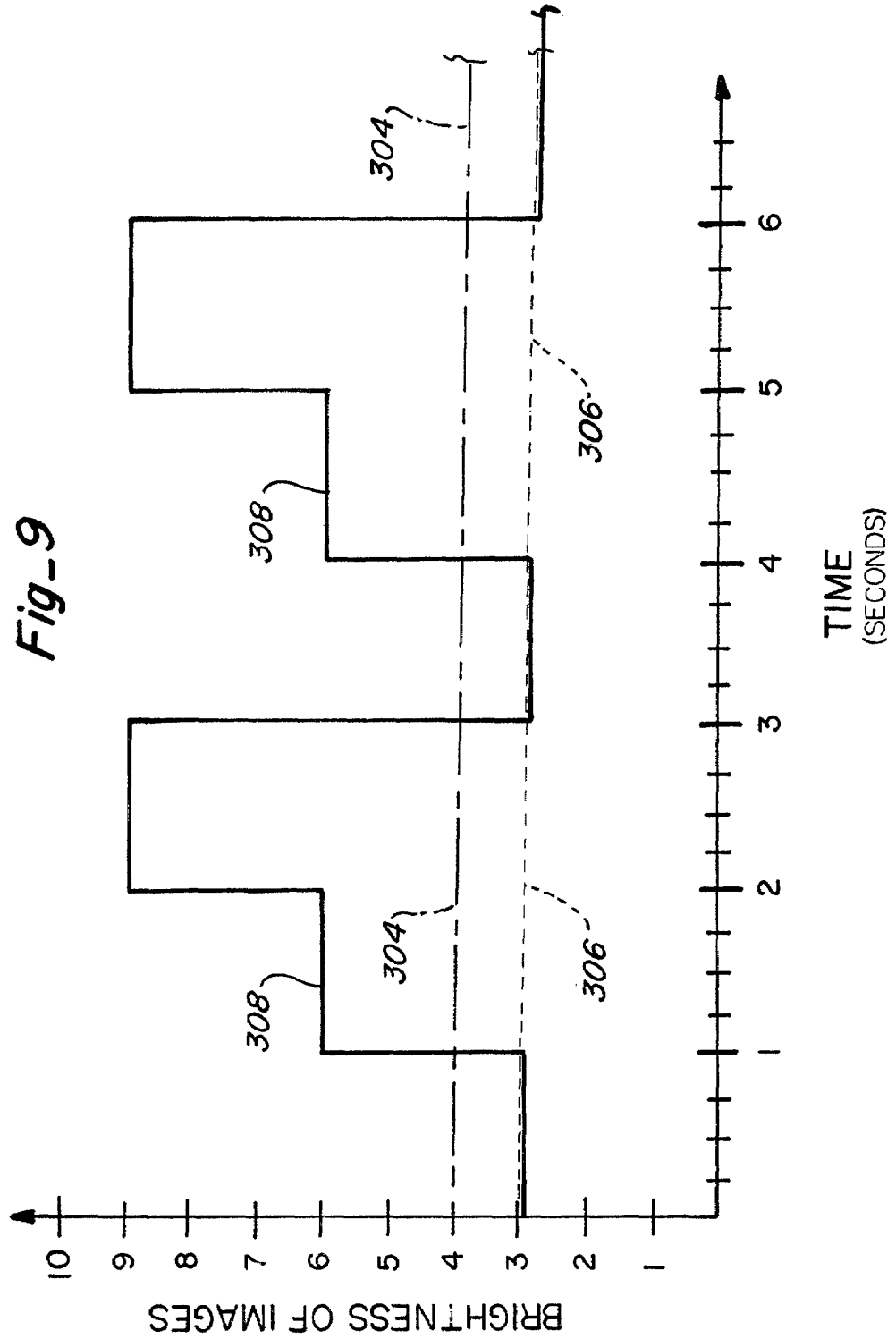


Fig_9
BRIGHTNESS OF IMAGES
10
9
8
7
6
5
4
3
2
1
TIME
(SECONDS)
1
2
3
4
5
6
304
306
308
304
306
308

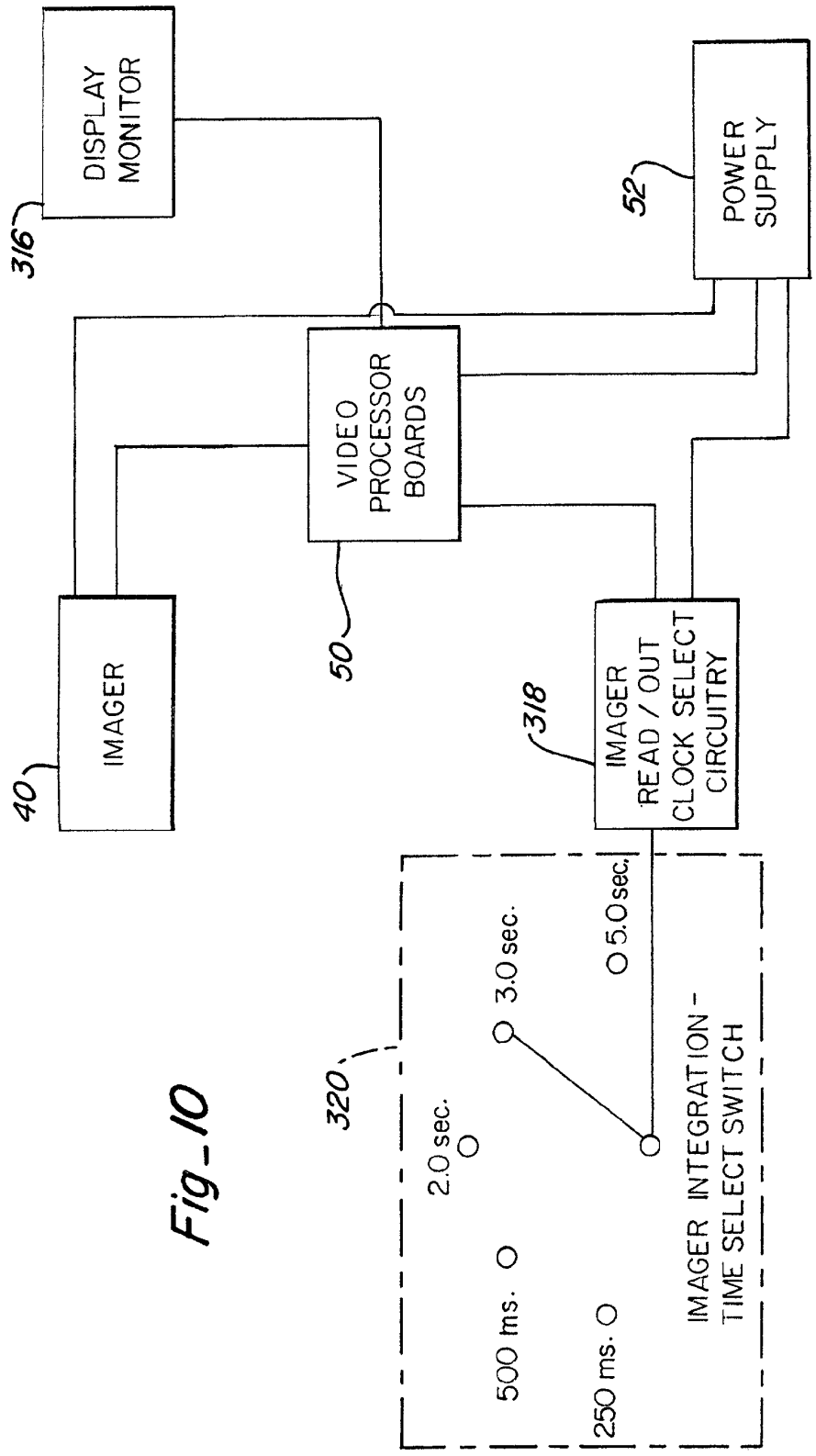

DISPLAY MONITOR
316
POWER SUPPLY
52
VIDEO PROCESSOR BOARDS
50
IMAGER
40
IMAGER READ / OUT CLOCK SELECT CIRCUITRY
318
320
2.0 sec.
3.0 sec.
5.0 sec.
500 ms.
250 ms.
IMAGER INTEGRATION - TIME SELECT SWITCH

Fig_10

REDUCED AREA IMAGING DEVICES UTILIZING SELECTED CHARGE INTEGRATION PERIODS

This application is a continuation-in-part application of U.S. Ser. No. 09/368,246, filed on Aug. 3, 1999, now U.S. Pat. No. 6,310,642 and entitled "Reduced Area Imaging Device Incorporated Within Surgical Instruments", which is a continuation-in-part of U.S. Ser. No. 08/976,976, filed Nov. 24, 1997, and entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments", now U.S. Pat. No. 5,986,693. This application is also a continuation-in-part application of U.S. Ser. No. 09/586,768, filed on Jun. 1, 2000 now U.S. Pat. No. 6,316,215 and entitled "Methods of Cancer Screening Utilizing Fluorescence Detection Techniques and Selectable Imager Charge Integration Periods"

TECHNICAL FIELD

This invention relates to solid state image sensors and associated electronics, and more particularly, to solid state image sensors which are configured to be of a minimum size, and which utilize selectable charge integration periods.

BACKGROUND ART

In recent years, endoscopic surgery has become the accepted standard for conducting many types of surgical procedures, both in the medical and dental arenas. The availability of imaging devices enabling a surgeon or dentist to view a particular surgical area through a small diameter endoscope which is introduced into small cavities or openings in the body results in much less patient trauma as well as many other advantages.

In many hospitals, the rod lens endoscope is still used in endoscopic surgery. The rod lens endoscope includes a very precise group of lenses in an elongate and rigid tube which are able to accurately transmit an image to a remote camera in line with the lens group. The rod lens endoscope, because of its cost of manufacture, failure rate, and requirement to be housed within a rigid and straight housing, is being increasingly replaced by solid state imaging technology which enables the image sensor to be placed at the distal tip of the investigating device. The three most common solid state image sensors include charged coupled devices (CCD), charge injection devices (CID) and photo diode arrays (PDA). In the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use. CMOS imaging devices offer improved functionality and simplified system interfacing. Furthermore, many CMOS imagers can be manufactured at a fraction of the cost of other solid state imaging technologies.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels than CCDs or other solid state imagers. Another major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and being compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129. A further description of this passive pixel device may be found in co-pending application, Ser. No. 08/976,976, entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, Calif., has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News*, Jan. 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enable the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, Calif. A brief description of both of the processes developed by Stanford University and Amain Electronics can be found in

an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging*. This reference is also hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of endoscopic instruments in order to view areas in the body that are particularly difficult to access, and to further minimize patient trauma by an even smaller diameter invasive instrument.

It is one object of this invention to provide reduced area imaging devices which take advantage of "camera on a chip" technology, but rearrange the circuitry in a stacked relationship so that there is a minimum profile presented when used within a surgical instrument or other investigative device. It is another object of this invention to provide low cost imaging devices which may be "disposable." It is yet another object of this invention to provide reduced area imaging devices which may be used in conjunction with standard endoscopes by placing the imaging device through channels which normally receive other surgical devices, or receive liquids or gases for flushing a surgical area. It is yet another object of this invention to provide a surgical device with imaging capability which may be battery powered and only requires one conductor for transmitting a pre-video signal to video processing circuitry within or outside the sterile field of the surgical area.

It is yet another object of the invention to provide a reduced area imaging device which utilizes selected charge integration periods in order to enhance the image in terms of a desired brightness or intensity. In the treatment of cancer, fluorescent markers have been used to help identify cancerous tissue within a patient. One example of a prior art reference which discloses a method of detection and treatment of malignant and nonmalignant tumors is U.S. Pat. No. 5,211,938 to Kennedy et al. Specifically, this reference discloses a method of detection of malignant and nonmalignant lesions by photo-chemotherapy of protoporphyrin IX precursors. 5-amino levulinic acid (5-ALA) is administered to the patient in an amount sufficient to induce synthesis of protoporphyrin IX in the lesions, followed by exposure of the treated lesion to a photo activating light in the range of 350–640 nanometers. Naturally occurring protoporphyrin IX is activatable by light in the incident red light range which more easily passes through human tissue as compared to light of other wave lengths. An endoscopic procedure may then be used to locate the photo activated lesions.

Other methods relating to cancer screening using fluorescence detection systems require the use of interventional devices such as endoscopes which have the special capability of delivering specified light frequencies to a targeted area within a patient. These endoscopes illuminate the targeted part of the body in which cancer is suspected. The light illuminates the targeted area which has previously been subjected to some type of fluorescent marker, causing the malignant cells to illuminate or fluoresce under observation of light at the specified frequency.

One distinct disadvantage or problem associated with use of fluorescent markers to locate and treat cancerous tissue is that it is oftentimes difficult to locate the cancerous tissue at all locations, particularly when lesions are at their early stages in formation, or the cancerous tissue has not yet grown to an extent which creates an observable amount of fluorescence. Furthermore, because an endoscopic procedure is undertaken to locate and treat many lesions, the surgeon does not have an infinite amount of time to locate or treat a particular lesion. Therefore, a need exists for enhancing observable fluorescence as well as being able to use an imager of such a small size that fluorescence endoscopy can be used in a wide array of surgical procedures.

In addition to the intended use of the foregoing invention with respect to medical purposes, it is also contemplated that the invention described herein has great utility with respect to oral surgery and general dental procedures wherein a very small imaging device can be used to provide an image of particularly difficult to access locations. Additionally, while the foregoing invention has application with respect to the medical and dental fields, it will also be appreciated by those skilled in the art that the small size of the imaging device set forth herein can be applied to other functional disciplines wherein the imaging device can be used to view difficult to access locations for industrial equipment and the like. Therefore, the imaging device of this invention could be used to replace many industrial boroscopes.

The "camera on a chip" technology can be furthered improved with respect to reducing its profile area and incorporating such a reduced area imaging device into very small investigative instruments which can be used in the medical, dental, or other industrial fields.

DISCLOSURE OF THE INVENTION

In accordance with the present invention, reduced area imaging devices are provided. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by a standard video device such as a television or video monitor accompanying a personal computer. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first embodiment, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of the endoscopic instrument while the remaining pro-

cessing circuitry may be found in a small remote control box which may communicate with the image sensor by a single cable.

In a second embodiment, the image sensor and the processing circuitry may all be placed in a stacked arrangement of circuit boards and positioned at the distal tip of the endoscopic instrument. In this embodiment, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other circuit boards. Alternatively, the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In another embodiment, the imaging device may be adapted for use with a standard rod lens endoscope wherein the imaging device is placed within a standard camera housing which is configured to connect to a standard "C" or "V" mount connector.

In yet another embodiment, the imaging device may be configured so that the processing circuitry is placed in the handle of the endoscope, which eliminates the necessity of having a remote box when the processing circuitry is remote from the pixel array. In this embodiment, the pixel array and the timing and control circuitry are placed at the distal tip of the endoscopic instrument, while the processing circuitry is placed within the handle of the endoscope.

For each of the embodiments, selected charge integration periods may be used to enhance the image to a desired brightness or intensity. Particularly in the field of medical fluorescence detection, the ability to adjust charge integration periods greatly enhances the ability to observe fluorescence from a group of cells which might otherwise be unobservable with normal or preset integration periods.

While the imager may be used within an endoscopic instrument, it is also contemplated that the image sensor may be incorporated within a microscope, or another imaging device which is used to view cell cultures and the like. Most commonly available fluorescence microscopes include CCD type imagers which are not capable of the variable charge integration. CCD imagers are charge storage and transfer devices wherein the detector signal produced is representative of the total light impinging or falling upon the pixel array during a preset exposure time. Because of the construction of CCD devices, these exposure times cannot be manipulated for charge integration because CCD imagers have destructive readout. In other words, each charge is read by transferring the collected charge in each pixel in a serial fashion to a readout amplifier. The same photon generated charge collected at the pixel site is transferred (coupled) pixel by pixel, one at a time, in a predesignated sequence that cannot be interrupted. When the pixel charge sequence is transferred to the readout amplifier, the pixel charge is destroyed. For CID (charge injection device) imagers, pixels accumulate charge which is injected into the substrate. Pixels in CID imagers can be individually accessed; however, in doing so, the charge is not destroyed by actual charge transfer, but is sensed and then replaced so that the integration process is not disturbed. Light continues to be collected for the preset integration period while the pixels continue to be monitored. This nondestructive readout capability of CID imagers makes it possible to carry out real time exposure monitoring and it also allows integration periods to be varied such that longer integration periods represent greater amounts of light being collected in the pixels.

By having the capability to adjust the integration periods, fluorescence detection can be enhanced by choosing an integration time which maximizes observable fluorescence. CMOS imagers also have variable charge integration capability to enhance observed fluorescence. As with CID imagers, integration periods in CMOS imagers may be varied, and fluorescence detection can be enhanced by choosing an integration period which maximizes the same. These CMOS imagers, as well as commercially available CMOS-CID imagers such as those manufactured by CIDTEC of Liverpool, NY can be modified to include an imager integration time select switch which allows an operator to preselect a desired integration period which maximizes observable fluorescence. The imagers sold by CIDTEC are "camera on a chip" type CMOS devices. The imager integration time select switch is coupled to video processing circuitry by clock select circuitry which varies the integration period as selected by the operator. Representative integration periods might include 250 milliseconds, 500 milliseconds, 2 seconds, 3 seconds and 5 seconds. The operator would adjust the integration periods to maximize the observed fluorescence. For example, an integration period selected at 5 seconds would result in charge being accumulated in the pixels of the imager for a 5-second period and thus, the observed fluorescence intensity would be greatly increased in comparison to standard readout cycles for CCD devices which may only be one-sixtieth of a second.

In a CMOS-CID device, photon charge collected by the photo-diodes are injected into the pixel substrate and stored. The photo-diodes continue to collect charge and transfers the charge into the substrate. The charge stored in the substrate continues to accumulate from the photo-diodes until the chosen integration period ends (i.e., the integration period selected by the user). At that time, the pixels are read out and the integration process begins again. Readout clock select circuitry creates a frequency which is fed into a series of CMOS divider circuits which divide the clock frequency down to a user selected clock rate. The user selected clock rate would correspond to the select switch positions enabling the operator to have a choice of a plurality of integration time periods. Because CMOS pixels can be accessed individually, the image can be updated as desired through various update cycles within the display monitor, while continuing to wait for the read out signal from the imager without disturbing the selected integration period. The user selectable integration time switch can be mounted as desired based upon the particular configuration of the imaging device. In the configuration of the imaging device which may utilize a control box, the integration time switch could be mounted on the front panel of the control box, and the additional circuitry required for charge integration would simply be incorporated within the control box. In the configuration of the imaging device in which all of the processing circuitry is housed within the particular endoscope or other instrument, the switch could simply be mounted on the handle of the instrument. Published papers which provide good background information on charge injection devices include "Charge Injection Devices for Use in Astronomy", by Z. Ninkov et al., *SPIE Proceedings,* 1994, Publication No. 2198, Vol. 868; and "Evaluation of a Charge Injection Device Array", by Z. Ninkov et al., *SPIE Proceedings,* 1994, Publication No. 2172, Vol. 15. These two papers are hereby incorporated by reference.

For use of the imaging device in endoscopy, a generic endoscope may be used which includes a very small diameter tubular portion which is inserted within the patient. The tubular portion may be made of a flexible material having a central lumen or opening therein for receiving the elements of the imaging device. The tubular portion may be modified

to include an additional concentric tube placed within the central lumen and which enables a plurality of light fibers to be placed circumferentially around the periphery of the distal end of the tubular portion. Additionally, control wires may extend along the tubular portion in order to make the endoscope steerable. The material used to make the endoscope can be compatible with any desired sterilization protocol, or the entire endoscope can be made sterile and disposable after use.

For the configuration of the imaging device which calls for the array of pixels and the timing and control circuitry to be placed on the same circuit board, only one conductor is required in order to transmit the image signal to the processing circuitry. In the other configuration of the imaging device wherein the timing and control circuits are incorporated onto other circuit boards, a plurality of connections are required in order to connect the timing and control circuitry to the pixel array and the one conductor is also required to transmit the image signal.

In addition to use of the imaging device in endoscopy, it is also contemplated that the imaging device of the invention can be incorporated within a microscope which may be used to analyze cell cultures and the like. Although size is not as much of a concern with use of the imaging device within a microscope, there are still great advantages to be obtained by providing the imaging device with selected charge integration periods to intensify the brightness of an image in fluorescence detection of cell culture media which has no observable fluorescence as observed under standard integration periods.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1***a* illustrates a first embodiment including a fragmentary cross-sectional view of a generic endoscopic instrument, and a fragmentary perspective view of a control box, the endoscope and control box each incorporating elements of a reduced area imaging device;

FIG. **1***b* is an enlarged fragmentary partially exploded perspective view of the distal end of the endoscopic instrument specifically illustrating the arrangement of the image sensor with respect to the other elements of the tubular portion of the endoscope;

FIG. **2***a* is a fragmentary cross-sectional view of a second embodiment of this invention illustrating another generic endoscope wherein the imaging device is incorporated in its entirety at the distal tip of the endoscope;

FIG. **2***b* is an enlarged fragmentary partially exploded perspective view of the distal end of the endoscope of FIG. **2***a* illustrating the imaging device;

FIG. **3***a* is an elevational fragmentary cross-sectional view of the image sensor incorporated with a standard camera housing for connection to a rod lens endoscope;

FIG. **3***b* is a fragmentary cross-sectional view of the imaging device incorporated within the camera housing of FIG. **3***a;*

FIG. **3***c* is a fragmentary cross-sectional view similar to that of FIG. **3***b* illustrating a battery as an alternate source of power;

FIG. **4** is a schematic diagram of the functional electronic components which make up the imaging device;

FIG. **4***a* is an enlarged schematic diagram of a circuit board which may include the array of pixels and the timing and control circuitry;

FIG. **4***b* is an enlarged schematic diagram of a video processing board having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted by a standard video device;

FIGS. **5***a*–**5***e* are schematic diagrams that illustrate an example of specific circuitry which may be used to make the imaging device.

FIG. **6** is a simplified schematic diagram of a passive pixel which may be placed in an array of passive pixels compatible with an imager of CMOS type construction;

FIG. **7***a* illustrates another preferred embodiment including a fragmentary cross-sectional view of a generic endoscope wherein the handle of the endoscope houses processing circuitry of the imaging device;

FIG. **7***b* is an enlarged fragmentary partially exploded perspective view of the distal end of the endoscope specifically illustrating the arrangement of the image sensor with respect to the other elements of the tubular portion of the endoscope;

FIG. **8***a* is another fragmentary cross-sectional view of the generic endoscope of FIG. **7***a*, but showing only one processing circuitry element within the handle of the endoscope;

FIG. **8***b* is an enlarged fragmentary partially exploded perspective view of the distal end of the endoscope of FIG. **8***a* specifically illustrating the array of pixels being placed on one planar structure, and the timing and control circuitry being placed on another planar structure adjacent to the pixel array;

FIG. **9** is a graphical representation of how variable charge integration periods can enhance the capability to observe light or fluorescence from a viewed area; and

FIG. **10** is a schematic diagram illustrating incorporation of variable charge integration capability with the imaging device of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In accordance with one embodiment of the invention as shown in FIG. **1***a*, an endoscope **10** is provided which incorporates a reduced area imaging device **11**, shown in FIG. **1***b*. As further discussed below, the elements of the imaging device may all be found at one location or the elements may be separated from one another and interconnected by the appropriate cable(s). The array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. The structure of the endoscope **10** includes a flexible or rigid tubular portion **14** which is inserted into the body of the patient and is placed at the appropriate location for viewing a desired surgical area. The tubular portion **14** attaches at its proximal end to a handle portion **12** which may be grasped by a surgeon who is conducting the endoscopic procedure. The handle **12** may include a central lumen or channel **13** which receives therethrough one or more cables or other structures which extend to the distal end **16** of tubular portion **14**. Handle portion **12** may further include a supplementary channel **15** which intersects with central channel **13** and which may provide another point of entry for other cables, fluids or operative instruments to be placed through the endoscope.

FIG. **1***b* illustrates the distal end of the endoscope **16**. The distal end **16** may be characterized by an outer tube **18** which traverses the length of the tubular portion **14** and connects to the handle portion **12**. Placed concentrically within the outer

tube **18** may be one or more inner tubes **20**. In FIG. **1***b*, the gap between inner tube **20** and outer tube **18** forms a space in which one or more light fibers **22** or control wires **24** may be placed. As well understood by those skilled in the art, a plurality of circumferentially spaced light fibers as illustrated in FIG. **1***b* can be used to illuminate the surgical site. Additionally, the control wires **24** may communicate with a control mechanism (not shown) integrated on the handle portion **12** for manipulating the distal end **16** of the endoscope in a desired direction. The flexible tubular portion **14** coupled with a steerable feature enables the endoscope to be placed within winding bodily passages or other locations difficult to reach within the body.

An image sensor **40** may be placed within the central channel defined by inner tube **20**. In the configuration shown in FIG. **1***b*, a cable **26** is used to house the conductors which communicate with the image sensor **40**. An intermediate support tube **28** may be placed concentrically outside of cable **26** and concentrically within inner tube **20** to provide the necessary support for the cable **26** as it traverses through the inner channel defined by inner tube **20**. In lieu of support tube **28**, other well-known means may be provided to stabilize the cable **26** such as clips or other fastening means which may attach to the inner concentric surface of inner tube **20**.

A control box **30** may be placed remote from the endoscope **10**. The control box **30** contains some of the processing circuitry which is used to process the image signal produced by image sensor **40**. Therefore, the imaging device **11** as previously defined would include the processing circuitry within control box **30** and the image sensor **40** located at the distal tip of the endoscope. Control box **30** communicates with image sensor **40** by means of cable **32** which may simply be an insulated and shielded cable which houses therein cable **26**. Cable **32** is stabilized with respect to the handle portion **12** by means of a fitting **34** which ensures that cable **32** cannot be inadvertently pushed or pulled within channel **13**. Additionally, an additional fitting **35** may be provided to stabilize the entry of a light cable **36** which houses the plurality of light fibers **22**.

Image sensor **40** is illustrated as being a planar and square shaped member. However, the image sensor may be modified to be in a planar and circular shape to better fit within the channel defined by inner tube **20**. Accordingly, FIG. **1***b* further shows an alternate shaped image sensor **40'** which is round. A lens group or system **42** may be incorporated at the distal end of the endoscope in order to manipulate the image prior to it being impinged upon the array of pixels on the image sensor **40**. This lens system **42** may be sealed at the distal end **16** of the endoscope so that the tubular portion **14** is impervious to fluids entering through the distal end **16**. In the configuration of the imaging device **11** in FIGS. **1***a* and **1***b*, there are only three conductors which are necessary for providing power to the image sensor **40**, and for transmitting an image from the image sensor **40** back to the processing circuitry found within control box **30**. Namely, there is a power conductor **44**, a grounding conductor **46**, and an image signal conductor **48** each of which are hard wired to the image sensor. Thus, cable **26** may simply be a three-conductor 50 ohm cable.

Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most endoscopic procedures would dictate that the image sensor **40** be between 4 mm to 8 mm in its largest dimension. The image signal transmitted from the image sensor through conductor **48** is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor **40** by means of conductor **48**, it is received by video processing board **50**. Video processing board **50** then carries out all the necessary conditioning of the pre-video signal and places it in a form so that it may be viewed directly on a standard video device, television or standard computer video monitor. The signal produced by the video processing board **50** can be further defined as a post-video signal which can be accepted by a standard video device. As shown in FIG. **1***a*, a conductor **49** is provided which transmits the post-video signal to an output connector **58** on the exterior surface of control box **30**. The cable (not shown) extending from the desired video device (not shown) may receive the post-video signal by means of connector **58**. Power supply board **52** may convert incoming power received through power source **54** into the desired voltage. In the preferred imager incorporated in this invention, the power to the imaging device is simply a direct current which can be a 1.5 volt to a 12 volt source. Incoming power from, for example, a wall receptacle, communicates with power supply board **52** by connector **56**. Power supply board **52** takes the incoming power source and regulates it to the desired level. Additionally, ground **46** is also shown as extending back to the source of power through connector **56**.

FIG. **2***a* illustrates a second embodiment of this invention wherein the imaging device is self-contained entirely within the distal end **16** of the endoscope, and a power source which drives the circuitry within the imaging device may come from a battery **66** housed within handle portion **12**.

As shown in FIG. **2***b*, the video processing board **50** may be placed directly behind image sensor **40**. A plurality of pin connectors **62** serve to electrically couple image sensor **40** with video processing board **50** depending upon the specific configuration of image sensor **40**, pin connectors **62** may be provided either for structural support only, or to provide a means by which image signals are transmitted between image sensor **40** and board **50**. When necessary, one or more supplementary boards **60** may be provided which further contain processing circuitry to process the image signal and present it in a form which may be directly received by a desired video device. The area which is occupied by image sensor **40** may be defined as the profile area of the imaging device and which determines its critical dimensions. Any imaging elements that are found on boards **50** or **60** must be able to be placed on one or more circuit boards which are longitudinally aligned with image sensor **40** along longitudinal axis XX. If the profile area is not critical in terms of limiting the largest sized imaging element within the imaging device, then the additional circuit boards **50** and **60** which are normally placed in line with image sensor **40** can be aligned in an offset manner or may be larger than the profile area of image sensor **40**. In the configuration of FIG. **2***b*, it is desirable that elements **40**, **50** and **60** be approximately the same size so that they may fit uniformly within the central channel of the endoscope. Additionally, image sensor **40** may be bonded to lens system **42** in order to provide further structural support to the imaging device **11** when mounted within the distal end **16**.

Referring back to the handle portion **12** in FIG. **2***a*, an additional channel **64** may be provided in order that a power supply cable **68** may communicate with battery **66**. Conveniently, battery **66** may itself be mounted within a well **65** formed in handle portion **12**. Cable **68** carries the conductor **44** and ground **46**. Cable **68** may intersect with cable **33** within channel **13**, cables **68** and **33** extending then to the distal end **16**. Cable **33** can be a single conductor cable which transmits the post-video signal to a desired video device. In other words, cable **33** may simply be an insulated

and shielded housing for conductor **49** which carries the post-video signal. Because a preferred image sensor of the imaging device **11** may only require a 5 volt power supply, a battery is an ideal power source in lieu of a conductor which would trail the endoscope. Accordingly, the endoscope is made more mobile and easier to handle by eliminating at least one of the trailing cables.

FIG. **3***a* illustrates yet another preferred embodiment of this invention, wherein the imaging device can be used in conjunction with a standard rod lens endoscope **70**. As shown, rod lens endoscope **70** includes a lens train **72** which includes a plurality of highly precise lenses (not shown) which are able to transmit an image from the distal end of the endoscope, to a camera in line with the endoscope. The rod lens endoscope is equipped with a light guide coupling post **74**. Light guide post **74** connects to a source of light in the form of a cable **77** having a plurality of fiber optic strands (not shown) which communicate with a source of light (not shown). The most common arrangement of the rod lens endoscope also includes a "C" or "V" mount connector **78** which attaches to the eyepiece **76**. The "C" or "V" mount attaches at its other end to a camera group **80**. The camera group **80** houses one or more of the elements of the imaging device. In this embodiment, the small size of the imaging device is not a critical concern since the imaging device is not being placed at the distal end of the endoscope. However, the incorporation of the imaging device in a housing which would normally hold a traditional camera still provides an advantageous arrangement. As shown, the camera group **80** may include a housing **82** which connects to a power/video cable **86**. Fitting **87** is provided to couple cable **86** to the interior elements of the camera group **80** found within housing **82**. FIG. **3***a* illustrates an arrangement of the imaging device **11** wherein the image sensor **40** is placed by itself within the housing **82** and the processing circuitry of the imaging device can be positioned in a remote control box as shown in FIG. **1***a*. Accordingly, only three conductors **44**, **46** and **48** are necessary for providing power to the image sensor **40** and for transmitting the pre-video signal to the control box. Alternatively, as shown in FIG. **3***b*, the entire imaging device **11** may be incorporated within camera group **80**, each of the elements of the imaging device being placed in the stacked arrangement similar to FIG. **2***b*. As discussed above, size is not as much of a concern in the embodiment of FIGS. **3***a* and **3***b* since the camera group housing **82** is much larger than the distal tip of the endoscope of FIGS. **1***a* and **2***a*.

FIG. **3***c* also illustrates the use of a battery **66** which provides source of power to the imaging device in either FIG. **3***a* or **3***b*. In this arrangement, housing **82** is altered to include a battery housing **69** which houses the battery **66** therein. Battery housing **69** may include a very small diameter channel which may allow conductor **48** or **49** to communicate directly with the processing circuitry or video device, respectively. It will also be understood that the embodiment in FIG. **1***a* may incorporate the use of a battery **66** as the source of power. Thus, handle **12** in FIG. **1***a* may be altered in the same way as housing **82** to allow a battery to be attached to the handle portion **12**.

FIG. **4** is a schematic diagram illustrating one way in which the imaging device **11** may be constructed. As illustrated, the image sensor **40** may include the timing and control circuits on the same planar structure. Power is supplied to image sensor **40** by power supply board **52**. The connection between image sensor **40** and board **52** may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors **44** and **46**. The output from image sensor **40** in the form of the pre-video signal is input to video processor board **50** by means of the conductor **48**. In the configuration of FIG. **4**, conductor **48** may simply be a 50 ohm conductor. Power and ground also are supplied to video processing board **50** by conductors **44** and **46** from power supply board **52**. The output signal from the video processor board **50** is in the form of the post-video signal and which may be carried by conductor **49** which can also be a 50 ohm conductor.

In the first embodiment illustrated in FIG. **1***a*, cable **32** can be used to house conductors **44**, **46** and **48**. In the embodiment shown in FIG. **2***a*, cable **33** can be used to house conductor **49** by itself when a battery power source is used, or alternatively, cable **33** may house conductors **44**, **46** and **49** if the embodiment of FIG. **2***a* utilizes a power source from board **52**.

Optionally, a supplementary processing board **60** may be provided to further enhance the pre-video signal. As shown in FIG. **4**, the supplementary board **60** may be placed such that the pre-video signal from image sensor **40** is first sent to the supplementary board and then output to the video processor board **50**. In this case, the output from board **50** can be carried along conductor **51**. This output can be defined as an enhanced pre-video signal. Furthermore, the post-video signal from video processor board **50** may return to the supplementary board **60** for further processing, as further discussed below. The conductor used to transmit the post-video signal back to the supplementary board is shown as conductor **59**. The power supply board **52** may also provide power to the supplementary board in the same manner as to image sensor **40** and board **50**. That is, a simple hard-wired connection is made onto the supplementary board for the ground and voltage carrying conductors. As discussed above, image sensor **40** may be placed remotely from boards **50** and **60**. Alternatively, image sensor **40**, and boards **50** and **60** each may be placed within the distal end of the endoscope.

Although FIG. **4** illustrates the image sensor and the timing and control circuits being placed on the same planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board **50**. The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor **40** and the rest of the imaging device, namely, conductors **44**, **46** and **48**. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the video processing board **50** in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50 ohm coaxial cables (not shown) must be used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

FIG. **4***a* is a more detailed schematic diagram of image sensor **40** which contains an array of pixels **90** and the timing and control circuits **92**. One example of a pixel array **90** which can be used within the invention is similar to that which is disclosed in U.S. Pat. No. 5,471,515 to Fossum, et

al., said patent being incorporated by reference herein. More specifically, FIG. 3 of Fossum, et al. illustrates the circuitry which makes up each pixel in the array of pixels **90**. The array of pixels **90** as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board **50** for further processing.

Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

The timing and control circuits **92** are used to control the release of the image information or image signal stored in the pixel array. In the image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns which contain the consolidated information from the rows. As shown in FIG. **4***a*, the control of information consolidated from the rows is achieved by latches **94**, counter **96**, and decoder **98**. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch **94** is enabled, it will allow the transfer of electrons to the decoder **98**. The counter **96** is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits **92**. When the counter **96** has reached its set point or overflows, the image information is allowed to pass through the latches **94** and be sent to the decoder **98** which places the consolidated information in a serial format. Once the decoder **98** has decoded the information and placed it in the serial format, then the row driver **100** accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches **94** will initially allow the information stored in each pixel to be accessed. The counter **96** then controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder **98** then knows to take the information and place it in the serial format. The whole process is repeated, based upon the timing sequence that is programmed. When the row driver **100** has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also controlled by a series of latches **102**, a counter **104** and a decoder **106**. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board **50**. This serial format of column information is the pre-video signal carried by conductor **48**. The column signal conditioner **108** places the column serial information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner **108** only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits **92** may simply be a quartz crystal timer. This clock input is divided into many other frequencies for use by the various counters. The run input to the timing and control circuit **92** may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the surgeon.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech Briefs, October* 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor **40** has created the pre-video signal, it is sent to the video processing board **50** for further processing. At board **50**, as shown in FIG. **4***b*, the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters **114** and **116**, and a band pass filter **112**. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector **120** and white balance circuit **124**, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter **114** then travels through gain control **118** which reduces the magnitude or amplitude of this portion to a manageable level. The output from gain control **118** is then fed back to the white balance circuit **124**. The portion of the signal traveling through filter **116** is placed through the processor **122**. In the processor **122**, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer **132**. Any chroma portion of the signal is held in processor **122**.

Referring to the output of the white balance circuit **124**, this chroma portion of the signal is sent to a delay line **126** where the signal is then further reduced by switch **128**. The output of switch **128** is sent through a balanced modulator **130** and also to the Y chroma mixer **132** where the processed chroma portion of the signal is mixed with the processed non-chroma portion. Finally, the output from the Y chroma mixer **132** is sent to the NTSC/PAL encoder **134**, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y chroma mixer **132** in encoder **134** to produce the post-video signal which may be accepted by a television.

Referring back to FIG. **4**, it further illustrates supplementary board **60** which may be used to digitally enhance or otherwise further condition the pre-video signal produced from image sensor **40**. For example, digital enhancement can brighten or otherwise clarify the edges of an image viewed on a video screen. Additionally, the background images may be removed thus leaving only the foreground images or vice versa. The connection between image sensor **40** and board **60** may simply be the conductor **48** which may also transfer the pre-video signal to board **50**. Once the pre-video signal has been digitally enhanced on supplementary board **60**, it is then sent to the video processor board **50** by means of another conductor **51**. The pre-video signal is an analog signal. The digitally enhanced pre-video signal may either be a digital signal or it may be converted back to the analog domain prior to being sent to board **50**.

In addition to digital enhancement, supplementary board **60** may further include other circuitry which may further condition the post-video signal so that it may be viewed in a desired format other than NTSC/PAL. As shown in FIGS. **4**, intermediate conductor **59** may transmit the signal output from Y chroma mixer **132** back to the supplementary board **60** where the signal is further encoded for viewing in a particular format. One common encoder which can be used includes an RGB encoder **154**. The RGB encoder separates the signal into three separate colors (red, green and blue) so that the surgeon may selectively choose to view only those images containing one or more of the colors. Particularly in tissue analysis where dyes are used to color the tissue, the RGB encoder may help the surgeon to identify targeted tissue.

The next encoder illustrated in FIG. **4** is a SVHS encoder **156** (super video home system). This encoder splits or separates the luminance portion of the signal and the chroma portion of the signal prior to entering the video device. Some observers believe that a cleaner signal is input to the video device by such a separation which in turn results in a more clear video image viewed on the video device. The last encoder illustrated in FIG. **4** is a VGA encoder **158** which enables the signal to be viewed on a standard VGA monitor which is common to many computer monitors.

One difference between the arrangement of image sensor **40** and the outputs found in FIG. 3 of the Fossum, et al. patent is that in lieu of providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry **92**. Accordingly, the pre-video signal only requires one conductor **48**.

FIGS. **5***a*–**5***e* illustrate in more detail one example of circuitry which may be used in the video processing board **50** in order to produce a post-video signal which may be directly accepted by a video device such as a television. The circuitry disclosed in FIGS. **5***a*–**5***e* is very similar to circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in FIGS. **5***a*–**5***e* are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in FIG. **5***a*, 5 volt power is provided along with a ground by conductors **44** and **46** to board **50**. The pre-video signal carried by conductor **48** is buffered at buffer **137** and then is transferred to amplifying group **138**. Amplifying group **138** amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control **140** shown in FIG. **5***b*. Automatic gain control **140** automatically controls the signal from amplifying group **138** to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control **140** conditions the signal based upon inputs from a 12 channel digital to analog converter **141**. Converter **141** retrieves stored information from EEPROM (electrically erasable programmable read only memory) **143**. EEPROM **143** is a non-volatile memory element which may store user information, for example, settings for color, tint, balance and the like. Thus, automatic gain control **140** changes the texture or visual characteristics based upon user inputs. The signal leaving the automatic gain control **140** is an analog signal until being converted by analog to digital converter **142**.

Digital signal processor **144** of FIG. **5***c* further processes the converted signal into a serial type digital signal. One function of the microprocessor **146** is to control the manner in which digital signal processor **144** sorts the digital signals emanating from converter **142**. Microprocessor **146** also controls analog to digital converter **142** in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor **146** may also control other functions of the imaging device such as white balance. The microprocessor **146** may selectively receive the information stored in the EEPROM **143** and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor **144**, the signal is sent to digital encoder **148** illustrated in FIG. **5***d*. Some of the more important functions of digital encoder **148** are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be placed in a condition for reception by a video device such as a television monitor. As also illustrated in FIG. **5***d*, once the signal has passed through digital encoder **148**, the signal is reconverted into an analog signal through digital to analog converter **150**.

This reconverted analog signal is then buffered at buffers **151** and then sent to amplifier group **152** of FIG. **5***e* which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in FIG. **5***e*, one SVHS outlet is provided at **160**, and two composite or NTSC outlets are provided at **162** and **164**, respectively.

In addition to the active pixel-type CMOS imager discussed above, certain advances in passive pixel-type CMOS imagers have been made such that the traditional noise associated with such passive arrangements can be overcome by improved manufacturing technologies which therefore does not require each signal to be amplified at each pixel site. Accordingly, FIG. **6** illustrates a simplified schematic diagram of a passive pixel which may be incorporated directly into the read out circuitry of Fossum, et al. (see FIG. **3**, U.S. Pat. No. 5,471,515; read out circuit or correlated double sampling circuit **70**). As shown in FIG. **6**, each passive pixel **160** in a passive pixel array comprises a photo diode **162** with a transistor **164** that passes the photoelectrically generated signal from photo diode **162** to a charge integration amplifier (not shown) outside the pixel array. After photo charge integration, the timing and control circuitry activates the access transistor **164**. The photoelectrically generated signal from photo diode **162** then transfers to the capacitance of the column bus **166** where the charge integration amplifier (not shown) at the end of the column bus **166** senses the resulting voltage. The column bus

voltage resets the photo diode **162**, and the timing and control circuitry then places the access transistor **164** in an off condition. The pixel **160** is then ready for another integration cycle. The signal output from either the active or passive pixel arrays are processed identically. Accordingly, FIG. **6** illustrates that the readout circuit **70** of Fossum, et al. is compatible with either the active or passive pixel arrays disclosed herein. One example of a manufacturer who has developed a passive pixel array with performance nearly equal to that of known active pixel devices and compatible with the read out circuitry of Fossum, et al. is VLSI Vision Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129.

FIGS. **7***a* and **7***b* illustrate yet another preferred embodiment of this invention. This embodiment also incorporates a generic endoscope, such as shown in FIGS **1***a* and **2***a*. Specifically, the generic endoscope **170** includes a handle **172** which may be grasped by the surgeon. The handle **172** has an interior opening **173** which allows wiring to pass through to the distal tip **177** of the endoscope. This interior opening **173**, as further discussed below, also houses the processing circuitry of the imaging device. The generic endoscope further includes a tubular portion **174** which is placed within the patient's body and which is defined by a flexible outer tube **178**. A battery channel **175** may also be incorporated within the handle **172** to receive a battery **176**. FIG. **7***b* shows the distal tip **177** of the endoscope in an enlarged fashion. A lens system **180** may be used to manipulate an image. Images are received upon a planar structure in the form of an image sensor **182** which includes an array of pixels and corresponding timing and control circuitry. This planar structure is the same as that illustrated in FIG. **4***a*. Image sensor **182** incorporating the pixel array and timing and control circuitry produces a pre-video signal (either analog or digital) which is transmitted by pre-video out conductor **188**. A 5-volt power source and a ground are provided to image sensor **182** by conductors **184** and **186**, respectively. A protective cable or sheathing **190** houses conductors **184**, **186** and **188** as they extend proximally back toward the handle **172** of the endoscope **170**. Additionally, a support tube **192** may fit over the protective cable **190** to provide further protection for the conductors. Referring back to FIG. **7***a*, desired processing circuitry can be placed directly within the handle of the endoscope since the processing circuitry is such a small size. In FIG. **7***a*, the processing circuitry incorporated within the handle **172** includes two planar structures, namely, a supplementary board **194** and a video processor board **196**. In terms of the construction of these boards, the boards **194** and **196** are the same as video processor board **50** and supplementary board **60**, respectively, of the first embodiment. Boards **194** and **196** may also be spaced apart from one another and placed in an aligned position as by pin connectors **195**. Pin connectors **195** are also of the same type as pin connectors **62** shown in FIG. **2***b*. The pre-video signal transmitted by conductor **188** is processed by the processing circuitry within the handle, and a post-video out signal is produced and transmitted by post-video out conductor **198**. Conductor **198** then connects directly to the desired video device (not shown) such as a video screen or personal computer. As shown in FIG. **7***a*, 5-volt power conductor **184**, ground conductor **186**, and post-video out conductor **198** may be housed within cable **199** which connects to the video device and a source of power (not shown). A fitting **200** may be used to stabilize cable **199** in its attachment to the handle **172**. As also shown in FIG. **7***a*, a light fiber bundle **202** may extend through the endoscope to provide light to the distal tip **177**. Accordingly, a cable **203** would extend back to a source of light (not shown), and fitting **204** would be used to stabilize the connection of cable **203** to the handle **172**. FIG. **7***a* further illustrates a power and ground conductor **206** which extends from the battery compartment/channel **175** in order to provide an alternate source of power to the endoscope. FIG. **7***a* has been simplified to better illustrate the differences between it and the previous embodiments. Accordingly, the light fibers and control wires which may extend to the distal end **177** are not illustrated (corresponding to light fibers **22** and control wires **24** of the first embodiment).

FIGS. **8***a* and **8***b* illustrate another endoscope which differs from FIGS. **7***a* and **7***b* by modifications made to the arrangement of the imaging device. FIG. **8***a* also does not illustrate the use of an alternate power source; however, it shall be understood, of course, that this Figure could also utilize a battery source of power as shown in FIG. **7***a*. More specifically, FIGS. **8***a* and **8***b* illustrate an imaging device wherein the array of pixels **208** and the timing and control circuitry **210** are on two separate planar structures placed back to back to one another in an aligned fashion. A multistrand conductor **212** transmits image signals produced by the pixel array **208**, and also carries the timing and control signals to the pixel array allowing the image signals to be read or unloaded at the desired speed, frequency, and sequence. Also FIG. **8***a* illustrates the use of video processor board **196**, and no supplementary board **194**. It shall be understood that, for both FIGS. **7***a* and **8***a*, the specific processing circuitry found within the interior opening **173** of the handle can include whatever type of processing circuitry as needed to create a post-video out signal which is readily acceptable by a video device without any further processing. Thus, FIG. **7***a* could be used without supplementary board **194**, and FIG. **8***a* could incorporate the use of supplementary board **194**. It shall also be understood that boards **194** and **196** have been greatly enlarged to better show their spatial arrangement and detail within interior opening **173**. Although it is possible that these boards may be of such illustrated size, as mentioned above with respect to the previous embodiment and boards **50** and **60**, these boards can be made small enough that the opening **173** within the endoscope has ample room to house the processing circuitry therein. In terms of the actual structure which is used to support the processing circuitry within the handle, the handle may be equipped with any suitable non-conductive support flanges or other extensions within the interior opening **173** which would allow the processing circuitry to be mounted thereon. Because of the extremely small size and insignificant weight of the processing circuitry, such supporting structure within interior opening **173** would be minimal.

As seen in FIG. **9**, the intensity or brightness of an image may be enhanced by a CMOS-CID imager which has a variable charge integration capability. The example at FIG. **9** shows a situation in which a viewed area may only reflect or emit an amount of light which is not normally capable of being seen by the human eye through a fluorescence microscope, endoscope, or may otherwise be very difficult to find. By adjusting the integration period, the image produced by the CMOS-CID imaging device intensifies the brightness or intensity of the image over the integration period to a much more readily observable amount of light. In the example of FIG. **9**, the brightness of a particular image is measured on the vertical axis, while the time in which the image is viewed or observed is measured on the horizontal axis. A threshold level of observable light or fluorescence is shown at horizontal line **304**, and which represents an average amount of light or fluorescence which can be observed by a currently available fluorescence microscope or endoscope without the aid of any special equipment. Any level of light or fluorescence falling below this threshold level **304** would be

considered very difficult to observe. Dashed line **306** represents the level of light or fluorescence which may be observed in viewing a particular area without the aid of an imager having variable charge integration capability. In accordance with the methods of this invention, an imager having charge integration capability could be used to enhance or brighten the observable light or fluorescence. The observed light or fluorescence using such an imager is depicted as line **308**. As shown, a three-second integration period has been chosen. During the first second of observation, there is no observable difference between viewing the area by use of a CCD type imager versus viewing the image with the aid of an imager having charge integration capability. However, between one and two seconds, the observed light or fluorescence **308** is now above the threshold level **304** which makes the area under investigation much more easy to locate and view. Between two and three seconds, the image is further brightened or enhanced due to the continuing charge integration period wherein charge continues to accumulate in the pixels of the imager. The stepped pattern of observed light or fluorescence **308** is due to the monitor update cycle or period. Thus, between one and two seconds, a first update of the monitor period occurs which reflects the increased charge accumulating in the pixels of the imager. Charge accumulates in the pixels in a linear fashion. Therefore, the monitor update period could be reduced to show a more linear increase of brightness of observed fluorescence. In some cases, it may be desirable to have more of a stepped visual image, as shown in FIG. **9**. When the charge integration period ends, the accumulated charge is then released or dumped from the pixels, and a new charge integration period begins. Thus, the example of FIG. **9** shows the brightness of an image being repeated in a similar pattern between three and six seconds. It can be seen that the capability to view observed light or fluorescence is greatly enhanced by use of an imager having variable charge integration capability which may overcome low light conditions or low fluorescence of a particular bodily tissue.

FIG. **10** is a schematic diagram of an imager and its processing circuitry which incorporate variable charge integration capability. Imager **40** is coupled to its video processing circuitry **50**. Power supply **52** supplies power to the imaging device and the additional circuitry to achieve charge integration. In order to incorporate variable charge integration capability, imager readout clock select circuitry **318** is added which communicates with one or more of the video processor boards **50**. An imager integration time select switch **320** is provided enabling an operator to manually select the desired integration period. As shown, the integration periods may be periods of less than one second, or more than one second. FIG. **10** illustrates a situation in which an operator has chosen a three-second integration period. As the area is observed by the imager **40**, the imager will accumulate charge based upon the selected integration period. The image is viewed on the display monitor **316**. As also discussed above, the monitor update period can also be adjusted to provide more or less of a stepped brightness image. The operator would then adjust the charge integration period to obtain the most desirable image of the area being viewed.

It should be understood that the imager **40** may be used in conjunction with the optics of a fluorescence microscope. Many fluorescence microscopes today also have miniature cameras which are used to record images observed by the fluorescence microscope. Thus, the imager **40** could replace the miniature camera or imager used on commercially available fluorescence microscopes. Also, it shall be understood that an endoscope which may be used in fluorescence guided endoscopy may also incorporate variable charge integration capability in order to enhance the ability to find and evaluate fluorescing cells. Thus, the use of variable charge integration capability has multiple benefits not only in viewing cells which have been removed from a body, but also to view cells in the body which may undergo some treatment or surgical procedure, and are to be located by fluorescence guided endoscopy.

Fluorescence-assisted surgery and fluorescence-assisted endoscopy can also be enhanced by providing an endoscope utilizing a CMOS-CID imager which has variable charge integration capability. The ability of a surgeon to view a cancerous growth inside the patient can be enhanced by choosing an integration period which greatly expands the imaging sensitivity of the endoscope. The faint or slight amount of fluorescence which might not be observable through a CCD imager can be enhanced by using a CMOS-CID imager modified with variable charge integration capability, resulting in readily observable fluorescence. Thus, in every conceivable aspect of endoscopy and cancer screening, use of an endoscope having a variable charge integration capability is advantageous for finding a cancerous growth.

One example of fluorescence guided endoscopy might be fluorescence endoscopy to find colon cancer. Once the patient has been administered 5-ALA or another similar compound, the surgeon would conduct the endoscopic procedure looking for fluorescing colon tissue. As the surgeon conducts the endoscopic procedure, the charge integration periods could be adjusted to maximize observable fluorescence. In some cases, it may be very difficult for the surgeon to find all fluorescing tissues within the colon. By using the variable charge integration capability incorporated within the endoscope, the surgeon is more capable of finding each and every fluorescing groups of tissue within the colon to make a proper diagnosis. Also, light delivery to the surgical site can be chosen from a desired frequency of light corresponding to the excitation frequency of the compound administered to the patient.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of an endoscope, or may have some elements of the imaging device being placed in a small remote box adjacent to the endoscope. Based upon the type of image sensor used, the profile area of the imaging device may be made small enough to be placed into an endoscope which has a very small diameter tube. Additionally, the imaging device may be placed into the channels of existing endoscopes to provide additional imaging capability without increasing the size of the endoscope. The imaging device may be powered by a standard power input connection in the form of a power cord, or a small lithium battery may be used.

The imaging device of the invention can be further enhanced by incorporating a charge integration feature which enhances the ability of a user to selectively adjust the brightness of an image. As discussed above, fluorescence detection in patient screening and treatment for a wide array of photo-dynamic treatments can be greatly improved by utilizing the imaging device of the invention having charge integration capability.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

What is claimed is:

1. A reduced area imaging device comprising:

an image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a first circuit board lying in a second plane and communicating with said image sensor by at least one pre-video conductor inner-connecting said image sensor and said first circuit board, said first circuit board including circuitry means for converting said pre-video signal to a post-video signal for reception by a standard video device;

a power supply coupled with said image sensor for driving said array of pixels and said timing and control means, and electrically coupled to said first circuit board for driving said first circuit board; and

a time select switch electrically communicating with said first circuit board and remote from said first circuit board for selectively varying integration periods to produce an image of a desired brightness, said switch having a plurality of settings enabling selective control to produce the image of a desired brightness.

2. A device, as claimed in claim **1**, wherein:

said array of pixels includes an array of CMOS pixels.

3. A device, as claimed in claim **1**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for enhancing said pre-video signal prior to reception by said first circuit board.

4. A reduced area imaging device comprising:

an image sensor lying in a first plane and including an array of pixels for receiving images thereon, said image sensor including circuitry means on said first plane and coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a control box remote from the said image sensor, said control box including circuitry means for receiving said pre-video signal from said image sensor, and for converting said pre-video signal to a post-video signal which may be received by a standard video device;

a power supply coupled to said control box and said image sensor for providing power thereto; and

a time select switch electrically communicating with said circuitry means and remote from said first circuit board for receiving and for converting, said time select switch for selectively varying integration periods to produce an image of a desired brightness, said switch having a plurality of settings enabling selective control to produce the image of a desired brightness.

5. A device, as claimed in claim **1**, wherein:

said array of pixels includes an array of CMOS pixels.

6. A device, as claimed in claim **1**, further including:

a second circuit board electrically coupled with said circuitry means for receiving and for converting said pre-video signal, said second circuit board for enhancing said pre-video signal prior to reception by said circuitry means for receiving and converting.

7. A reduced area imaging device comprising:

an image sensor lying in a first plane and including an array of pixels for receiving images thereon;

a first circuit board spaced from said image sensor and electrically communicating therewith, said first circuit board including circuitry means for timing and control of said array of CMOS pixels, said image sensor and said timing and control circuitry producing a pre-video signal said first circuit board further including circuitry means for converting said pre-video signal, to a post-video signal for reception by a standard video device;

a power supply electrically coupled with said image sensor and said first circuit board for providing power thereto; and

a time select switch electrically communicating with said first circuit board and remote from said first circuit board for selectively varying integration periods to produce an image of a desired brightness, said switch having a plurality of settings enabling selective control to produce the image of a desired brightness.

8. A device, as claimed in claim **7**, wherein:

said array of pixels includes an array of CMOS pixels.

9. A device, as claimed in claim **7**, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for enhancing said pre-video signal.

10. A reduced area imaging device comprising:

an image sensor lying in a first plane and including an array of pixels for receiving images thereon;

circuitry means electrically coupled to said array of pixels for timing and control of said array of pixels, said image sensor producing a pre-video signal;

a control box remote from said image sensor and said timing control means, said control box including circuitry means for receiving said pre-video signal from said image sensor and for converting said pre-video signal to a post-video signal which may be received by a standard video device;

a power supply coupled to said control box and said image sensor for providing thereto; and

a time select switch electrically communicating with said circuitry means for receiving and for converting, said time select switch for selectively varying integration periods to produce an image of a desired brightness, said switch being remote from said first circuit board and having a plurality of settings enabling selective control to produce the image of a desired brightness.

11. A device, as claimed in claim **10**, wherein:

said array of pixels includes an array of CMOS pixels.

12. A device, as claimed in claim **10**, further including:

a second circuit board electrically coupled with said circuitry means for receiving and converting, said second circuit board for enhancing said pre-video signal.

13. A method of viewing an object with an imaging device, said method comprising the steps of:

providing an image sensor including an array of pixels, circuitry means coupled to said array of pixels for timing and control of said pixels, said image sensor producing a pre-video signal;

providing first circuitry means for receiving said pre-video signal from said image sensor and for converting said pre-video signal to a post-video signal which may be received by a standard video device;

viewing the object and determining a desired level of brightness to be viewed;

providing a time select switch remote from the image sensor and circuitry means; and

adjusting a charge integration period of the imager by manipulating time select switch to maximize desired brightness of the image.

14. A method, as claimed in claim **13**, wherein:

said array of pixels includes an array of CMOS pixels.

15. A method, as claimed in claim **13**, further including the step of:

providing second circuitry means coupled to said first circuitry means for enhancing said pre-video signal.

* * * * *

CERTIFICATE OF COMPLIANCE WITH RULE 32(B)

1. This brief complies with the type-volume limitation of Fed. Cir. R. 32(b) because this brief contains 6,891 words, exclusive of the certificate of interest, table of contents, table of citations, statement of related cases, addendum and this certificate of compliance as exempted by Fed. R. App. P. 32(f) and Fed. Cir. R. 32(b).

2. This brief complies with the typeface requirements of Fed. R. App. P. 32(a)(5) and the type style requirements of Fed. R. App. P. 32(a)(6) because this brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14 point font.

Respectfully submitted,

Dated: May 2, 2022

/s/ Paul J. Andre
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