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Paper No. 76
Filed: April 30, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2018-01604
Patent 7,421,524 B2

Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and CHRISTA P. ZADO, *Administrative Patent Judges.*

DESHPANDE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Microsoft Corporation ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1, 2, and 13–15 of U.S. Patent No. 7,421,524 B2 (Ex. 1001, "the '524 patent"). Paper 2 ("Pet."). FG SRC LLC ("Patent Owner") filed a Preliminary Response pursuant to 35 U.S.C. § 313. Paper 15 ("Prelim. Resp.").[1]

On May 3, 2019, we issued a Decision ordering that "an *inter partes* review is hereby instituted with respect to all grounds set forth in the Petition." Paper 21 ("Dec."), 29. After institution, Patent Owner filed a Patent Owner's Response (Paper 38, "PO Resp."). In reply, Petitioner filed a Petitioner's Reply to Patent Owner's Response (Paper 56, "Pet. Reply"). In response, Patent Owner filed a Patent Owner's Sur-Reply (Paper 62, "PO Sur-Reply"). Petitioner and Patent Owner also filed Motions to Exclude Evidence (Papers 63 ("Pet. Mot."), 64 ("PO Mot.")), Oppositions to the Motions (Papers 65 ("Pet. Opp. Mot."), 66) and Replies to the Oppositions (Papers 68, 69). Petitioner and Patent Owner presented oral arguments on February 3, 2020, and a transcript has been entered into the record. Paper 75 ("Tr.").

The Board has jurisdiction under 35 U.S.C. § 6. In this Final Written Decision, after reviewing all relevant evidence and arguments, we determine that Petitioner has met its burden of showing, by a preponderance of the

[1] Saint Regis Mohawk Tribe, originally named as Patent Owner, assigned the '524 patent to DirectStream, LLC on May 21, 2019. Paper 27, 1. DirectStream, LLC assigned the '524 patent to FG SRC LLC on January 22, 2020. Paper 73, 1.

evidence, that claims 1, 2, and 13–15 of the '524 patent are unpatentable. Petitioner's Motion to Exclude is *denied-in-part* and *dismissed-in-part*. Patent Owner's Motion to Exclude is *denied-in-part* and *dismissed-in-part.*

B. Related Proceedings

The parties indicate that the '524 patent currently is involved in *SRC Labs, LLC et al. v. Microsoft Corp.*, Civil Action No. 2-18-cv-00321 (W.D. Wash.), which was transferred from *SRC Labs, LLC et al. v. Microsoft Corp.*, Civil Action No. 1-17-cv-01172 (E.D. Va.). Pet. 3; Prelim. Resp. 4–5. The following proceedings, before the Board, also involve the same parties: IPR2018-01594, IPR2018-01599, IPR2018-01600, IPR2018-01601, IPR2018-01602, IPR2018-01603, IPR2018-01605, IPR2018-01606, and IPR2018-01607.[2]

C. The '524 Patent (Ex. 1001)

The '524 patent is directed to the field of computer architecture, and, specifically, "a switch/network adapter port ('SNAP') for clustered computers employing a chain of multi-adaptive processors ('MAP[]') . . . in a dual in-line memory module ('DIMM') format." Ex. 1001, 1:29–37.

A block diagram of an exemplary MAP element is disclosed in Figure 3:

[2] IPR2018-01602 and IPR2018-01603 have been consolidated with IPR2018-01601. IPR2018-01606 and IPR2018-01607 have been consolidated with IPR2018-01605.

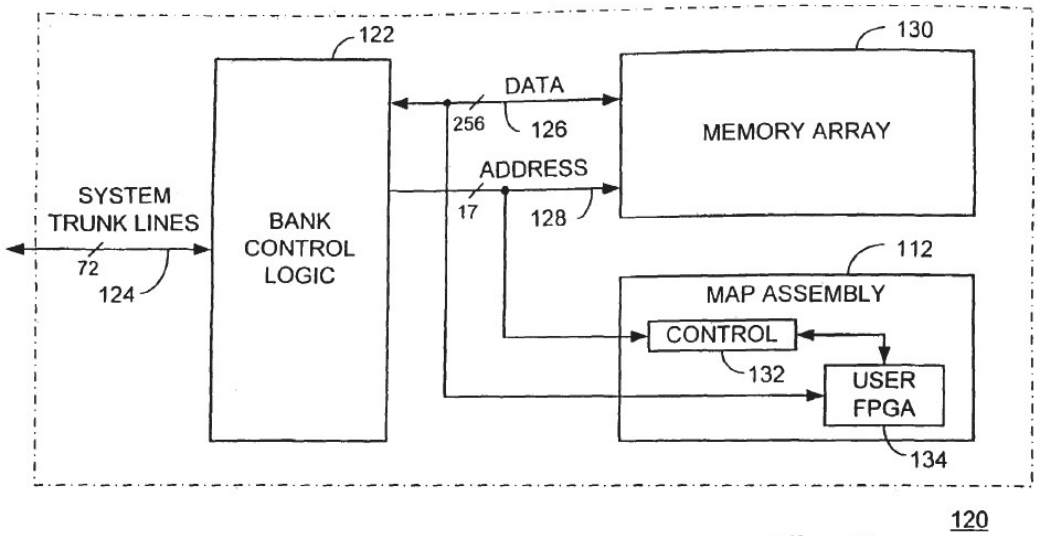

Fig. 3

Figure 3 illustrates memory bank 120 for a MAP element-based system computer architecture (not depicted in Figure 3). *Id.* at 4:60–64. "Each memory bank 120 includes a bank control logic block 122 bi-directionally coupled to the computer system trunk lines, for example, a 72 line bus 124." *Id.* at 4:64–66. Memory array 130 is coupled to bank control logic 122 via bi-directional data bus 126 and address bus 128. *Id.* at 4:67–5:3. "MAP element 112 comprises a control block 132 coupled to the address bus 128." *Id.* at 5:5–6. "[C]ontrol block 132 is also bi-directionally coupled to a user field programmable gate array ('FPGA')," and "user FPGA 134 is coupled directly to the data bus 126." *Id.* at 5:6–10. The '524 patent discloses that MAP element 112 has direct memory access (DMA) capability, which permits it to write to memory, and "it is possible to allow a MAP element 112 to feed results to another MAP element 112 through use of a chain port" because MAP element 112 receives operands via writes to memory. *Id.* at 5:50–54.

Computer system 200 including MAP element 212 in DIMM format is depicted in Figure 5:

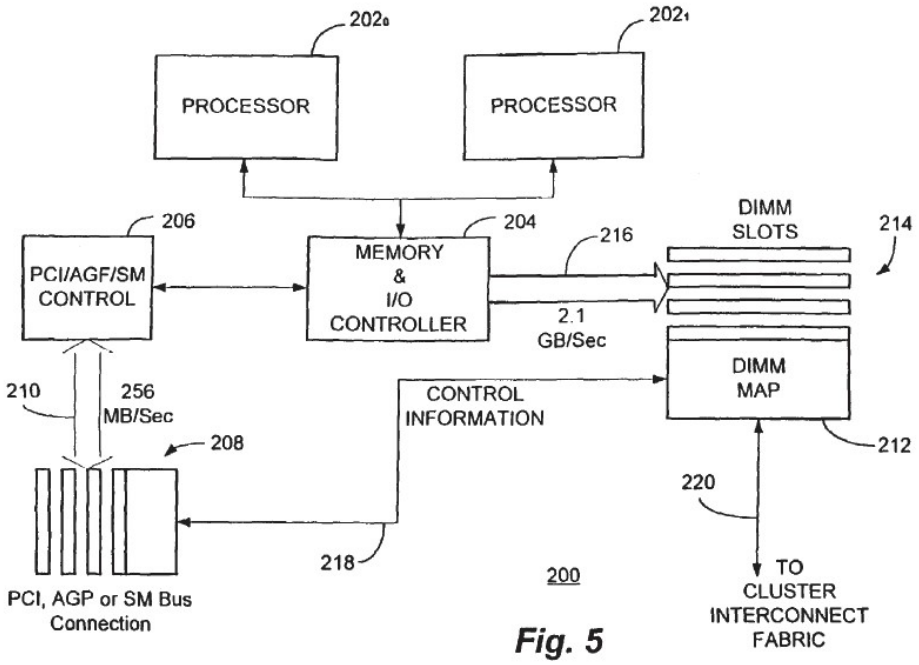

Fig. 5

Figure 5 illustrates "computer system 200 includ[ing] one or more processors 202_0 and 202_1 which are coupled to an associated PC memory and I/O controller 204." *Id.* at 7:42–45. "[C]ontroller 204 is . . . conventionally coupled to a number of DIMM slots 214 by means of a much higher bandwidth DIMM bus 216 capable of data transfer rates of 2.1 GB/sec. or greater." *Id.* at 7:56–59. DIMM MAP element 212 is associated with, or physically located within, one of DIMM slots 214, which may be coupled to another clustered computer MAP element by a cluster interconnect fabric connection 220 that is connected to MAP chain ports. *Id.* at 7:59–62, 7:65–8:1.

The '524 patent discloses that because DIMM MAP element 212 is placed in one of DIMM slots 214, FPGA 134 of DIMM MAP element 212 accepts normal memory "read" and "write" transactions, and converts them to a format used by an interconnect switch or network. *Id.* at 8:13–17. According to the '524 patent, however, "the electrical protocol of the

DIMMs is such that once the data arrives at the receiver, there is no way for a DIMM module within the DIMM slots 214 to signal the microprocessor 202 that it has arrived." *Id.* at 8:29–33. The "efforts of the processor 202 would have to be synchronized through the use of a continued polling of the DIMM MAP elements 212 to determine if data has arrived." *Id.* at 8:29–36. According to the '524 patent, this would consume the processor and much of its bandwidth, thereby stalling all other bus agents. *Id.* at 8:36–38.

To address this issue, the '524 patent discloses connection 218 interconnecting DIMM MAP element 212 and PCI bus 210 such that DIMM MAP element 212 may generate communications packets and send them via PCI bus 210 to processor 202. *Id.* at 7:62–65; 8:39–43. According to the '524 patent, because these packets would account for a very small percentage of the data moved, low bandwidth effects of PCI bus 210 would be minimized. *Id.* at 8:43–47.

D. Illustrative Claim

Petitioner challenges claims 1, 2, and 13–15 of the '524 patent. Pet. 12–80. Claim 1 is the only independent claim at issue. Claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A processor element for a memory module bus of a computer system, said processor element comprising:
>
> a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided directly thereto on said memory module bus; and
>
> a direct data connection coupled to said field programmable gate array for providing said altered data directly from said memory module bus to an external device coupled thereto.

Ex. 1001, 9:42–10:4.

E. The Alleged Grounds of Unpatentability

The information presented in the Petition sets forth grounds of unpatentability of claims 1, 2, and 13–15 of the '524 patent as follows (*see* Pet. 12–80):[3,4]

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 13–15	§ 102	Tsutsui[5]
1, 2, 13–15	§ 103	Tsutsui
1, 2, 13–15	§ 103	Tsutsui, Tsutsui II[6]
2	§ 103	Tsutsui, Stone,[7] with or without Tsutsui II
14	§ 103	Tsutsui, Collins,[8] with or without Tsutsui II
15	§ 103	Tsutsui, Hayashi,[9] with or without Tsutsui II

[3] Petitioner supports its challenge with the Declaration of Scott Hauck, Ph.D. Ex. 1003.

[4] All references to 35 U.S.C. §§ 102, 103 herein are pre-AIA.

[5] Akihiro Tsutsui et al., *YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing*, Proceedings of Association for Computing Machinery / Special Interest Group for Design Automation (ACM/SIGDA) FPGA '97, 93–99, (1997) (Ex. 1007, "Tsutsui").

[6] A. Tsutsui et al., *Special Purpose FPGA for High-speed Digital Telecommunications Systems*, 1995 IEEE International Conference on Computer Design: VLSI in Computers & Processors, pp. 486–491 (1995) (Ex. 1009, "Tsutsui II").

[7] Harold S. Stone, MICROCOMPUTER INTERFACING 1–41 (Tom Robbins et al. 2d ed. 1983) (Ex. 1010, "Stone").

II. ANALYSIS

A. Motions to Exclude

The party moving to exclude evidence bears the burden of proof to establish that it is entitled to the relief requested—namely, that the material sought to be excluded is inadmissible under the Federal Rules of Evidence. *See* 37 C.F.R. §§ 42.20(c), 42.62(a). For the reasons discussed below, Petitioner's Motion is *denied-in-part* and *dismissed-in-part*, and Patent Owner's Motion is *denied-in-part* and *dismissed-in-part*.

1. Petitioner's Motion to Exclude

a. Exhibits 2067 and 2086

Petitioner moves to exclude the declaration of one of the named inventors of the '524 patent, Jon Huppenthal (Exhibit 2067), "in its entirety as not being relevant to any issue on which trial has been instituted, and for lacking foundation, containing hearsay, and/or causing undue prejudice." Pet. Mot. 3–6. Petitioner additionally moves to exclude portions of "Mr. Huppenthal's declaration (Ex. 2067 ¶¶ 80, 82–86) due to his refusal to answer questions concerning those portions of the declaration." *Id*. at 1–3 (citing Paper 51, 7–8).

Petitioner also moves to exclude a transcript (Exhibit 2086) of a deposition of Petitioner's declarant from other *inter partes* reviews as "not being relevant to any issue on which trial has been instituted, for containing

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[8] U.S. Patent No. 5,671,355, issued September 23, 1997 (Ex. 1008, "Collins").

[9] K. Hayashi et al., *Reconfigurable Real-Time Signal Transport System using Custom FPGAs*, IEEE Symposium on FPGAs for Custom Computing Machines, IEEE (1995) (Ex. 1013, "Hayashi").

hearsay, and/or causing undue prejudice." *Id.* at 6–7. Petitioner argues that allowing the transcript in the record would be "highly prejudicial as it presents itself with the indicia of expert testimony while being totally devoid from the necessary context of the matter from which it originates." *Id.* at 6. Patent Owner cites Exhibits 2067 and 2086 in its Response and Sur-Reply.

Petitioner's Motion is dismissed as moot, as we do not rely on the testimony in a manner adverse to Petitioner in this Decision. As explained below, even if the testimony is considered, we are not persuaded by Patent Owner's arguments regarding the state of the art or alleged nonobviousness of the challenged claims, and Patent Owner has not shown proof of secondary considerations that would support a conclusion of nonobviousness. *See supra* Sections II.C–II.D.

b. Exhibit 2102

Petitioner moves to exclude paragraph 133 of the declaration of Patent Owner's declarant, Houman Homayoun, Ph.D., which refers to Exhibit 2067. Pet. Mot. 8. Because we do not exclude that exhibit, and do not rely on paragraph 133 of the Homayoun Declaration, we also dismiss as moot Petitioner's Motion with respect to Exhibit 2102.

c. Exhibits 2060, 2062–2064, 2066, 2072-2080, 2085, 2088, 2092, 2094, 2096–2101, 2103, 2104, 2106–2145, 2147, 2148, 2157, and 2160

Petitioner moves to exclude a number of exhibits as "not being relevant to any issues on which trial has been instituted, lacking foundation, and/or causing undue prejudice" because the exhibits were not discussed substantively and/or cited in Patent Owner's Response and Sur-Reply. Pet. Mot. 7–8. Petitioner's Motion is dismissed as moot, as we do not rely on the exhibits in a manner adverse to Petitioner in this Decision. We note,

however, that in evaluating Petitioner's asserted grounds of unpatentability, we only consider substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document that can be considered.

d. Patent Owner's Response

Petitioner moves to exclude portions of Patent Owner's Response referring to the exhibits that Petitioner seeks to exclude. Pet. Mot. 8. Patent Owner's Response is a paper with attorney arguments, not evidence that may be excluded.[10] Further, we do not exclude any of the exhibits referred to in the identified portions of the Response. Petitioner's Motion is denied as to Patent Owner's Response.

2. Patent Owner's Motion to Exclude

a. Exhibits 1007, 1036 and 1038

Patent Owner first objected to the authenticity of Exhibit 1007 in its Patent Owner Response. PO Mot. 5 (citing PO Resp. 48). Now, Patent Owner moves to exclude Exhibits 1007, 1036, and 1038 as unauthenticated under Federal Rule of Evidence 901 because Petitioner's declarant, Stephen Trimberger, Ph.D., "admits that his original declaration did not properly authenticate EX1007." PO Mot. 5–7 (citing Ex. 1034 ¶ 7). Patent Owner argues that Petitioner attempts to authenticate Exhibit 1007 using evidence submitted for the first time in Petitioner's Reply, which violates Patent

[10] Petitioner did not seek authorization to file a motion to strike Patent Owner's Response. *See* Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019), 80–81, *available at* https://www.uspto.gov/TrialPracticeGuideConsolidated ("Trial Practice Guide").

Owner's due process and administrative rights. *Id.* at 6. Patent Owner further argues that Exhibits 1036 and 1038, which are identical copies of Exhibit 1007, should be excluded "for the same reasons" as Exhibit 1007. *Id.* at 5, 7.

"Any objection to evidence submitted during a preliminary proceeding must be filed within ten business days of the institution of the trial. . . . The objection must identify the grounds for the objection with sufficient particularity to allow correction in the form of supplemental evidence." 37 C.F.R. § 42.64(b)(1); *see* 37 C.F.R. § 42.2 (defining a "preliminary proceeding" as the time period beginning "with the filing of a petition for instituting a trial" and ending "with a written decision as to whether a trial will be instituted"). This process allows the party that originally submitted the evidence to attempt to cure the objection by serving supplemental evidence. 37 C.F.R. § 42.64(b)(2). If the submitting party does not serve supplemental evidence, or if the supplemental evidence does not cure the objection, "[a] motion to exclude evidence must be filed to preserve [the] objection. The motion must identify the objections in the record in order and must explain the objections." 37 C.F.R. § 42.64(c).

"To satisfy the requirement of authenticating or identifying an item of evidence, the proponent must produce evidence sufficient to support a finding that the item is what the proponent claims it is." Fed. R. Evid. 901(a). Certain evidence, though, is "self-authenticating" and "require[s] no extrinsic evidence of authenticity in order to be admitted." Fed. R. Evid. 902.

Petitioner asserts that Patent Owner waived its objection by failing to timely object to Exhibit 1007 as lacking authenticity. Pet. Opp. Mot. 1. We

agree. Patent Owner admits that it objected to the authenticity of Exhibit 1007 in its Response. PO Mot. 5. Patent Owner submitted its Response on August 5, 2019, more than ten business days after we instituted this proceeding on May 3, 2019. Therefore, Patent Owner's objection to Exhibit 1007 based on authenticity is untimely.

Petitioner further asserts that Exhibits 1007, 1036, and 1038 are authentic. Pet. Opp. Mot. 1–4. First, Petitioner asserts Exhibit 1007 is authentic under Federal Rule of Evidence 901(a) because the record evidence unambiguously shows that Exhibit 1007 is a copy of the Tsutsui reference. *Id.* at 2. Second, Petitioner asserts that Exhibits 1036 and 1038 are self-authenticating as ancient documents under Federal Rule of Evidence 901(b)(8) because each is "in a condition that creates no suspicion about its authenticity," "was in a place where, if authentic, it would likely be," and "is at least 20 years old when offered." *Id.* at 2–3. Because Exhibits 1036 and 1038 are self-authenticating, and Exhibits 1007, 1036, and 1038 are identical, then Exhibit 1007 is also self-authenticating according to Petitioner. *Id.* Third, Petitioner argues that Exhibits 1007, 1036, and 1038 are Association for Computing Machinery (ACM) publications that each include "an ACM trade inscription, copyright symbol, and [International Standard Book Number (ISBN)]," and therefore, these documents self-authenticate under Federal Rules of Evidence 902(6) and 902(7). *Id.* at 3–4. Finally, Petitioner asserts that Exhibits 1007, 1036, and 1038 are also authenticated under Federal Rule of Evidence 901(b)(4) based on the totality of the circumstances and because Patent Owner does not identify anything to suggest the exhibits are not authentic. *Id.* at 4.

We agree with Petitioner that Exhibits 1007, 1036, and 1038 are self-authenticating under Federal Rules of Evidence 902(6) and 902(7), and that Exhibits 1036 and 1038 are ancient documents under Federal Rule of Evidence 901(b)(8) for the reasons stated by Petitioner. Exhibits 1007, 1036, and 1038 include an ACM trade inscription, copyright symbol, and ISBN number. Exhibits 1036 and 1038 are authentic as ancient documents, as they meet the requirements of Federal Rule of Evidence 901(b)(8).

Accordingly, we deny Patent Owner's Motion to Exclude Exhibits 1007, 1036, and 1038.

b. Exhibits 1034, 1035, and 1039

Patent Owner moves to exclude certain portions of Exhibits 1034, 1035, and 1039 because many portions of the reply declarations allegedly "are not based on the personal knowledge of the witness, are impermissible hearsay, and/or are impermissible expert opinions from a witness unqualified to provide such opinions." PO Mot. 7–8. We are not persuaded. Patent Owner does not identify any particular "statement" in any of the exhibits that is being offered "to prove the truth of the matter asserted in the statement," and thus fails to meet its burden to prove inadmissibility as hearsay. *See* Fed. R. Evid. 801(c); 37 C.F.R. § 42.20(c). Petitioner further establishes that the declarations were each based on the declarant's personal knowledge and qualifications. Pet. Opp. Mot. 5–7 (citing Ex. 1034 ¶¶ 2, 4, 9, 16, 30; Ex. 1035 ¶¶ 7–8, 17 (citing Ex. 1039 ¶¶ 2, 5–6)); *see* Ex. 1034 ¶ 2 ("I am submitting this declaration based on my own personal knowledge of the facts stated here . . . ."). Accordingly, we deny Patent Owner's Motion to Exclude Exhibits 1034, 1035, and 1039.

c. Exhibit 1032

Patent Owner moves to exclude Exhibit 1032 because it is "irrelevant to this case" and because Petitioner "failed to properly authenticate" Exhibit 1032. PO Mot. 8–9. Patent Owner also asserts that, to the extent Petitioner attempts to meet its burden of proof using Exhibit 1032, Petitioner's use of the document is impermissible hearsay. *Id.* at 9. Petitioner argues that Exhibit 1032 is the specific copy of the Tsutsui reference that Dr. Hauck relied on for purposes of his declaration, and was not initially filed with the Petition (but was filed with the Reply). Pet. Opp. Mot. 7–8. Petitioner also asserts that "extensive testimony entered into the record by Dr. Trimberger" authenticates Exhibit 1032. *Id.* at 8.

We agree with Petitioner that Patent Owner has not set forth sufficient argument and evidence to exclude Exhibit 1032 as irrelevant. We are also persuaded that Dr. Trimberger's testimony authenticates Exhibit 1032. *See, e.g.*, Ex. 1034 ¶¶ 7 ("I understand that the version of the *Tsut[su]i* paper which I refer to as Exhibit 1007 (included here as EX1032 and referred to as *Tsutsui-1032*) was not included with my original declaration, and a different version of the same paper was included in its place."), 5 ("*Tsutsui-1007* and *Tsutsui-1032* are substantively identical."). Accordingly, Patent Owner's Motion to Exclude Exhibit 1032 is denied.[11]

d. Exhibits 1033, 1036, 1038, 1040, 1041, 1043–1050, 1053–1057

Patent Owner moves to exclude Exhibits 1040, 1041, 1043, and 1045–1049 because none of these exhibits "are cited, discussed, or relied upon by

[11] To be clear, Petitioner's asserted grounds of unpatentability are based on the version of Tsutsui filed as Exhibit 1007, not Exhibit 1032. *See* Dec. 7–8, 29; Pet. 4; Pet. Opp. Mot. 8.

any expert witness or fact witness in this case." PO Mot. 9. Patent Owner also moves to exclude Exhibits 1033, 1036, 1038, 1044, 1050, and 1053–1057 because they are "not cited in any of Petitioner's papers." *Id.* at 12. We see no basis to exclude the exhibits for that reason and dismiss Patent Owner's request, but again note that in evaluating Petitioner's asserted grounds of unpatentability, we only consider substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document that can be considered.

Patent Owner further moves to exclude Exhibits 1040, 1043, and 1049 as unauthenticated under Federal Rule of Evidence 901. *Id.* at 10–11. Petitioner argues that "Patent Owner identifies nothing about the documents themselves that brings into question their authenticity," and "Patent Owner bears the burden as movant to demonstrate these documents are not authentic." Pet. Opp. Mot. 10. Petitioner further asserts that Exhibits 1040 and 1049 are IEEE publications that each include "a trade inscription, copyright symbol, and ISBN," and, therefore, these documents self-authenticate under Federal Rules of Evidence 902(6) and 902(7). *Id.* at 10–11. Petitioner further argues that Exhibits 1040, 1043, and 1049 are authenticated under Federal Rule of Evidence 901(b)(4) "based on the totality of the circumstances based on their appearance alone, as nothing about those exhibits suggests that [they] are not what the[y] purport to be, and Patent Owner never identifies anything to suggest otherwise." *Id.* at 11. Petitioner also argues that Exhibit 1040 is an ancient document because it is over twenty years old and meet the requirements of Federal Rule of

Evidence 901(b)(8). *Id.* at 11. We agree with Petitioner that Patent Owner has not set forth sufficient argument and evidence to exclude Exhibits 1040, 1043, and 1049 as unauthenticated, and we further agree that Exhibit 1040 is self-authenticating and an ancient document for the reasons stated by Petitioner.

Patent Owner further moves to exclude Exhibits 1040, 1041, 1043, and 1045–1049 as containing inadmissible hearsay under Federal Rule of Evidence 802. PO Mot. 10–11. Patent Owner states that Petitioner in its Reply "cites each of these documents to prove the truth of technical matters allegedly asserted in such documents, *i.e.* to support Petitioner's specific factual assertions regarding a technical issue." *Id.* at 10. We are not persuaded. Patent Owner does not identify any particular "statement" in any of the exhibits that is being offered "to prove the truth of the matter asserted in the statement," and thus fails to meet its burden to prove inadmissibility as hearsay. *See* Fed. R. Evid. 801(c); 37 C.F.R. § 42.20(c). Even if Patent Owner had done so, Petitioner cites the exhibits to show what a person of ordinary skill in the art would have known at the time of the '524 patent about the technical features and developments in the pertinent art. Pet. Opp. Mot. 12 (citing Ex. 1040 and 1041). The exhibits are not being offered for the truth of any particular matter discussed in the references. Accordingly, we deny Patent Owner's Motion to Exclude Exhibits 1040, 1041, 1043, and 1045–1049.

Patent Owner appears to move to exclude uncited portions of deposition testimony from Mr. Huppenthal and Dr. Homayoun (Exhibits 1033 and 1055–1057) because "Petitioner has failed to establish [their] relevance to this case." PO Mot. 13. We see no basis to exclude the exhibits

for that reason and dismiss Patent Owner's request, but again note that in evaluating Petitioner's asserted grounds of unpatentability, we only consider substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document that can be considered.

e. Exhibits 1051 and 1052

Patent Owner moves to exclude certain portions of the transcripts of two depositions of Steven A. Guccione, Ph.D., because the questions asked were "vague and ambiguous." PO Mot. 11–12 (citing Ex. 1052, 51:1–7; Ex. 1051, 38:14–39:6). Patent Owner's Motion is dismissed as moot, as we do not rely on the disputed portions of the testimony in rendering our Decision.

Additionally, Patent Owner appears to move to exclude uncited portions of deposition testimony from Dr. Guccione because "Petitioner has failed to establish [their] relevance to this case." *Id.* at 13. We see no basis to exclude the exhibits for that reason and dismiss Patent Owner's request, but again note that in evaluating Petitioner's asserted grounds of unpatentability, we only consider substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document that can be considered. Accordingly, Patent Owner's Motion with respect to uncited portions of Dr. Guccione's testimony is dismissed.

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art for a challenged patent, we look to "1) the types of problems encountered in the art; 2) the prior art solutions to those problems; 3) the rapidity with which innovations are made; 4) the sophistication of the technology; and 5) the educational level of active workers in the field." *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 666–667 (Fed. Cir. 2000); *see also Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–963 (Fed. Cir. 1986). "Not all such factors may be present in every case, and one or more of them may predominate." *Ruiz*, 234 F.3d at 666–667; *see also Custom Accessories*, 807 F.2d at 963.

Petitioner asserts that a person of ordinary skill in the art, at the time of the '524 patent, would have had "a Bachelor's degree in Electrical Engineering, Computer Engineering, Computer Science, or in a related field, and four years of experience with the design or use of field programmable gate array based systems or network adapters." Pet. 5 (citing Ex. 1003 ¶ 41). Petitioner alternatively argues that a person of ordinary skill in the art "would have had an advanced degree in one of those fields and two years of related experience." *Id.* Moreover, such a person, according to Petitioner, would have been knowledgeable about computer architectures and how FPGAs could be included in them. *Id.* at 5. Such a person also would have been knowledgeable about software algorithms that could be implemented on FPGAs and how to configure FPGAs to carry out such implementation. *Id.* (citing Ex. 1003 ¶ 41).

Patent Owner disputes Petitioner's assessment of the level of ordinary skill in the art, but does not provide a proposed level of ordinary skill in the

art that we should apply in this proceeding.[12] PO Resp. 30–33. Patent Owner contends Petitioner's assessment is incorrect because a person of ordinary skill in the art would not have had the detailed FPGA knowledge assumed by Petitioner's definition. *Id.* Patent Owner further contends the technical problem the '524 patent sought to address is in the field of High-Performance Computing ("HPC"). *Id.* at 3. Concatenating the experience Petitioner argues an artisan would have had with Patent Owner's assessment of the technical field, Patent Owner argues the result would have been a "mythical person" knowledgeable about both FPGAs and HPC. *Id.* at 30–33. According to Patent Owner, it would have been rare to find a person knowledgeable in both disciplines, and that any such person would have had more education and experience than that proposed by Petitioner. *Id.*

Patent Owner's assertions are unavailing. Patent Owner relies on the Declaration of Dr. Guccione to support its assertion that there were few engineers at the time of the '524 patent who knew how to program FPGAs to run software algorithms. PO Resp. 31–32 (citing Ex. 2146 ¶¶ 87, 193–198). Dr. Guccione testifies, for example, that implementing algorithms in FPGAs (i.e., hardware) is more complex than implementing algorithms in software, and therefore requires a different skillset. Ex. 2146 ¶ 87. Dr. Guccione's testimony, however, is at odds with what is reflected in the prior art of the period. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). As Petitioner points out, "numerous prior art references disclose computer architectures with multiple

[12] Patent Owner's declarant, Dr. Homayoun, agrees with "the level of education and skill" that a person of ordinary skill in the art would have according to Petitioner. Ex. 2102 ¶ 123.

processing elements and FPGAs used for network interface," including the main references on which Petitioner relies, Tsutsui and Tsutsui II. Reply 4 (citing Exs. 1007, 1009, 1040, 1041). The art of record therefore indicates that Petitioner's assessment of the education and experience required in the field of programming FPGAs is accurate.

Also, we find insufficient evidence that the level of ordinary skill in the art would have required specialized knowledge in the field of High Performance Computing. Patent Owner cites to portions of the '524 patent that describe enhancing overall processing speed in a multiprocessor computer architecture incorporating a number of memory algorithm processors, but has not shown why these systems are HPC architectures, much less limited to being HPC architectures. PO Resp. 4–5. The '524 patent does not limit the invention to HPC, but rather more broadly states

> The present invention relates, in general, to the field of computer architectures incorporating multiple processing elements. More particularly, the present invention relates to a switch/network adapter port ("SNAP") for clustered computers employing a chain of multi-adaptive processors ("MAP[]") . . . in a dual in-line memory module ("DIMM") format to significantly enhance data transfer rates over that otherwise available from the peripheral component interconnect ("PCI") bus.

Ex. 1001, 1:29–37. This description, however, is non-limiting, and indicates a shortcoming of systems with "multiple processing elements," namely very high latency due to the location of chips below the processor bus. Ex. 1001, 1:51–56. This evidence does not suggest the '524 patent is directed only to HPC systems.

We also find unavailing Patent Owner's argument that in assessing the level of skill in the art, Petitioner erred by focusing on the technical

solution—using programmable computing elements—rather than on the technical problem to be solved. PO Resp. 32; Sur-Reply 2–3. Patent Owner provides no legal basis to support its contention that the only appropriate factor to consider in determining the hypothetical person of ordinary skill in the art is the technical problem to be solved. Contrary to Patent Owner's assertion, several factors may be considered, including the types of problems encountered in the art, prior art solutions to those problems, rapidity with which innovations are made, sophistication of the technology, and educational level of active workers in the field. *Ruiz*, 234 F.3d at 666–667; *Custom Accessories*, 807 F.2d at 963. Moreover, such factors may or may not be present in every case, and one or more of the factors may predominate. *Ruiz*, 234 F.3d at 666–667; *see also Custom Accessories*, 807 F.2d at 963. Here, we have considered the entirety of the '524 entirety disclosure, and the prior art of record. Further, to the extent Patent Owner disputes the number of *actual* persons with the proposed education and technical experience at the time of the '524 patent, we note that "[t]he person of ordinary skill is a *hypothetical* person who is presumed to be aware of all the pertinent prior art." *Custom Accessories*, 807 F.2d at 962 (emphasis added).

For the foregoing reasons, we adopt Petitioner's proposal as to the level of ordinary skill in the art. We note that had we not adopted Petitioner's proposal that the relevant experience be specific to FPGAs—in particular, had we not articulated a specialty within the field of computer architecture—it would not have altered the outcome of this Decision. As we noted above, the level of skill in the art also may be reflected in the prior art. *See GPAC*, 57 F.3d at 1579; *Oelrich*, 579 F.2d at 91. Here, Tsutsui and

Tsutsui II, for example, reflect the appropriate level of skill in the art. We also note that to the extent we determine Petitioner has demonstrated certain claims are unpatentable as obvious, below, we make such findings under an even lower standard than that suggested by Patent Owner's arguments—namely, we determine the claims would have been obvious even without assuming the level of skill in the art requiring specialized knowledge in the field of High-Performance Computing. *See Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366 (Fed. Cir. 2012) ("[I]t is generally easier to establish obviousness under a higher level of ordinary skill in the art.").

C. Claim Construction

The parties agree that the '524 patent has expired. *See* Pet. 12; Prelim. Resp. 18. Accordingly, we apply the district court claim construction standard. *See* 37 C.F.R. § 42.100(b). In district court, claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). We determine that the following terms and limitations require construction.

1. "memory module bus"

Claim 1 recites a "memory module bus." Ex. 1001, 9:42. Based on the arguments presented in the Petition and Preliminary Response, we were

persuaded by Petitioner and preliminarily construed "memory module bus" in the Decision on Institution to mean "a bus used to communicate with a memory module." Dec. 10–11; *see* Pet. 13.

Patent Owner argues that "memory module bus" should be construed to mean "[a] bus designed to comply with applicable standards for connecting the main system processor(s) to a standardized memory device module according to the physical and logical connection protocols that are required by the memory module's specifications, which does not include a PCI bus or other I/O bus that is used to connect the system processor(s) to peripheral or external devices." PO Resp. 33–34; *see id.* at 39–40 (citing Ex. 2146 ¶ 216). Patent Owner asserts that the plain and ordinary meaning, and the meaning in the '524 patent specification, of "memory module bus" only includes "a bus that is intended to communicate with a memory module *according to the adopted standards* for interfacing with the memory module." *Id.* at 35; *see id.* at 39–40 (citing Ex. 2146 ¶ 216); *see* PO Sur-Reply 16–18. Patent Owner argues that the '524 patent specification explains that "the MAP element [is] inserted into a DIMM-standard memory slot." PO Resp. 40 (citing Ex. 1001, Fig. 5, 8:4–26). Patent Owner further argues that Petitioner's expert, Dr. Hauck, testifies that the '524 patent disclaims a PCI bus as a "memory module bus." *Id.* at 35–36 (citing Ex. 1003 ¶¶ 76–82).[13] Patent Owner argues that because Dr. Hauck's

[13] Patent Owner also requests sanctions on the basis that Petitioner exhibited a lack of good faith and violated its duty of candor by failing to alert the Board to the testimony of Dr. Hauck which Patent Owner alleges is inconsistent with Petitioner's proposed construction of "memory module bus." PO Resp. 35–36 (citing Ex. 1003 ¶¶ 76–81); PO Sur-Reply 27–28. We dismiss Patent Owner's request for sanctions for the reasons discussed

construction excludes a PCI bus, similar peripheral buses with similar characteristics should also be excluded. *Id.* at 36–37.

In response, Petitioner argues that Patent Owner's proposed construction is substantially different than what was proposed by Patent Owner in its Preliminary Response and in parallel litigation between the parties. Pet. Reply 5. Petitioner argues that nothing in the intrinsic or extrinsic record supports Patent Owner's contention that the "memory module bus" must be "designed to comply with applicable standards." *Id.* at 6–7. Petitioner also asserts that Patent Owner's proposed construction improperly extends the disclaimer of a PCI bus to other types of peripheral buses. *Id.* at 8–9. Petitioner further asserts that the PCI bus disclaimer is irrelevant, as the relied-upon prior art, Tsutsui, does not disclose a PCI bus. *Id.* at 8; *see also* Tr. 19:12–20:3, 21:1–11, 22:18–23:10 (explaining the same).

We are persuaded that "memory module bus" should be construed to mean "a non-PCI bus used to communicate with a memory module." This construction is consistent with the plain and ordinary meaning of "memory module bus," is consistent with the '524 patent specification, and incorporates the '524 patent specification's disclaimer of a standard PCI bus. *See* Ex. 1001, 7:56–59; Ex. 1003 ¶¶ 77–78 (citing Ex. 1001, Abstract, 1:29–67, 2:1–13, 4:7–13, 7:34–41, 8:4–29). We limit the scope of "memory module bus" to exclude a PCI bus given the specific statements in the '524 patent specification and the parties' agreement that the '524 patent

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below. *See infra* Section G. Moreover, *all of* the cited testimony in Dr. Hauck's declaration (Ex. 1003) was in the record and available to the Board at the time of institution.

disclaimed a PCI bus. PO Resp. 55 (citing Ex. 1003 ¶¶ 76–82; Ex. 2146 ¶ 210); *see also* Tr. 19:13–20:3 ("[I]f the Board wants to find disclaimer of a PCI bus, we made that argument in District Court. We believe it's disclaimed . . . ."). Specifically, the '524 patent specification explains how a PCI bus is different from the bus used in the disclosed invention and why the disclosed bus solves the problems that a PCI bus had at the time. *See, e.g.*, Ex. 1001, 1:29–67, 2:1–38, 4:7–13, 7:34–41, 8:4–29, code (57).

We are unpersuaded by Patent Owner's attempt to limit the scope of a "memory module bus" to require a connection "according to the adopted standards for interfacing with the memory module," or to extend the disclaimer beyond PCI buses. PO Resp. 35–37 (emphasis omitted). We are not persuaded that the claims of the '524 patent and the '524 patent specification support such a construction. The specification states that the disclosed arrangement has improved data transfer rates "over that otherwise available" from a PCI bus, but does not distinguish any other type of bus or generalize beyond PCI buses. *See, e.g.*, Ex. 1001, 1:31–37, 2:8–12, 4:7–13, 7:34–41, code (57). The specification also explains that controller 204 is "*conventionally coupled* to a number of DIMM slots 214." Ex. 1001, 7:56–57 (emphasis added). Thus, Patent Owner's proposed construction seeking to extend the explicit disclaimer to "other types of peripheral buses" with the "same characteristics" as a PCI bus does not find support in the intrinsic record. *See* PO Resp. 36–37. In addition, we are not persuaded that a construction using the term "applicable standards," as Patent Owner proposes, would be appropriate, as it is unclear what standards would or would not be encompassed within such a construction.

Accordingly, we construe "memory module bus" to mean "a non-PCI bus used to communicate with a memory module."

2. "a direct data connection coupled to said field programmable gate array for providing said altered data directly from said memory module bus to an external device coupled thereto"

Claim 1 recites "a direct data connection coupled to said field programmable gate array for providing said altered data directly from said memory module bus to an external device coupled thereto." Ex. 1001, 10:1–4. In the Decision on Institution, we preliminarily construed this limitation to mean that the field programmable gate array receives and operates on data directly from the memory module bus, producing altered data and providing that altered data directly to the external device via a direct data connection. Dec. 14.

The parties do not further argue the meaning of this limitation. We see no reason to depart from our construction in our Decision on Institution. Accordingly, we construe this limitation to mean that the field programmable gate array receives and operates on data directly from the memory module bus, producing altered data and providing that altered data directly to the external device via a direct data connection.

3. "control connection"

Claim 2 recites a "control connection." Ex. 1001, 10:6. We construe this limitation in order to address Patent Owner's argument that Tsutsui fails to disclose it. *See infra* Section II.D.2.b.iv.; PO Resp. 63. Patent Owner contends that "control connection" should be construed to mean "a bus or data communication channel separate from the memory module bus." PO Resp. 43 (emphasis omitted). Patent Owner contends that the '524 patent discloses that a "control connection" is "either a PCI bus, graphics bus,

accelerated graphics port (AGP) bus, or a system maintenance bus." *Id.* at 41–42 (citing Ex. 1001, 7:34–41, 10:10–24, Fig. 5). Patent Owner argues that a person with ordinary skill in the art would have understood that the '524 patent specification "describes the 'memory module bus' and 'control connection' as communication paths that are being used for fundamentally different things." *Id.* at 42 (citing Ex. 2146 ¶ 229). Petitioner does not proffer a definition for this term. *See generally* Pet. Reply 4–11. We are persuaded by Patent Owner, and construe "control connection," consistent with the '524 patent specification, to mean "a bus or data communication channel separate from the memory module bus."

4. *"processor of said computer system" and "plurality of processors"*

Claim 2 recites "a processor of said computer system" and claim 14 recites "a plurality of processors." Ex. 1001, 10:7, 10:39–40. We construe these limitations in order to address Patent Owner's argument that Tsutsui fails to disclose them. *See infra* Section II.D.2.b.v.; PO Resp. 63–64. Patent Owner argues that "processor of said computer system" should be construed to mean "the main system processor consisting of a microprocessor or an FPGA programmed to function as a von Neumann-style stored memory instruction processor." PO Resp. 43 (citing Ex. 2146 ¶¶ 231–233) (emphasis omitted). Patent Owner argues that the claim language differentiates the "processor of said computer system" from the "processor element" of claim 1. *Id.* Patent Owner further argues that a person of ordinary skill in the art in 2001 would understand "processor of said computer system" to refer to "main system processors coupled to the main memory modules via a memory module bus." *Id.* (citing Ex. 2146 ¶¶ 231–233).

Petitioner argues that Patent Owner has provided no intrinsic evidence to support its proposed construction. Pet. Reply 10–11. Petitioner contends that the ordinary meaning of "processor of said computer system," and as discussed in the '524 patent specification, would encompass "any processor in the computer system." *Id.* (emphasis omitted); Pet. 21–22 (citing Ex. 1003 ¶¶ 344, 346–349; Ex. 1001, Title, 1:29–37, 3:40–42, 5:17–24, Fig. 3, 3:66–4:2, 6:19–38).

We agree with Petitioner that the plain and ordinary meaning of "a processor in the computer system" is "any processor in the computer system." Pet. Reply 10–11. Although we agree with Patent Owner that the claim language demonstrates that the "processor of said computer system" is distinct from the "processor element" of claim 1, we are not persuaded that either the intrinsic or extrinsic record supports limiting the scope of this limitation to be "the main system processor" or a "processor consisting of a microprocessor or an FPGA programmed to function as a von Neumann-style stored memory instruction processor." Patent Owner's sole support for its proposed construction is the testimony of Dr. Guccione, and we do not credit that testimony given the lack of any support in the '524 patent claims, written description, or prosecution history. Accordingly, we construe "a processor in the computer system" to mean "any processor in the computer system that is not the processor element of claim 1."

Patent Owner further argues that "plurality of processors," as recited in claim 14, should be construed to mean "more than one processor." PO Resp. 43–44. Petitioner does not dispute this proposed construction. *See generally* Pet. Reply 4–11. We agree with Patent Owner that the plain and ordinary meaning of a "plurality of processors" is "more than one

processor." Accordingly, we construe "a plurality of processors" to mean "more than one processor."

5. Remaining Terms and Limitations

We determine that no other express claim construction analysis of any claim term is necessary. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (holding that only terms in controversy must be construed and only to the extent necessary to resolve the controversy) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Anticipation of Claims 1, 2, and 13–15 by Tsutsui

Petitioner contends that claims 1, 2, and 13–15 of the '524 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Tsutsui. Pet. 30–53. For the reasons discussed below, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, and 13–15 of the '524 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Tsutsui.

1. Tsutsui (Ex. 1007) [14]

Tsutsui is directed to a "system architecture applicable to high-

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[14] Petitioner asserts that Tsutsui qualifies as a prior art printed publication under 35 U.S.C. § 102(a). Pet. 22; Reply 13–16. Patent Owner contends that "Petitioner did not Authenticate EX1007 (Tsutsui [])," and that "[a]s a result, Petitioner has failed to prove that EX1007 is a prior art publication under 35 U.S.C. § 102(b)." *Id.*; PO Sur-Reply 13–14 (arguing that Petitioner "failed to authenticate EX1007"). Thus, Patent Owner's sole contention that Tsutsui (i.e., the document filed as Exhibit 1007) is not a prior art printed publication is that Petitioner failed to authenticate it. Patent Owner confirmed that to be the case during the hearing. Tr. 39:25–40:12 (in response to a question asking whether Patent Owner is contesting authentication or qualification as a printed publication, stating: "It's really just authentication . . . . In this case we're not conceding that it was publicly available but we haven't contested it but the authentication, yes, we're

performance and flexible transport data processing which includes complex protocol operation and a network control algorithm." Ex. 1007, 1. Tsutsui discloses an FPGA and micro-processing unit ("MPU") system named Yet Another Re-Definable System ("YARDS"). *Id.* YARDS comprises three programmable devices, thereby providing high flexibility. *Id.* The system "supports various styles of coupling between the FPGAs and the MPU." *Id.* The system architecture is suitable for implementing flexible and real-time transport data processing operations. *Id*.

2. Analysis

a. Petitioner's Contentions

Independent claim 1 recites "[a] processor element for a memory module bus of a computer system." Ex. 1001, 9:42–43. Petitioner contends that Tsutsui discloses "multiple FPGAs, the VME-I/F, the Interrupt Signals from the FPGAs to the MPU, and the Direct-I/O connection," which comprise a "processing element." Pet. 30–31 (citing Ex. 1007, Fig. 1). Petitioner argues that the "'FPGAs' within YARDS can be 'treated as co-processors or special peripheral devices of the MPU.'" *Id.* at 31 (quoting Ex. 1007, 2; citing Ex. 1003 ¶¶ 188–189). Petitioner further argues that the "processing element" is "coupled to the Local Bus of YARDS," and, therefore, is "for a memory module bus." *Id.* (citing Ex. 1007, 3; Ex. 1003 ¶¶ 190, 197) (emphasis omitted).

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pressing that argument."). We address Patent Owner's authentication arguments above in deciding Patent Owner's Motion to Exclude Tsutsui as unauthenticated under Federal Rule of Evidence 901. *See supra* Section II.A.2; PO Mot. 5–7. Petitioner has proven, for the reasons stated in its papers, which are supported by the evidence of record cited in those papers, that Tsutsui is a prior art printed publication under 35 U.S.C. § 102(a). *See* Pet. 22; Reply 13–16.

Claim 1 further recites "a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided directly thereto on said memory module bus." Ex. 1001, 9:44–47. Petitioner contends that Tsutsui discloses FPGAs that are configured to perform processing functions. Pet. 32 (citing Ex. 1007, 2–3). Petitioner further argues that Tsutsui discloses that FPGAs, during operations and maintenance processing ("OAM") cell operations, determine the appropriate action for extracted cell data, including determining the control method using a control algorithm and accessing a database. *Id.* at 34 (citing Ex. 1007, 3, Fig. 16; Ex. 1003 ¶ 208). Petitioner also argues that Tsutsui discloses FPGAs that perform an algorithm on a received operand, including performing hash functions on received data, processing data provided directly from memory, and "re-shaping" data before transmission, which "would necessarily include '*identified algorithms*' that operate on data." *Id.* at 32–33, 35–36 (citing Ex. 1007, 1, 3; Ex. 1003 ¶¶ 205–207, 217–220). According to Petitioner, Tsutsui's "re-shaping" of data includes "reordering and changing the spacing of the ATM cells within a stream." *Id.* at 35 (citing Ex. 1007, 1, 3; Ex. 1021, 2:36–55; Ex. 1003 ¶¶ 211–214). Petitioner argues that the "re-shaping" of data constitutes altering data. *Id.* (citing Ex. 1021, 2:36–56; Ex. 1003 ¶¶ 211–214). Petitioner also argues that there is "a direct connection between the Local Bus and the FPGA." *Id.* (citing Ex. 1007, 2).

Claim 1 also recites "a direct data connection coupled to said field programmable gate array for providing said altered data directly from said memory module bus to an external device coupled thereto." Ex. 1001, 10:1–4. As discussed above, we construe this limitation to mean that the field

programmable gate array receives and operates on data directly from the memory module bus, producing altered data and providing that altered data directly to the external device via a direct data connection. *See supra* Section II.B.2. Petitioner argues that, under this construction, Tsutsui discloses that the "direct I/O channel enables a direct exchange of signals between other devices and the FPGA card," where the Direct I/O channel is directly connected to an FPGA. Pet. 41 (quoting Ex. 1007, 2; citing Ex. 1007, Fig. 1).

Notwithstanding Patent Owner's arguments, which we address below, we are persuaded by Petitioner that Tsutsui discloses the limitations of claim 1. As discussed above, Tsutsui discloses an FPGA and MPU system named YARDS. Ex. 1007, 1; *see supra* Section II.D.1. The main parts of the system include programmable switching devices and 2-port SRAMs. Ex. 1007, 2. YARDS supports three different styles of connection between the FPGAs and MPUs: a bus, a direct interrupt, and a 2-port SRAM channel. *Id.* Using the local bus, the transport data stream is directly input into the FPGA, which executes operations and transfers the results to the main memory. *Id.* at 3. After the MPU completes high level protocol operations, the FPGA "re-shapes" the data as the output transport data stream. *Id.* The system further includes external interfaces via a VME-Bus and Direct-I/O. *Id.* at 2. Accordingly, we are persuaded by Petitioner that Tsutsui discloses the claimed FPGA and direct data connection of the processor element for a memory module bus of a computer system.

Petitioner provides a similar analysis for dependent claims 2 and 13–15, explaining exactly how Tsutsui discloses the limitations of the claims. Pet. 30–53. We find that Petitioner supports its arguments with credible

evidence, and we are persuaded by Petitioner that Tsutsui discloses the limitations of claims 2 and 13–15. *See id*. Accordingly, notwithstanding Patent Owner's arguments, which we address below, we are persuaded that Tsutsui anticipates claims 1, 2, and 13–15.

b. Patent Owner's Arguments

Patent Owner argues that Tsutsui fails to disclose the following limitations: (i) "memory module bus" (claim 1), (ii) "data provided directly thereto on said memory module bus" (claim 1), (iii) "direct data connection" (claim 1), (iv) "control connection for indicating to a processor of said computer system" (claim 2), and (v) "a plurality of processors" (claim 14). PO Resp. 55–64. We address these arguments in turn.

i. "memory module bus"

Patent Owner argues that Tsutsui fails to disclose the claimed "memory module bus," as Patent Owner construes the term. PO Resp. 55–57; PO Sur-Reply 20–23. Specifically, Patent Owner argues that the proper claim construction for "memory module bus" excludes a PCI bus (*see supra* Section II.C.1), and argues that Tsutsui's Local Bus is "functionally equivalent" to a PCI bus. PO Resp. 55–56 (citing Ex. 1003 ¶¶ 76–82; Ex. 2146 ¶¶ 210, 264–265; Ex. 1007, 3). Patent Owner further argues that Tsutsui's Local Bus is not a "memory module bus" because there is no evidence that it is used to communicate with a memory module. *Id.* at 56–57 (citing Ex. 1007, Fig. 1); PO Sur-Reply 21–22. Patent Owner argues that the Local Bus "has . . . many components attached to it" and "supports only one bus master at a time," requiring "bus contention," where local bus congestion "is the same technical problem addressed by the patent." PO

Resp. 56 (citing Ex. 2146 ¶ 265, Ex. 1007, 3) (emphasis omitted); PO Sur-Reply 20–21.

In response, Petitioner asserts that Patent Owner's arguments are both unsupported and premised on an improper claim construction. Pet. Reply 17–18. Petitioner further argues that Patent Owner fails to explain the alleged equivalence between Tsutsui's Local Bus and a PCI bus. *Id.* at 17 (citing PO Resp. 55). Petitioner argues that Patent Owner's arguments relating to bus contention and the Local Bus "suffer[ing] from congestion" are not even requirements of Patent Owner's proposed claim construction. *Id.* Finally, Petitioner argues that Tsutsui satisfies Patent Owner's proposed construction because Tsutsui's Local Bus is not a PCI or I/O bus that connects to peripheral/external devices. *Id.* at 17–18 (citing Pet. 30–31; Pet. Reply 17; Ex. 2156, 447; Ex. 1003 ¶¶ 130, 197; Ex. 1007, Fig. 1).

We are not persuaded by Patent Owner's arguments. We construe "memory module bus" to mean "a non-PCI bus used to communicate with a memory module." *See supra* Section II.C.1. Tsutsui does not describe the Local Bus as a PCI bus. Tsutsui discloses a "processing element" that includes multiple FPGAs, the VME-I/F, Interrupt Signals from the FPGAs to the MPU, and the Direct-I/O connection, and discloses that the "processing element" is "coupled to the Local Bus of YARDS." Ex. 1007, 1–3, Figs. 1, 13; Pet. 31 (citing Ex. 1003 ¶¶ 190, 197). Tsutsui discloses FPGAs and DRAM (SIMM) both coupled to the Local Bus. Ex. 1007, 1–3. Further, we are not persuaded by Patent Owner's argument that Tsutsui's Local Bus is a PCI bus because Patent Owner merely alleges that the Local Bus "shares characteristics that a [person of ordinary skill in the art] would recognize are indicative of a PCI bus," but fails to set forth persuasive

evidence and argument to establish that Tsutsui's Local Bus is functionally the same as a PCI Bus. PO Resp. 55–56 (citing Ex. 2146 ¶ 264). That is, even if the Local Bus shared certain characteristics with a PCI bus, that does not mean that the Local Bus is the same thing as a PCI bus. As such, we are not persuaded that Tsutsui's Local Bus is a PCI Bus. We determine that Tsutsui's DRAM is memory and is connected to the Local Bus, and, therefore, the Local Bus is a "memory module bus." Accordingly, we are not persuaded by Patent Owner's argument that Tsutsui fails to disclose a "memory module bus."

ii. "data provided directly thereto on said memory module bus"

Patent Owner further argues that Tsutsui fails to disclose "data provided directly thereto on said memory module bus" because "the FPGAs in Tsutsui never receive data directly from the memory module bus." PO Resp. 57. Rather, Patent Owner argues that "the MPU and FPGAs communicate through shared memory to avoid bus contention of the 'Local Bus.'" *Id.* at 57–59 (citing Ex. 1007, 2–4, Figs. 2, 11, 17; Ex. 2146 ¶¶ 242–244, 267, 269–270). Patent Owner further argues that Tsutsui did not implement, and teaches away from, the "Typical Implementation Style Using Local Bus" depicted in Figure 11 of Tsutsui because data communication between the MPU and FPGAs occurs frequently, and therefore the local bus "would be blocked by the 'repetitive data transformations among the MPU, the FPGAs, and the memories.'" *Id.* at 58–59 (quoting Ex. 1007, 2–4). Patent Owner argues that "[t]he FPGAs do not receive any data directly from the Local Bus," as Tsutsui uses a 2-port SRAM channel "via the I-Cube switching device" between the MPU and FPGAs to avoid problems associated with the local bus architecture. *Id.*

(citing Ex. 1007, 2; Ex. 2146 ¶¶ 267, 269–270). Finally, according to Patent Owner, "any data path that includes the I-Cube switch cannot meet the 'direct' data connection requirements of Claim 1 because it is unknown whether the data would be stored in the SRAM memory contained in the I-Cube switching device," and an ambiguous disclosure is insufficient to show anticipation. *Id.* at 60–61.

Petitioner responds that Tsutsui teaches the use of the bus style of Figure 11 in which data is directly communicated between the main memory and FPGAs. Pet. Reply 20 (citing Ex. 1007, 2–3; Ex. 1003 ¶ 225). Further, Petitioner asserts that Patent Owner's arguments regarding teaching away are not relevant to the issue of anticipation. *Id.* (citing *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1344 (Fed. Cir. 2012)).

We agree with Petitioner. Tsutsui discloses that "YARDS supports three different styles of connection between FPGAs and [the] MPU: a bus, a direct interrupt, and a 2-port SRAM channel." Ex. 1007, 2. Although Tsutsui discloses expected "frequent[]" data communication between the MPU and FPGAs, Tsutsui expressly discloses that YARDS supports a local bus connection between the MPU and FPGAs. *Id.* at 2–3 ("The bus style is the same as the conventional one. . . . Using only the bus architecture, an implementation style of our target system should be similar to Figure 11. The transport data stream is input into the FPGA directly."), Fig. 1 (depicting the connection between each FPGA and the Local Bus, which Tsutsui states on page 2 are "direct[]" connections), Fig. 9, (depicting the conventional Local Bus style), Fig. 11 (depicting a direct connection to the FPGA via the Local Bus). We credit Dr. Hauck's testimony as to how a person of ordinary skill in the art would have understood Tsutsui in that

regard, as it is consistent with the figures and language used in the reference. Ex. 1003 ¶¶ 217–224. Further, even with respect to the I-Cube switching device implementation in particular, based on the disclosures of Tsutsui cited above that the system can implement local bus interconnection as shown in Figures 9 and 11, as well as Tsutsui's statement that the I-Cube switching device "supports various types of connections among its pins such as . . . a bus," a person of ordinary skill in the art would have understood the I-Cube switching device implementation to use a local bus architecture with direct connection to the FPGA. *Id.* ¶ 225 (quoting Ex. 1007, 2). Given the express disclosure in Tsutsui of direct connection to the FPGA, we agree.

Accordingly, we determine that Tsutsui discloses a local bus connection to the FPGAs that provides data that the FPGAs then "re-shap[e]" and output (Pet. 35–36 (citing Ex. 1007, 1–3; Ex. 1003 ¶¶ 217–220)), and we are not persuaded by Patent Owner's argument that Tsutsui fails to disclose that the FPGA alters data "provided directly thereto on said memory module bus."

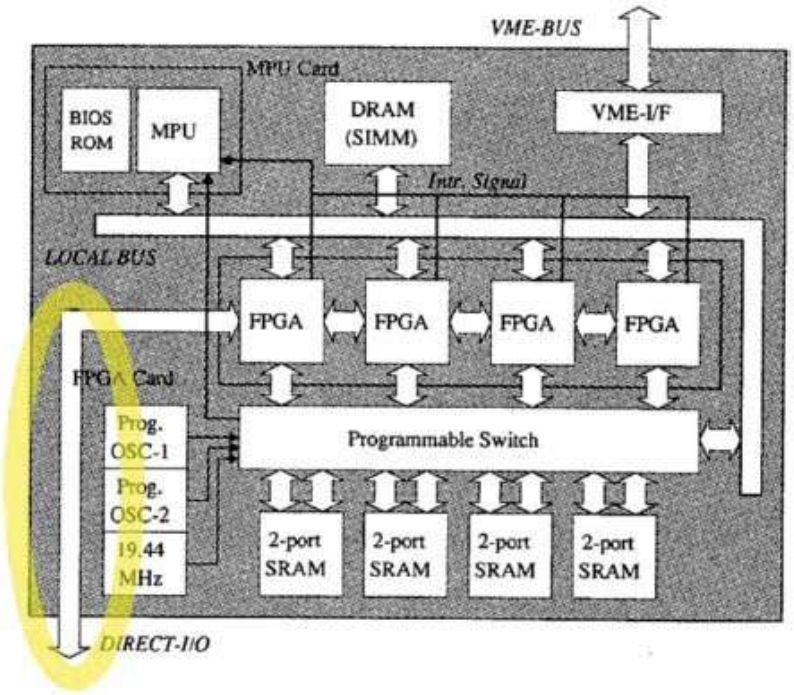
iii. "direct data connection"

Patent Owner further argues that Tsutsui fails to disclose a "direct data connection" between the FPGAs and an external device. PO Resp. 61–63. Specifically, Patent Owner argues that in Tsutsui, "all data going in and coming out of the FPGAs gets stored in either the 2-Port SRAM on the YARDs card, the memory contained in the I-Cube, or both." *Id.* at 61. Patent Owner further asserts that Petitioner has failed to show support for Tsutsui's VME-BUS I/F acting as a direct data connection to external devices, and that Tsutsui instead uses the VME bus for controlling and

monitoring the system. *Id.* at 61–62 (citing Ex. 2146 ¶¶ 277–278; Ex. 1003 ¶¶ 281–282).

Petitioner responds that Tsutsui discloses that the "Direct I/O connection is connected directly to the FPGAs, *i.e.*, without intervening memory," as the claimed direct data connection. Pet. Reply 21–22 (citing Pet. 40–43; Ex. 1007, Figs. 1, 13) (emphasis omitted). Petitioner argues that Patent Owner's expert, Dr. Guccione, explains that the Direct I/O connection of Tsutsui "is a fast, dedicated set of signals on the FPGA that connect directly to the data (network) interface." *Id.* (quoting Ex. 2146 ¶ 274) (emphasis omitted).

We agree with Petitioner. As explained above, we construe "direct data connection" to mean that the field programmable gate array receives and operates on data directly from the memory module bus, producing altered data and providing that altered data directly to the external device via a direct data connection. *See supra* Section II.B.2. Tsutsui discloses the Direct I/O provides a connection to the FPGAs without intervening memory. Ex. 1007, Figs. 1, 13; *see* Pet. Reply 21–22 (citing Pet. 40). Petitioner provides the following annotated version of Figure 1 of Tsutsui (Pet. 40):



The annotated Figure 1 depicts the "DIRECT-I/O" connection to a FPGA, which Tsutsui describes as "enabl[ing] a direct exchange of signals between other devices and the FPGA card." Ex. 1007, 2; *see id.*, Figs. 1, 13 (both showing the "DIRECT-I/O" connection); Pet. 40–43. Tsutsui further states that "FPGAs have many direct I/O ports and are suited to handle real-time operations for continuous data streams." *Id.* at 3. Dr. Guccione also agrees that the "DIRECT-I/O" connection "is a fast, dedicated set of signals on the FPGAs that connect *directly* to the data (network) interface." Ex. 2146 ¶ 274 (emphasis added).

Accordingly, we determine that Tsutsui's description of the direct I/O channel discloses the claimed "direct data connection."

iv. "control connection"

Patent Owner further argues Tsutsui fails to disclose a "control connection . . . for indicating to a processor of said computer system," as recited in claim 2. PO Resp. 63 (citing Ex. 2146 ¶¶ 282–283). Patent

Owner argues that a "control connection implies some sophisticated method of communicating status information back to the processor, and more critically, a way to receive information back, for the purposes of control." *Id.* Patent Owner argues that the '524 patent specification discloses the use of a PCI bus that permits bi-directional data flow. *Id.*

We are not persuaded by Patent Owner's argument. Claim 2 recites "a control connection coupled to said processor element for indicating to a processor of said computer system an arrival of data on said data connection from said external device." As discussed above, we adopt Patent Owner's proposed construction of "control connection" to mean "a bus or data communication channel separate from the memory module bus." *See supra* Section II.C.3. As argued by Patent Owner, a person with ordinary skill in the art would have understood that the "memory module bus" and "control connection" are separate communication paths. *See id*.

Claim 2 only requires indicating to the processor the *arrival* of data from an external device. Petitioner contends that the YARDS processor element includes interrupt signals that enable the FPGA to control the behavior of the processor element. Pet. 43 (citing Ex. 1007, 2–3; Ex. 1003 ¶ 308). That is, the interrupt signal indicates the *arrival* of data to the processor element. We see no reason to limit the scope of claim 2 to require a PCI Bus or a bi-directional flow of data. As such, we are not persuaded by Patent Owner's argument.

v. "plurality of processors"

Patent Owner further argues that Tsutsui fails to disclose a "plurality of processors," as recited in claim 14. PO Resp. 64 (citing Ex. 2146 ¶ 284). Patent Owner argues that claim 14 requires the main system host processor

to be a plurality of instruction-based processors, and Tsutsui's YARDS card only discloses a single MPU microprocessor. *Id.* (citing Ex. 2146 ¶ 274–280, 285).

Petitioner responds that Patent Owner's argument is based on an erroneous claim construction. Pet. Reply 24. We agree. As noted above, we construe "a plurality of processors" to mean "more than one processor," and "processor" to mean "any processor in the computer system that is not the processor element of claim 1." *See supra* Section II.C.4. As such, we are not persuaded by Patent Owner's argument that claim 14 requires a main system host processor to be a plurality of instruction-based processors. PO Resp. 64. Tsutsui discloses a plurality of processors by disclosing a processing element that includes multiple FPGAs that process data. Ex. 1007, 3; Pet. 48–49 (citing Ex. 1003 ¶¶ 351–352, 353–354). Accordingly, we are not persuaded by Patent Owner's argument.

3. Conclusion

We are persuaded by Petitioner's arguments, as they are supported by the cited evidence, including the testimony of Dr. Hauck, which we credit, explaining how a person of ordinary skill in the art would have understood the disclosure of Tsutsui, and notwithstanding Patent Owner's arguments addressed above. We determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, and 13–15 of the '524 patent are anticipated by Tsutsui.

E. Obviousness of Claims 1, 2, and 13–15 over Tsutsui and Tsutsui II

Petitioner contends that claims 1, 2, and 13–15 of the '524 patent are unpatentable under 35 U.S.C. § 103 as obvious over Tsutsui and Tsutsui II.[15] Pet. 65–69. For the reasons discussed below, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, and 13–15 of the '524 patent are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Tsutsui and Tsutsui II.

1. Tsutsui II (Ex. 1009)

Tsutsui II is cited by Tsutsui as a reference, and shares two of the same authors as Tsutsui. Ex. 1007, 4. Tsutsui II discloses a FPGA for high-speed digital telecommunication systems. Ex. 1009, 486. Tsutsui II states that the FPGA can realize high-speed transport data processing and its inter-chip connection mechanism enables flexible multi-FPGA modules. *Id.* Tsutsui II further discloses the use of the FPGA in a transport processing system that executes operations due to extraction of data structures from a bit-serial main data stream. *Id*. The data structures consist of two types of data: one being for transportation control (i.e., the "Header") and the other for the transport of data (i.e., the "Payload"). *Id.* Tsutsui II discloses that transport processing mainly treats the Header part to determine the operation appropriate for a corresponding data block, although other essential operations for transport data, such as bit-error detection/correction and scrambling, are included. *Id.* at 486–87.

[15] Petitioner argues, and we agree, that Tsutsui II is a prior art printed publication under 35 U.S.C. §§ 102(a) and (b). *See* Pet. 29.

2. Analysis

a. Petitioner's Contentions

As discussed above, Petitioner contends that Tsutsui discloses the limitations of claim 1. *See supra* Section II.D.2.a. Petitioner further argues that Tsutsui II discloses an FPGA that performs data processing functions, including scrambling data. Pet. 65 (citing Ex. 1009, 486). As such, Petitioner argues that to the extent the FPGA of Tsutsui is not "operative to alter data," as recited in claim 1, the combination of Tsutsui and Tsutsui II discloses "a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided directly thereto on said memory module bus." *Id.* at 65–66. Specifically, according to Petitioner, it would have been obvious to include Tsutsui II's data scrambling in the system of Tsutsui, such that the Direct-I/O connection in Tsutsui ("direct data connection") would provide scrambled payload data ("altered data") to the ANT card ("external device") connected to the Direct-I/O connection. *Id.* at 65–66, 69. That is, the only modification being made to Tsutsui is the alteration of data by the FPGA (i.e., scrambling data rather than re-shaping data).

Petitioner argues that a person with ordinary skill in the art would have been motivated to combine Tsutsui and Tsutsui II because Tsutsui cites to Tsutsui II as disclosing "an original FPGA especially designed for high-speed telecommunication data processing." *Id.* at 67 (quoting Ex. 1007, 1). Petitioner further argues that a person with ordinary skill in the art would have looked to Tsutsui II to combine its scrambling processing with the ATM protocol system of Tsutsui. *Id.* (citing Ex. 1009, 486; Ex. 1003 ¶ 240). Petitioner further contends that Tsutsui and Tsutsui II are analogous art to

the '524 patent and the combination of Tsutsui and Tsutsui II "would have been only the arrangement of old elements . . . with each performing the function it was known to perform and yielding no more than what one would expect from such an arrangement (low level transport processing on a multi-FPGA system)." *Id.* (citing Ex. 1003 ¶ 238).

Notwithstanding Patent Owner's arguments and alleged objective indicia of nonobviousness, which we address below, we are persuaded by Petitioner that the combination of Tsutsui and Tsutsui II discloses the limitations of claim 1, and a person with ordinary skill in the art would have combined Tsutsui with Tsutsui II. Pet. 65–69. As discussed above, we find that Tsutsui discloses the limitations of claim 1. Tsutsui II discloses features for high-speed transport data processing, including "bit-error detection/correction and scrambling." Ex. 1009, 486. As such, we agree with Petitioner that the combination of Tsutsui and Tsutsui II discloses "a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided directly thereto on said memory module bus." We specifically agree with Petitioner that a person with ordinary skill in the art would have looked to improve synchronization, and would have determined that application of a scrambling technique, as taught by Tsutsui II, would have improved synchronization. *See* Pet. 68–69. For the reasons discussed above, Petitioner's arguments are supported by the record, including the testimony of Dr. Hauck, and we find them persuasive. Accordingly, we are persuaded that a person with ordinary skill in the art would have been motivated to combine Tsutsui and Tsutsui II. *See* Pet. 66–69; Ex. 1003 ¶¶ 233–244.

Petitioner provides an analysis for dependent claims 2 and 13–15, explaining exactly how the combination of Tsutsui and Tsutsui II discloses the limitations of the claims, and articulates a rationale to combine Tsutsui and Tsutsui II. Pet. 43–53, 65–69. We find that Petitioner supports its arguments with credible evidence, and we are persuaded by Petitioner that Tsutsui and Tsutsui II disclose the limitations of claims 2 and 13–15 and there would have been reason for a person with ordinary skill in the art to combine Tsutsui and Tsutsui II. *See id*.

b. Patent Owner's Arguments

Patent Owner argues that the combination of Tsutsui and Tsutsui II fails to disclose certain elements of independent claim 1 for the same reasons asserted in opposing Petitioner's anticipation challenge of claims 1, 2, and 13–15. *See* PO Resp. 67; *supra* Section II.D.2.b. We do not repeat those arguments here. We are not persuaded by Patent Owner's arguments for the same reasons discussed above. *See id.*

Patent Owner does not separately argue that Tsutsui II in combination with Tsutsui fails to disclose "a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto and operative to alter data provided directly thereto on said memory module bus." *See generally* PO Resp. 67–69; PO Sur-Reply 25–26. Rather, Patent Owner generally argues that a person with ordinary skill in the art "would not [have been] motivated to make the proposed combination of Tsutsui with the other prior art." PO Resp. 71. Patent Owner further generally argues that "Petitioner and its expert resort to both hindsight reasoning and *ipse dixit* errors that are generally fatal to [*inter partes* review] petitions." *Id.* at 72–73. Petitioner argues that Patent Owner does not address any of the

Petition's motivation arguments in detail and improperly incorporates material by reference. Pet. Reply 27–29.

We are not persuaded by Patent Owner's arguments. Patent Owner generally alleges deficiencies in Petitioner's arguments towards a rationale to combine Tsutsui and Tsutsui II, but fails to set forth persuasive argument and evidence to undermine Petitioner's showing that a person with ordinary skill in the art would have been motivated to combine Tsutsui and Tsutsui II. That is, we are not persuaded by Patent Owner's general allegations that a person with ordinary skill in the art would not have been motivated to modify Tsutsui. Rather, Petitioner has set forth multiple persuasive reasons to combine Tsutsui and Tsutsui II (two related references with very similar disclosures), and Patent Owner has not meaningfully contested Petitioner's arguments.

As discussed above, as argued by Petitioner and supported by Dr. Hauck's testimony, a person with ordinary skill in the art would have been motivated to combine Tsutsui and Tsutsui II because Tsutsui cites to Tsutsui II as disclosing "an original FPGA especially designed for high-speed telecommunication data processing." Pet. 67 (quoting Ex. 1007, 1). Furthermore, Tsutsui provides explicit motivation to look to Tsutsui II's disclosure, stating the system of Tsutsui II "is useful in implementing lower-layer transport operations." *Id.* (quoting Ex. 1007, 1). Petitioner persuasively argues that a person with ordinary skill in the art, moreover, would have looked to Tsutsui II to combine its scrambling processing with the ATM protocol system of Tsutsui because Tsutsui II refers to scrambling as an "essential operation[] for transport data." *Id.* (citing Ex. 1009, 486; Ex. 1003 ¶ 240). Petitioner further contends, and we agree, that Tsutsui and

Tsutsui II are analogous art to the '524 patent and the combination of Tsutsui and Tsutsui II "would have been only the arrangement of old elements (the system of Tsutsui with the FPGA payload scrambling processing of Tsutsui II) with each performing the function it was known to perform and yielding no more than what one would expect from such an arrangement (low level transport processing on a multi-FPGA system)." *Id.* at 67 (citing Ex. 1003 ¶ 238).

Accordingly, we are not persuaded by Patent Owner's general allegations of deficiencies in Petitioner's arguments regarding a motivation to combine.

Patent Owner additionally argues, with respect to all of Petitioner's asserted obviousness combinations, that Dr. Hauck's testimony is conclusory, grounded in hindsight bias, fails to disclose the underlying facts or data on which his opinions are based under 37 C.F.R. § 42.65(a), fails to consider whether the asserted combinations were "feasible," and "assume[s] all the benefits [of the asserted combinations] and ignore[s] any drawbacks of cobbling together [the] prior art as proposed in the Petition." PO Resp. 71–74; PO Sur-Reply 13. Patent Owner acknowledges Dr. Hauck's experience with FPGAs, but argues that he "lacks the expertise in memory system design and computer architecture that are necessary in this case." PO Sur-Reply 13. We do not see how any such lack of experience undermines Dr. Hauck's testimony regarding how a person of ordinary skill in the art would have understood the FPGA-related disclosures of Tsutsui and Tsutsui II and why a person of ordinary skill in the art would have been motivated to combine their teachings. To the extent Patent Owner argues that we should not afford Dr. Hauck's declaration any weight, we

appropriately weigh Dr. Hauck's testimony pertaining to Petitioner's anticipation ground and obviousness ground premised on the combination of Tsutsui and Tsutsui II based on the specific testimony provided to determine whether Petitioner has established, by a preponderance of the evidence, the unpatentability of the challenged claims.

3. Objective Indicia of Nonobviousness

Patent Owner also argues that objective indicia of nonobviousness demonstrate that claims 1, 2, and 13–15 would not have been obvious to a person of ordinary skill in the art. PO Resp. 74–75. Patent Owner lists various alleged types of indicia of nonobviousness, including long-felt need, teaching away, well-known limitations, commercial success, and unexpected results, and provides citations to various documents. *Id.* Patent Owner's citations to documents appear to indicate that the documents support Patent Owner's listed types of objective indicia of nonobviousness.

Patent Owner, however, fails to provide any argument or analysis demonstrating the nonobviousness of the claims. At best, Patent Owner's citations are an inappropriate incorporation by reference of documents. 37 C.F.R. § 42.6(a)(3). Patent Owner neither argues that there is a presumption of a nexus between the claims and the objective indicia of nonobviousness nor provides any explanation establishing a nexus between any objective evidence of nonobviousness and the challenged claims. *See generally* PO. Resp. 74–75. For example, Patent Owner does not explain how the cited testimony shows skepticism in the industry regarding the claimed processor element. Nor does Patent Owner provide any explanation or analysis demonstrating that any products embody the claimed processor element to establish nexus or show commercial success. Accordingly, we

conclude that Patent Owner's evidence purportedly showing long felt need, skepticism in the industry, teaching away, well-known limitations, commercial success, and unexpected results does not weigh in favor of nonobviousness of the challenged claims.

4. Conclusion

For the foregoing reasons, we are persuaded that Petitioner has shown by a preponderance of the evidence that claims 1, 2, and 13–15 of the '524 patent are unpatentable as obvious over the combination of Tsutsui and Tsutsui II.

F. Additional Grounds

Petitioner also challenges claims 1, 2, and 13–15 as obvious over Tsutsui alone, claim 2 as obvious over Tsutsui and Stone, with or without Tsutsui II, claim 14 as obvious over Tsutsui and Collins, with or without Tsutsui II, and claim 15 as obvious over Tsutsui and Hayashi, with or without Tsutsui II. Pet. 53–65, 69–80. Petitioner has proven by a preponderance of the evidence that these claims are unpatentable on other grounds. *See supra* Sections II.D–E. As such, we need not address Petitioner's alternative grounds of unpatentability as to claims 1, 2, and 13–15.

G. Request for Sanctions

Patent Owner "requests a finding that Petitioner violated its duty of candor in this proceeding, and requests appropriate sanctions." PO Resp. 35–36; PO Sur-Reply 27–28. Specifically, Patent Owner argues that Petitioner failed to "cite its own expert's testimony" that contradicted its position. *Id.* Patent Owner argues that the failure to "bring this testimony to

the attention of the Board" was a violation of Petitioner's duty of candor to the Board. *Id.* (citing 37 C.F.R. §§ 42.11, 42.12).

"Relief, other than a petition requesting the institution of a trial, must be requested in the form of a motion." 37 C.F.R. § 42.20(a). 37 C.F.R. § 42.11(d)(2) permits a party, under certain circumstances, to file a motion for sanctions based on conduct that violates the duty of candor in representations made to the Board. *See* 37 C.F.R. §§ 42.11(a), (c). It requires, however, that such a motion for sanctions "must be made separately from any other motion" and "must be authorized by the Board under § 42.20 prior to filing the motion." 37 C.F.R. § 42.11(d)(2). It also requires that such a motion be served on opposing counsel "[a]t least 21 days prior to seeking authorization to file a motion for sanctions" and must not be filed or presented to the Board if withdrawn or appropriately corrected within twenty-one days of service of the proposed motion. *Id.*

Here, Patent Owner has requested a finding of unspecified sanctions in Patent Owner's Sur-Reply. PO Sur-Reply 27–28. Patent Owner never requested or obtained authorization from the Board before filing a motion for sanctions, and did not file a motion for sanctions separate from "any other motion." Furthermore, Patent Owner does not present any evidence or persuasive argument that it had served Petitioner with a proposed motion for sanctions, thereby allowing Petitioner to appropriately correct its alleged violation. As such, Patent Owner has not followed the proper procedure set forth in 37 C.F.R. § 42.11(d)(2), and, accordingly, Patent Owner's request for sanctions is dismissed.

H. Constitutionality of the Proceedings

Patent Owner "objects to the entirety of these proceedings based on the Federal Circuit's recent opinion in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019)." PO Sur-Reply 26. Patent Owner argues that "the current structure of the Board violates the Appointments Clause." *Id.* (citing *Arthrex*, 941 F.3d at 1335). Patent Owner "requests that this proceeding be dismissed in its entirety on the grounds that the panel lacks the constitutional authority to enter a final decision in this case." *Id.* at 27.

However, Patent Owner's constitutional challenge as to this issue—whether the as-constituted panel is constitutional—has been addressed by the Federal Circuit's decision. *See Arthrex*, 941 F.3d at 1337 ("This as-applied severance . . . cures the constitutional violation."). Accordingly, we do not consider this issue any further.

III. CONCLUSION

Based on the information presented, we conclude that Petitioner has shown, by a preponderance of the evidence, that claims 1, 2, and 13–15 of the '524 patent are unpatentable.[16]

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 2, 13–15	102	Tsutsui	1, 2, 13–15	

[16] As discussed above, we do not reach Petitioner's challenges to claims 1, 2, and 13–15 as obvious over Tsutsui alone, claim 2 as obvious over Tsutsui and Stone, with or without Tsutsui II, claim 14 as obvious over Tsutsui and Collins, with or without Tsutsui II, and claim 15 as obvious over Tsutsui and Hayashi, with or without Tsutsui II. *See supra* Section II.F.

1, 2, 13–15	103	Tsutsui		
1, 2, 13–15	103	Tsutsui and Tsutsui II	1, 2, 13–15	
2	103	Tsutsui and Stone, with or without Tsutsui II		
14	103	Tsutsui and Collins, with or without Tsutsui II		
15	103	Tsutsui and Hayashi, with or without Tsutsui II		
Overall Outcome			1, 2, 13–15	

IV. ORDER

After due consideration of the record before us, and for the foregoing reasons, it is:

ORDERED that claims 1, 2, and 13–15 of the '524 patent are held unpatentable;

FURTHER ORDERED that Patent Owner's request for sanctions is *dismissed*;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 63) is *denied-in-part* and *dismissed-in-part*;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 64) is *denied-in-part* and *dismissed-in-part*; and

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2018-01604
Patent 7,421,524 B2

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