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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2018-01000
Patent 6,465,743 B1

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges.*

BAER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Petitioner Micron Technology, Inc. filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1–8 of U.S. Patent No. 6,465,743 B1 (Ex. 1001, "the '743 patent"). Pursuant to 35 U.S.C. § 314(a), we determined Petitioner showed a reasonable likelihood that it would prevail in establishing the unpatentability of all challenged claims and instituted an *inter partes* review. Paper 9, 21–22. Patent Owner North Star Innovations, Inc. filed a Response (Paper 16, "PO Resp."), and Petitioner filed a Reply to Patent Owner's Response (Paper 28, "Pet. Reply"). Patent Owner then filed a Sur-reply to Petitioner's Reply. Paper 29 ("Sur-reply"). An oral hearing was held before the Board. Paper 32 ("Tr.").

We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Having considered the record before us, and as explained below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–8 of the '743 patent are unpatentable. *See* 35 U.S.C. § 316(e).

A. RELATED PROCEEDINGS

The parties assert the '743 patent is involved in *North Star Innovations, Inc. v. Micron Technology, Inc.*, 17-cv-506-LPS-CJB (D. Del.). *See* Pet. 2; Paper 4, 1.

B. THE '743 PATENT

The '743 patent relates to ball-grid array (BGA) packaging. Ex. 1001, at [57]. Figure 2 of the '743 patent is reproduced below.

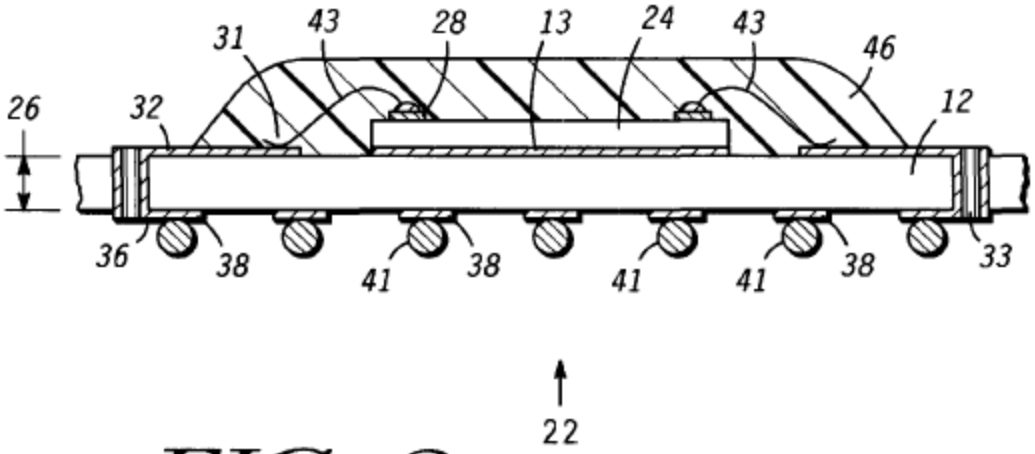

FIG. 2

Figure 2 "illustrates an enlarged cross-sectional view of one BGA structure, assembly, or package 22 after assembly but before singulation or separation into individual packages." *Id.* at 3:31–33. The specification describes Figure 2 as follows:

> BGA structure 22 comprises one of BGA substrates 12 within PCB [printed circuit board] 11. . . .
>
> BGA structure 22 further includes a semiconductor die 24 attached die attach pad 13 on an upper surface of each of BGA substrates 12. Semiconductor die 24 has a plurality of bonding or bond pads 28. Each of BGA substrates 12 has a conductive connective structure comprising bond posts 31, upper conductive traces 32, vias 33, lower conductive traces 36 and contact pads 38. Conductive solder balls 41 are attached to contact pads 38. Conductive wires or wire bonds 43 electrically couple bond pads 28 to bond posts 31. . . . An encapsulating layer or encapsulant 46 covers semiconductor die 24 and wire bonds 43 to provide protection of active circuit elements from physical damage and/or corrosion.

Id. at 3:34–62.

In particular, the '743 patent focuses on manufacturing conventional BGAs as described above using an N by M array (i.e., a single substrate that

is N packages long and M packages wide), with N and M each greater than or equal to 2. *See id*. at [57].

C. ILLUSTRATIVE CLAIM

Of the challenged claims, only claim 1 is independent. Independent claim 1 is illustrative of the claimed subject matter and is reproduced below.

> 1. A method for assembling ball-grid array (BGA) packages, comprising the steps of:
>
> providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board having a thickness, wherein N and M are greater than or equal to 2, each of the plurality of BGA substrates having a plurality of bond posts on one side and a plurality of contact pads on an opposite side;
>
> attaching a semiconductor die to each of the plurality of BGA substrates, the semiconductor die having a plurality of bond pads;
>
> encapsulating the semiconductor die with an encapsulant;
>
> curing the encapsulant;
>
> attaching conductive solder balls to each of the plurality of contact pads; and
>
> dividing the N by M array into separate BGA packages, and wherein each of the separate BGA packages is substantially planar.

Id. at 5:9–27.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 4–6.

Claims Challenged	35 U.S.C. §	Reference(s)
1 and 8	103(a)	Pastore[1], Altman[2], and Variot[3]
2	103(a)	Pastore, Altman, Variot, and Engelmaier[4]
3	103(a)	Pastore, Altman, Variot, and Freyman[5]
4	103(a)	Pastore, Altman, Variot, and Lau[6]
5 and 6	103(a)	Pastore, Altman, Variot, and JEDEC Standard[7]
7	103(a)	Pastore, Altman, Variot, and Spanjer[8]
1, 5, 6, and 8	103(a)	Houghten[9], Altman, and JEDEC Standard
2	103(a)	Houghten, Altman, JEDEC Standard, and Engelmaier
3	103(a)	Houghten, Altman, JEDEC Standard, and Freyman
4	103(a)	Houghten, Altman, JEDEC Standard, and Lau
7	103(a)	Houghten, Altman, JEDEC Standard, and Spanjer

[1] U.S. Patent No. 5,285,352 (issued Feb. 8, 1994) (Ex. 1005, "Pastore").
[2] PCT Pub. No. WO 90/07792 (pub. July 12, 1990) (Ex. 1006, "Altman").
[3] U.S. Patent No. 5,435,482 (issued July 25, 1995) (Ex. 1007, "Variot").
[4] Werner Engelmaier, "Thermo-Mechanical Effects" in Electronic Materials Handbook, Vol. 1 (1989) (Ex. 1008, "Engelmaier").
[5] U.S. Patent No. 5,635,671 (issued June 3, 1997) (Ex. 1010, "Freyman").
[6] J. Lau et al., "No Clean Mass Reflow of Large Over Molded Plastic Pad Array Carrier (OMPAC)," Proceedings of IEEE IEMT (1993) (Ex. 1011 "Lau").
[7] JEDEC Standard No. MO-151A, "SPXGA-X/PBGA Plastic Ball Grid Array Family Registration," (Nov. 1993) (Ex. 1013, "JEDEC Standard").
[8] U.S. Patent No. 4,753,863 (issued June 28, 1988) (Ex. 1015, "Spanjer").
[9] Julie Houghten, "New Package Takes on QFPs," Advanced Packaging,

II. ANALYSIS

A. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner asserts that a person of ordinary skill in the art at the time of the '743 patent "would have had at least a Bachelor of Science degree in electrical engineering, chemistry, physics, or other equivalent scientific or engineering areas, along with at least 4-5 years of experience in the field of semiconductor packaging and assembly." Pet. 18–19. In addition, according to Petitioner, "[a]n individual with an advanced degree in a relevant field would require less experience in the field of semiconductor packaging and assembly." *Id.* (citing Ex. 1003 ¶¶ 26–30). Patent Owner does not provide its own formulation of a person of ordinary skill or contest Petitioner's assertion. PO Resp. 32. We agree with and adopt Petitioner's proposal because it is consistent with the '743 patent, as well as the problems and solutions in the prior art of record. *See Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

B. CLAIM CONSTRUCTION

Neither party proposes that we construe any claim terms. *See* Pet. 18; PO Resp. 32. We conclude no express claim construction is necessary. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.").

C. ASSERTED PRIOR ART

1. Pastore (Ex. 1005)

Pastore discloses a "pad array semiconductor device." Ex. 1005, at [57]. Pastore's Figure 1 is reproduced below.

Volume 2, No. 1 (1993) (Ex. 1016, "Houghten").

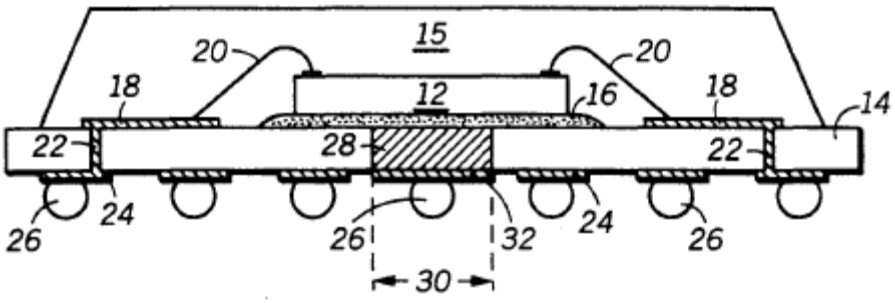

FIG.1

Figure 1 "illustrates, in a cross-sectional view, a semiconductor device 10." *Id*. at 3:59–60. Pastore describes Figure 1 as follows:

> Device 10 includes a semiconductor die 12 mounted to circuitized substrate 14 within a die receiving area of a top surface of the substrate. The die and portions of the substrate are encapsulated in a conventional epoxy resin package body 15 . . . . In most instances die 12 will be a[n] integrated circuit (IC), such as a microprocessor or memory . . . .
>
> . . . To accomplish signal routing, substrate 14 includes a plurality of conductive traces 18 on its top surface. . . . Semiconductor die 12 is electrically coupled to conductive traces 18 by conventional wire bonds 20, or by other known coupling methods such as tape-automated-bonding (TAB), flip-chip bonding, direct-chip-attach, or the like. Also to enable signal routing, circuitized substrate 14 includes a plurality of conductive vias 22. Conductive vias 22 extend through substrate 14 and electrically couple conductive traces on the top surface of the substrate to those on the bottom. . . . At an end portion of each conductive trace on the bottom of circuitized substrate is an integral conductive pad 24 for receiving a solder ball 26. Solder balls 26 are terminals of device 10 which permit external electrical accessibility to semiconductor die 12.

Id. at 3:61–4:30.

2. Altman (Ex. 1006)

Altman discloses manufacturing pad grid arrays using a 3x6 matrix to create multiple individual pad grid array devices from a single substrate. Ex. 1006, 4:2–5.

3. Variot (Ex. 1007)

Variot discloses techniques for maintaining coplanarity of solder balls on plastic BGAs. Ex. 1007, at [54], [57].

4. Engelmaier (Ex. 1008)

Engelmaier discloses that mismatched thermal expansion of semiconductor components and substrates strains the materials and solder joints in semiconductor packages, causing reliability problems. Ex. 1008, 3. To address this issue, Engelmaier discloses "tailoring" the coefficients of thermal expansion ("CTE") of the substrate and components "by deliberate design or material choice," such that the CTEs are similar or overlapping, to reduce the total strain from thermal expansion. *Id.*

5. Freyman (Ex. 1010)

Freyman teaches using stress-relief slots on strips of BGA substrates to reduce stress-induced warping during processing. Ex. 1010, 7:12–17.

6. Lau (Ex. 1011)

Lau discloses Over Molded Plastic Pad Grid Array Carrier (OMPAC) packages with substrate thicknesses ranging from 0.1–0.6 mm and 0.8–1.0 mm. Ex. 1011, 2.

7. JEDEC Standard (Ex. 1013)

JEDEC Standard is an industry standard for plastic BGAs. It sets maximums for deviations from coplanarity in plastic BGAs, Ex. 1013, 5, as well as the permissible body sizes (i.e., length and width) for plastic BGAs, Ex. 1013, 2.

8. Spanjer (Ex. 1015)

Spanjer discloses an additive for "common plastic encapsulants" for electronic devices that causes the encapsulant to change colors when exposed to a laser, which allows for marking the encapsulant. Ex. 1015, at [57], Figs. 2, 3.

9. Houghten (Ex. 1016)

Houghten discloses an OMPAC. Ex. 1016, 39. Houghten's Figure 2 is reproduced below.

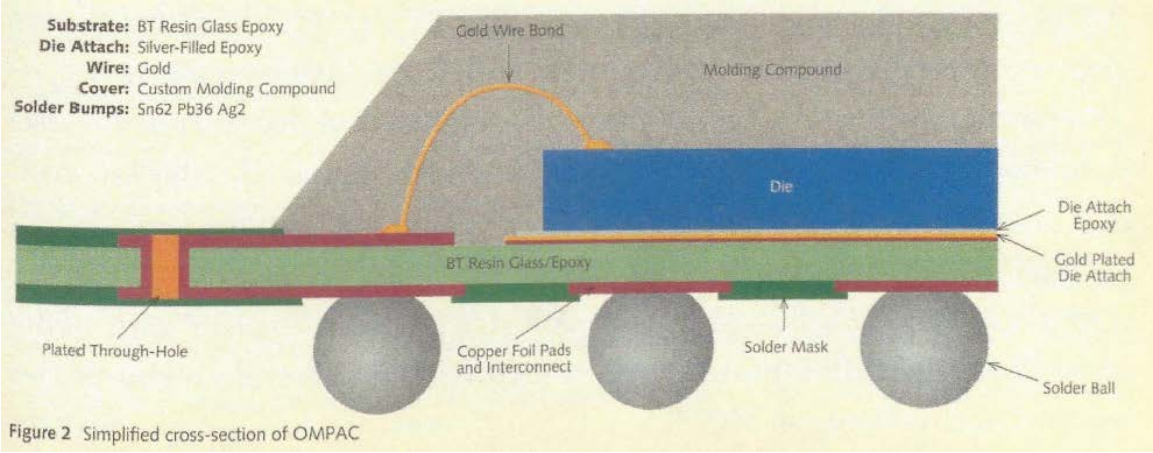

Figure 2 is a "[s]implified cross-section of OMPAC." *Id.*

D. Obviousness Analysis

In its first set of asserted grounds, Petitioner contends claims 1–8 would have been obvious over Pastore, Altman, Variot, and other secondary references, along with an ordinarily skilled artisan's knowledge. Pet. 28–57. For these grounds, Petitioner generally reads claim 1's method for assembling BGA packages onto Pastore's assembly method for pad array devices with solder balls on the bottom of a substrate. *Id.* at 28–41. Petitioner relies on Altman for teaching claim 1's N by M array of pad grid arrays on a single substrate, where N and M are greater than or equal to 2. *Id.* at 30. Petitioner asserts that an ordinarily skilled artisan would have been

motivated to manufacture Pastore's BGAs using Altman's N by M array teaching because it was known that manufacturing BGAs using N by M arrays was more cost-effective. *Id.* at 38. Petitioner further relies on Variot for teaching claim 1's substantially planar limitation. *Id.* at 35. Petitioner asserts that an ordinarily skilled artisan would have combined Variot's substantially planar teaching with Pastore and Altman because keeping coplanarity deviation low (i.e., below 0.006 inches) maintains reliable electrical connectivity and is necessary to comply with industry standards. *Id.* at 39.

In its second set of asserted grounds, Petitioner contends claims 1–8 would have been obvious over Houghten, Altman, JEDEC Standard, and other secondary references, along with an ordinarily skilled artisan's knowledge. *Id.* at 57–89. For these asserted grounds, Petitioner replaces Pastore and Variot with Houghten and JEDEC Standard. Petitioner explains that it includes these grounds because, whereas Pastore and Variot are prior art under §§ 102(a) and (e), Houghten and JEDEC Standard are prior art under § 102(b) and therefore cannot be antedated. *Id*. at 7.

For the reasons explained below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–8 of the '743 patent are unpatentable based on both sets of asserted grounds.

1. Obviousness of Claims 1 and 8 Based on Pastore, Altman, and Variot and of Claim 2 Based on Pastore, Altman, Variot, and Engelmaier

a. Disputed N by M Array Limitation in Claim 1

Claim 1 recites "providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board . . . wherein N and M are greater than or equal to 2." Petitioner relies on Altman for its disclosure of

"manufacturing a 3x6 (*i.e.*, NxM, with N=3 and M=6) matrix of pad grid arrays on a single substrate" as corresponding to claim 1's N by M array limitation. *Id.* at 30. Petitioner explains, with support from its expert, Dr. Philip Garrou, and the prior art, that an ordinarily skilled artisan "would have been motivated to manufacture Pastore's BGAs using Altman's array teachings because it was known that manufacturing BGAs using NxM arrays was more cost-effective." *Id.* at 38. As Petitioner notes, "this cost reduction resulted from not having to calibrate and align the tooling used in the process as frequently, because the tooling had to be realigned each time a new substrate was placed for processing." *Id*. Further, "[b]y fabricating multiple packages on a single large substrate, the substrate needed to be swapped less frequently, resulting in fewer realignments." *Id*. We agree with Petitioner that Altman teaches the recited "N by M array . . . wherein N and M are greater than or equal to 2" feature. In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of Pastore's pad array device assembly method with Altman's N by M array would have been obvious to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Patent Owner does not dispute that Altman teaches claim 1's N by M array. Instead, Patent Owner contends that it would not have been obvious to modify Pastore in view of Altman to achieve the N by M array limitation. PO Resp. 32–40. According to Patent Owner, Altman's N by M array teachings are limited to ceramic BGAs and are inapplicable to Pastore's plastic BGAs. *Id*. at 39–40. Specifically, Patent Owner contends that it would not have been obvious to combine Pastore with Altman "to make

Pastore's . . . OMPACs in the matrix array disclosed by Altman in light of the unique challenges of plastic material warpage in this technology at the time of the invention of the '743 patent." *Id.* at 39. According to Patent Owner, a skilled artisan "would not have had a reasonable expectation of success in making the ceramic NxM substrate disclosed by Altman out of plastic due to the significant warpage concerns of using plastic." *Id*. at 40. We disagree with Patent Owner's argument.

While Patent Owner's argument (using plastic introduces warpage concerns) might undermine applying Pastore's teaching of using plastic substrates to Altman's BGA N by M array, it does not undermine Petitioner's actual proposed modification, which is applying Altman's N by M array configuration to Pastore's plastic BGAs. *See* Pet. 30–31, 38. That is, even if Patent Owner is correct that using plastic introduced "significant warpage concerns," PO Resp. 40, Patent Owner's argument is inapposite to Petitioner's assertion that cost reduction would have motivated a skilled artisan to apply Altman's N by M array configuration to Pastore's plastic BGAs.

b. Disputed Planarity Limitations in Claims 1 and 2

Claim 1 recites "wherein each of the separate BGA packages is substantially planar." Petitioner relies on Variot's teaching that "nonplanarity beyond 0.006 inches in plastic BGAs could decrease electrical reliability" as corresponding to claim 1's "substantially planar" limitation. Pet. 35. Claim 2 further requires "wherein size of the N by M array and the thickness are such that each of the plurality of BGA substrates maintains a planarity variation less than approximately 0.15 mm after assembly." Petitioner notes that Variot teaches "each substrate having non-planarity no

greater than 0.006 inches after assembly," and "0.006 inches is approximately 0.15mm." *Id*. at 42. Petitioner also explains, again with support from its expert and the prior art, that a skilled artisan would have combined Variot's substantially planar and variation less than approximately 0.15 mm teaching with Pastore and Altman "to achieve the benefits of keeping coplanarity deviation below 0.006in, such as maintaining reliable electrical connectivity, especially given Pastore's discussions of the importance of planarity." *Id.* at 39. In addition, "because Variot discloses that 0.006in was the limit specified in JEDEC Standard, a POSA would further have been motivated to meet this limit to comply with industry standards and ensure compatibility with other industry-standard products." *Id*. We agree with Petitioner that Variot teaches the recited "substantially planar" limitation of claim 1. We also agree with Petitioner that Variot discloses claim 2's "planarity variation less than approximately 0.15 mm." In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

Patent Owner argues that Variot does not teach claim 1's "substantially planar" limitation or claim 2's "planarity variation less than approximately 0.15 mm" because Variot could allow for exactly 0.006 inches coplanarity. *See* PO Resp. 42–43.

Even if we equate claim 1's "substantially planar" limitation with claim 2's more stringent "planarity variation less than approximately 0.15 mm," as Patent Owner does, we agree with Petitioner that Variot teaches the required planarity. First, Variot teaches that a 0.006 inch coplanarity value

"statistically decreases the reliability of the electrical connections" and is therefore "at the limit of what can be tolerated." Ex. 1007, 3:3–11; *see also id*. at 3:15–16 (explaining that JEDEC has proposed an industry standard that "calls for a non-planarity of no more than 0.006 inches"). As Petitioner explains, and we agree, "[b]ecause 'approximately 0.15 mm' could be 0.16mm or another amount close to but somewhat more than 0.15mm, no more than 0.006 inches (which is 0.153mm) is 'less than approximately 0.15 mm.'" Pet. Reply 11 (citing Ex. 1041 ¶¶ 42–44).

c. Reasonable Expectation of Success in Achieving the Planarity Limitations in Claims 1 and 2

Patent Owner also asserts that "a POSA would not have had a reasonable expectation of success in achieving the planarity limitations claimed by the '743 patent." PO Resp. 47. In particular, Patent Owner asserts that the 0.15 mm coplanarity standard referenced in the prior art "never rose above being aspirational" and does not give rise to a reasonable expectation of success in achieving 0.15 mm coplanarity. *Id*. at 46, 51. Patent Owner notes that the document that recited 0.15 mm coplanarity "was merely a JEDEC 'Registered Outline' and was *never* adopted as a JEDEC industry-wide standard." *Id*. at 48. Patent Owner explains that when JEDEC Standard "was modified and ultimately elevated to standard status, the proposed 0.15 mm coplanarity dimension had been abandoned" in favor of a more relaxed 0.20 mm standard. *Id*. at 49–50. Patent Owner contends further that there was "significant concern as to whether 0.15mm coplanarity could be achieved," and cites as evidence several statements from industry stakeholders questioning the feasibility of a 0.15 mm standard. *Id*. at 51–53 (citing Ex. 1014, 191; Ex. 1034, 36; Ex. 1024, 1).

Even if we once again equate claim 1's "substantially planar" limitation with claim 2's more stringent "planarity variation less than approximately 0.15 mm," as Patent Owner does, we agree with Petitioner that one skilled in the art would have had a reasonable expectation of success in achieving planarity variation less than approximately 0.15 mm. First, adoption of the JEDEC Standard's coplanarity requires "wide acceptance in the electronics industry," Ex. 2008 ¶ 9, which is more demanding than a mere reasonable expectation of success. It appears that economic concerns irrelevant to whether a skilled artisan could reasonably have expected to successfully make the proposed combination impacted whether 0.15 mm coplanarity was ultimately adopted as the industry standard. *See* Ex. 1014, 191 (stating that "[w]hile the 0.15mm coplanarity will ultimately be achieved LSI Logic is concerned that this effort will add cost without value to each [plastic ball grid array (PBGA)] package"); Ex. 1041 ¶¶ 77–79 (explaining that hesitancy in adopting a 0.15 mm coplanarity standard related to potentially imposing unneeded extra costs on commercial BGA manufacturers). On the other hand, Registered Outlines (like JEDEC Standard) "reflect products with anticipated usage in the electronics industry," Ex. 2008 ¶ 9, and thus better reflect a reasonable expectation of success. *See* Ex. 1041 ¶ 75.

In addition, more telling than JEDEC standards is Petitioner's unrebutted evidence of testing data showing that the vast majority of a manufacture's tested BGA packages met and even surpassed 0.15 mm coplanarity during the relevant timeframe. *See* Pet. Reply 12–13. In particular, as Petitioner explains:

> In 1993, Citizen Watch published an article reporting testing results relating to "plastic BGA coplanarity." (Ex. 1024, Shimizu

> at 1.) Twenty samples of three differently sized "BGA packages"—including 22x22mm, 27x27mm, and 35x35mm packages—were tested. (*Id.* at 2.) Package thicknesses of 0.2mm and 0.6mm were employed. (*Id.* at 4.) The article reports average coplanarity across the 20 packages of each size and the maximum measured coplanarity:

BGA Package		169L	225L	396L
Package Size (mm Square)		22.0	27.0	35.0
Coplanarity Value (um)	Max.	134.4	149.4	161.3
	SD.	12.0	10.5	10.4
	Ave.	118.8	126.9	142.5

Table 1: BGA Package (Package Size) vs Coplanarity Value

BGA Package		225L		396L	
Substrate Core Thickness (mm)		0.2	0.6	0.2	0.6
Coplanarity Value (um)	MAX.	149.4	120.1	161.3	122.3
	SD.	10.5	11.3	13.6	11.6
	Ave.	126.9	104.0	141.1	112.0

Table 3: Substrate Core Thickness vs Coplanarity Value

> (*Id.* at 4, 6.) This data shows that plastic BGAs can be successfully made with a coplanarity value less than approximately 150 μm (0.15mm). In fact, with the exception of the 0.2mm thick 35x35mm package, which still had an average coplanarity below 0.15mm, all the packages had maximum measured coplanarities below 0.15mm. This means that almost every plastic BGA package tested by Citizen was successfully made with a coplanarity value below the approximately 0.15mm value referenced by the '743 patent. (*See* Ex. 1041, Bravman Dec. ¶¶57-64.)

Pet. Reply 12–13. Although the testing data reflects only single packages' warpage, Petitioner presented further evidence that the "structural differences between an array of packages and a single package . . . do not have a significant bearing on the warpage and planarity of an array versus a single package." Ex. 1041 ¶ 70. Thus, a skilled artisan could reasonably have expected to achieve the same coplanarity values with arrays of BGAs

as with the tested BGAs. Moreover, we credit Dr. Bravman's testimony that a skilled artisan "would have been more than capable of optimizing package size, package thickness, and material CTE, and of incorporating slots into the substrate array, to achieve a desired level of coplanarity, including a coplanarity less than about 0.15mm." *Id*. ¶ 55. Given the record evidence, we agree with Petitioner that a skilled artisan would have had a reasonable expectation of success in achieving the planarity limitations of claims 1 and 2.

d. Matching Thermal Coefficients of Expansion Limitation in Claim 2

Claim 2 depends from claim 1 and recites "wherein the step of encapsulating the semiconductor die includes encapsulating with an encapsulant having a thermal coefficient of expansion close to that of the semiconductor die and the printed circuit board." Petitioner explains that Engelmaier discloses this limitation because it teaches "tailoring (*i.e.*, matching) the CTE of package 'substrate and/or components' to reduce mismatched thermal expansion." Pet. 41 (citing Ex. 1008, 3). Further, Petitioner explains, a skilled artisan would have been motivated to use Engelmaier's CTE tailoring when manufacturing Pastore's BGA using Altman's matrix approach "to avoid expansion stresses." *Id.* at 42. We agree with Petitioner that Engelmaier teaches the required CTE-matching limitation. In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

Patent Owner asserts Engelmaier does not disclose this limitation because "Engelmaier discloses matching the CTE of the entire . . . SMT

[(surface mount)] package to the PWB [(printed wiring board)]," rather than "matching the CTE of the package components, *i.e.*, the semiconductor die, the package substrate and the encapsulant," as claim 2 requires. PO Resp. 57. We disagree with Patent Owner's argument.

"A person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421. Further, "we do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art." *In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007). As Petitioner notes, Engelmaier discloses that using CTE matched materials reduces the well-known problem of "strains" in electronic components. Ex. 1008, 3; *see* Ex. 1023, 1; Ex. 1024, 1. Patent Owner recognizes that "the purpose of Engelmaier is to use CTE tailoring in order to minimize the stress between the package and the PWB." PO Resp. 57. Although, as Patent Owner notes, Engelmaier employs CTE matching to protect the solder joints connecting a package to a wiring board, we agree with Petitioner that a skilled artisan would have been able to and would have had reason to apply Engelmaier's general CTE-matching concept to the components within the package itself. *See* Pet. Reply 22 (citing Ex. 1041 ¶¶ 87–88). In short, Petitioner's proposed combination amounts to little more than known methods (i.e., Engelmaier's CTE matching) applied to familiar elements (i.e., Pastore's and Houghten's BGA assembly components) to yield the predictable result of reducing strain on those components. *See KSR*, 550 U.S. at 401. Thus, we agree with Petitioner that Engelmaier, in combination with the other asserted references, teaches "wherein the step of encapsulating the semiconductor die includes encapsulating with an encapsulant having a thermal coefficient of expansion

close to that of the semiconductor die and the printed circuit board," as claim 2 requires.

e. Remaining Undisputed Limitations in Claims 1 and 8

Relying on Pastore's Figure 1, Petitioner asserts that Pastore's packages include a "plurality of bond posts," a "plurality of contact pads," "semiconductor dies," "bond pads," an "encapsulant," and "conductive solder balls," as recited in claim 1. Pet. 28–34. Patent Owner does not dispute these teachings. We agree with Petitioner that Pastore discloses a "plurality of bond posts," a "plurality of contact pads," "semiconductor dies," "bond pads," an "encapsulant," and "conductive solder balls."

Claim 8 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board comprises of an organic resin." Petitioner explains that Pastore discloses this limitation because it teaches using bismaleimide triazine (BT), epoxy, polyimide, triazine, or phenolic resins for the printed circuit board. *Id*. at 36. Petitioner notes that "[t]hese resins are organic resins, because they are based on carbon chains or rings with hydrogen, oxygen, nitrogen, and other elements." *Id.* at 36–37. Patent Owner does not dispute these teachings. We agree with Petitioner that Pastore discloses the "organic resin" limitation recited in claim 8.

2. Obviousness of Claim 3 Based on Pastore, Altman, Variot, and Freyman

Claim 3 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a plurality of stress-relief slots at various locations within the printed circuit board."

Petitioner contends claim 3 would have been obvious over Pastore, Altman, Variot, and Freyman in view of a skilled artisan's knowledge. *Id.* at 44–45. Specifically, Petitioner explains, with support from its expert and the prior art, that Freyman discloses providing stress-relief slots on a printed circuit board substrate for BGAs to prevent warping. *Id.* at 44. Further, Petitioner explains, a skilled artisan "would have been motivated to use Freyman's stress-relief slots to reduce coplanarity deviations, which decrease electrical reliability in BGAs." *Id.* at 45. Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that Freyman teaches the recited "a plurality of stress-relief slots" limitation. In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

3. Obviousness of Claim 4 Based on Pastore, Altman, Variot, and Lau

Claim 4 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a thickness in a range from approximately 0.5 mm to approximately 0.8 mm." Petitioner contends claim 4 would have been obvious over Pastore, Altman, Variot, and Lau in view of a skilled artisan's knowledge. Pet. 46–47. Specifically, Petitioner explains that Lau teaches the claimed circuit board thickness range because "Lau specifically discloses OMPAC BGAs with 0.8mm thick substrates, which are within the range of 0.5-0.8mm." *Id.* at 46. Petitioner further explains, with support from its expert and the prior art, that a skilled artisan would have been motivated to use Lau's 0.8mm

substrates "to reduce coplanarity deviations, which decrease electrical reliability in BGAs" because "it was known that using thicker substrates could prevent coplanarity deviations." *Id*. Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that Lau teaches the recited circuit board thickness range. In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

4. Obviousness of Claims 5 and 6 Based on Pastore, Altman, Variot, and JEDEC Standard

Claim 5 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a width on an order of 63 mm." Claim 6 also depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a length in a range from approximately 187 mm to 212 mm." Petitioner contends claims 5 and 6 would have been obvious over Pastore, Altman, Variot, and JEDEC Standard in view of a skilled artisan's knowledge. Pet. 48–55.

Petitioner explains that "JEDEC Standard discloses the permissible body sizes (*i.e.*, length/width) in millimeters for plastic BGAs." *Id.* at 48. In particular, Petitioner references JEDEC Standard's Table 5, which includes a BGA body size of 21 mm in length and width. *Id*. at 50. Petitioner explains that "[m]anufacturing 21.00mm body size BGAs, as specified in JEDEC Standard, using Altman's 3x6 matrix approach uses a

63.00mm wide substrate" as recited in claim 5 "because 21.00mm wide BGAs arranged 3-wide is 63.00mm." *Id.* at 50–51. As for claim 6, Table 5 also includes a BGA body size of 33 mm in length and width and, as Petitioner explains, "[m]anufacturing 33.00mm body size BGAs, as specified in JEDEC Standard, using Altman's 3x6 matrix approach uses a 198.00mm long substrate because 33.00mm wide BGAs arranged 6-long is 198.00mm" *Id.* at 52. Further, as Petitioner notes, 198.00mm is within the 187mm to 212mm range recited in claim 6. *Id.* Patent Owner does not dispute these teachings.

In addition, Petitioner explains that a skilled artisan would have been motivated to implement JEDEC Standard's teachings related to BGA body size "because Variot's disclosure of JEDEC Standard would have provided an express motivation to refer to JEDEC Standard." *Id.* at 52. A skilled artisan "investigating BGAs would thus have looked to JEDEC Standard to ensure compliance with the industry standard and compatibility with other industry-standard products," and "[t]his would have included complying with the permissible body and ball grid matrix sizes identified in JEDEC Standard's Table 5." *Id.* at 53. Thus, Petitioner explains,

> [a] POSA using Altman's process to manufacture JEDEC Standard-compliant BGAs would have recognized that selecting a particular BGA body size, and thus the width of the substrate for Altman's 3x6 array, was a matter of selecting from a finite number of identified, predictable body size choices – specifically, the 21 sizes between 7.00mm and 50.00mm specified in JEDEC Standard.

Id. Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that JEDEC Standard's BGA body length and width teachings, combined with Altman's 3x6 array, disclose the width

limitation recited in claim 5 (i.e., "having a width on an order of 63 mm.") and length limitation recited in claim 6 (i.e., "having a length in a range from approximately 187 mm to 212 mm"). In addition, we agree with Petitioner that selecting a particular body size from JEDEC Standard's Table 5 would have been obvious as one of a finite number of identified, predictable solutions. *See KSR*, 550 U.S. at 402 (explaining that "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp").

5. Obviousness of Claim 7 Based on Pastore, Altman, Variot, and Spanjer

Claim 7 depends from claim 1 and recites "bonding conductive wires to the plurality of bond pads and the plurality of bond posts after the step of attaching the semiconductor die." Claim 7 further recites "marking the BGA packages after the step of encapsulating the semiconductor die." Petitioner contends claim 7 would have been obvious over Pastore, Altman, Variot, and Spanjer in view of a skilled artisan's knowledge. Pet. 55–57. Petitioner explains that Pastore discloses the claimed bonding feature because it teaches "wire bonds 20 (*i.e.*, conductive wires) that electrically couple the semiconductor die to conductive traces 18 (*i.e.*, bond posts) after the die is mounted," and "the wire bonds attach to the semiconductor die at the bond pads." *Id.* at 55. Patent Owner does not dispute these teachings. We agree with Petitioner that Pastore teaches the recited "bonding conductive wires to the plurality of bond pads and the plurality of bond posts after the step of attaching the semiconductor die."

Petitioner also explains that Spanjer teaches claim 7's marking step because it "discloses an additive for 'common plastic encapsulants' that

causes the encapsulant to change colors when exposed to a laser." *Id.* at 56 (citing Ex. 1015, Abstract, Figs. 2, 3, 6:43–53). This, Petitioner notes, "allows for marking the encapsulant with part numbers, identifiers, or other desired marks." *Id.* Petitioner explains further, with support from the prior art and its expert, that one skilled in the art would have been motivated to combine Pastore, Altman, Variot, and Spanjer to manufacture Pastore's BGAs, using Altman's 3x6 matrix approach, with Spanjer's encapsulant additive, to lasermark the packages—a common practice in the industry to visually identify completed packages. *Id.* at 56–57. Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that Spanjer teaches the recited "marking the BGA packages after the step of encapsulating the semiconductor die." In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

6. Obviousness of Claims 1–8 Based on Houghten, JEDEC Standard, and Other References

Petitioner contends claims 1–8 would have been obvious over Houghten, JEDEC Standard, and other secondary references, along with a skilled artisan's knowledge. Pet. 57–89. For these asserted grounds, Petitioner replaces Pastore's and Variot's teachings discussed above with Houghten's and JEDEC Standard's teachings.

a. Claims 1 and 2

Petitioner contends that claim 1 would have been obvious over Houghten, Altman, and JEDEC Standard, and claim 2 would have been obvious over Houghten, Altman, JEDEC Standard, and Engelmaier. *Id.* at 57–68, 80–82. Except for two claim elements, Petitioner generally reads

claim 1's method for assembling BGA packages onto Houghten's method of assembling Motorola's OMPAC BGAs by attaching an integrated circuit die to a printed circuit board substrate, wire bonding the die to conductive traces in the substrate, and connecting the traces to a solder ball array on the bottom of the substrate. *See id*. at 57–68. Relying on Houghten's Figure 2, Petitioner notes that Houghten's packages include a "plurality of bond posts," a "plurality of contact pads," "semiconductor dies," "bond pads," an "encapsulant," and "conductive solder balls," as recited in claim 1. *Id*. Patent Owner does not dispute these teachings. We agree with Petitioner that Houghten discloses these elements.

For claim 1's limitation reciting "providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board . . . wherein N and M are greater than or equal to 2," Petitioner relies on the same teaching (i.e., Altman's 3x6 matrix of pad grid arrays) and the same rationale for combining that teaching (i.e., cost reduction) as it did for its challenge based on Pastore. *See id.* at 60–61, 73–75. Patent Owner raises the same challenges noted above—i.e., that it would not have been obvious to modify Houghten in view of Altman to achieve the N by M array limitation because Altman's array teachings are limited to ceramic BGAs and are inapplicable to Houghten's plastic BGAs. *See* PO. Resp. 32–40. We disagree with Patent Owner's argument for the reasons explained above. We agree with Petitioner that Altman teaches the recited "N by M array . . . wherein N and M are greater than or equal to 2" feature and that Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings

would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

For the planarity limitations—i.e. claim 1's "substantially planar" and claim 2's "planarity variation less than approximately 0.15 mm"—Petitioner relies on JEDEC Standard's teaching that the maximum allowable coplanarity deviation for plastic BGAs is 0.15 mm. Pet. 66. Patent Owner does not contest these teachings, and we agree with Petitioner that JEDEC Standard teaches the recited "substantially planar" and "planarity variation less than approximately 0.15 mm" limitations. Petitioner further explains, again with support from its expert and the prior art, that a skilled artisan would have been motivated to combine JEDEC Standard's substantially planar teaching with Houghten/Altman to achieve the known benefit of maintaining reliable electrical connectivity, and to comply with the industry standard and ensure compatibility with other industry-standard products. *Id.* at 75. In light of its assertions, we find Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

Patent Owner raises the same combinability argument explained above—that a skilled artisan would not have had a reasonable expectation of success in achieving the planarity limitations because the 0.15 mm coplanarity standard was ultimately not adopted as the industry-wide standard. *See* PO. Resp. 47–54. We disagree with Patent Owner's argument for the reasons explained above. Instead, for the reasons explained above, we agree with Petitioner that a skilled artisan would have had a reasonable

expectation of success in achieving the planarity limitations in claims 1 and 2.

Claim 2 depends from claim 1 and recites "wherein the step of encapsulating the semiconductor die includes encapsulating with an encapsulant having a thermal coefficient of expansion close to that of the semiconductor die and the printed circuit board." Petitioner explains that Engelmaier discloses this limitation because it teaches "tailoring (*i.e.*, matching) the CTE of package 'substrate and/or components' to reduce mismatched thermal expansion." Pet. 80 (citing Ex. 1008, 3). Further, Petitioner explains, a skilled artisan would have been motivated to use Engelmaier's CTE tailoring when manufacturing Houghten's BGA using Altman's matrix approach "to avoid expansion stresses." *Id.* We agree with Petitioner that Engelmaier teaches the required CTE-matching limitation. In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

Patent Owner raises the same argument contesting Engelmaier's teaching explained above—that Engelmaier discloses CTE matching between the SMT package and the PWB, rather than between package components, as claim 2 requires. *See* PO Resp. 57. We disagree with Patent Owner's argument for the reasons explained above.

b. Claim 3

Claim 3 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a plurality

of stress-relief slots at various locations within the printed circuit board." Petitioner contends claim 3 would have been obvious over Houghten, Altman, JEDEC Standard, and Freyman in view of a skilled artisan's knowledge. Pet. 82–84. Petitioner's assertions regarding Freyman's teachings and its reason to combine those teachings with Houghten, Altman, and JEDEC Standard parallel its assertions for the grounds involving Pastore's teachings discussed above. *See id*. Patent Owner does not dispute Petitioner's assertions in these regards. As explained above, we agree with Petitioner that Freyman teaches the recited "a plurality of stress-relief slots" limitation. In addition, for the reasons explained above, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

c. Claim 4

Claim 4 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a thickness in a range from approximately 0.5 mm to approximately 0.8 mm." Petitioner contends that claim 4 would have been obvious over Houghten, Altman, JEDEC Standard, and Lau in view of a skilled artisan's knowledge. Pet. 84–86. Petitioner's assertions regarding Lau's teachings and its reason to combine those teachings with Houghten, Altman, and JEDEC Standard parallel its assertions for the grounds involving Pastore's teachings discussed above. *See id*. Patent Owner does not dispute Petitioner's assertions in these regards. As explained above, we agree with Petitioner that Lau

teaches the recited circuit board thickness range. In addition, for the reasons explained above, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

d. Claims 5 and 6

Claim 5 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a width on an order of 63 mm." Claim 6 depends also from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board having a length in a range from approximately 187 mm to 212 mm." Petitioner contends claims 5 and 6 would have been obvious over Houghten, Altman, and JEDEC Standard in view of a skilled artisan's knowledge. Pet. 68–72. Petitioner's assertions regarding JEDEC's body-size teachings and its reason to combine those teachings with Houghten and Altman parallel its assertions for the grounds involving Pastore discussed above. *See id*. Patent Owner does not dispute Petitioner's assertions in these regards. As explained above, we agree with Petitioner that JEDEC teaches the recited circuit-board-size limitations recited in claims 5 and 6. In addition, for the reasons explained above, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

e. Claim 7

Claim 7 depends from claim 1 and recites "bonding conductive wires to the plurality of bond pads and the plurality of bond posts after the step of attaching the semiconductor die; and marking the BGA packages after the step of encapsulating the semiconductor die." Petitioner contends claim 7 would have been obvious over Houghten, Altman, JEDEC Standard, and Spanjer in view of a skilled artisan's knowledge. Pet. 86–89. Petitioner explains that Houghten discloses the claimed bonding feature because it teaches "making electrical connections to the IC using gold ball bonding after attaching the IC to the substrate." *Id*. at 86 (citing Ex. 1016, 1; Ex. 1003, K1–K2). Petitioner further explains that "gold ball bonding includes bonding a gold conductive wire to the bond pads on the IC die and to the copper traces (*i.e.*, plurality of bond posts) in the substrate," as illustrated in Houghten's Figure 2. *Id*. at 86–87 (citing Ex. 1016, 2). Patent Owner does not dispute these teachings. We agree with Petitioner that Houghten teaches the recited "bonding conductive wires to the plurality of bond pads and the plurality of bond posts after the step of attaching the semiconductor die."

Petitioner also explains that Spanjer teaches claim 7's marking step because it "discloses an additive for 'common plastic encapsulants' that causes the encapsulant to change colors when exposed to a laser." *Id.* at 87 (citing Ex. 1015, Abstract, Figs. 2, 3, 6:43–53). Petitioner's assertions regarding its reason to combine Spanjer's marking with Houghten, Altman, and JEDEC parallel its assertions for the grounds involving Pastore discussed above—i.e., to lasermark the packages and thereby visually identify completed packages. *Id*. at 88. Patent Owner does not dispute

Petitioner's assertions in these regards. We agree with Petitioner that Spanjer teaches the recited "marking the BGA packages after the step of encapsulating the semiconductor die." In addition, Petitioner has articulated persuasive reasoning with rational underpinning to support the legal conclusion that its proffered combination of prior-art teachings would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

f. Claim 8

Claim 8 depends from claim 1 and recites "wherein the step of providing the plurality of BGA substrates . . . includes providing the plurality of BGA substrates within a printed circuit board comprises of an organic resin." Petitioner contends claim 8 would have been obvious over Houghten, Altman, and JEDEC Standard in view of a skilled artisan's knowledge. Pet. 73–79. Specifically, Petitioner explains that Houghten discloses claim 8's organic-resin limitation because it discloses using bismaleimide triazine resin glass/epoxy PC board laminate for the substrate, which is an organic resin. *Id*. at 73. Patent Owner does not dispute these teachings. We agree with Petitioner that Houghten discloses the "organic resin" limitation recited in claim 8.

7. Secondary Considerations of Non-Obviousness

Patent Owner argues that certain objective evidence weighs in favor of non-obviousness. PO Resp. 58–64. Patent Owner alleges that "in spite of the widely-acknowledged desire to decrease the coplanarity value to as low as .15mm for PBGA packages, both to increase their reliability and to reduce cost while increasing manufacturing throughput, the evidence establishes that even the leaders of the manufacturing industry were unable to achieve that goal." *Id*. at 65. As support, Patent Owner points to certain published

test results from a PBGA manufacturer "[a]cknowledging that its own BGA does not satisfy coplanarity of 150μm." *Id*. at 62 (citing Ex. 1024, 6). Patent Owner also notes JEDEC's proposal, and subsequent failure to adopt the 0.15 mm planarity standard, as further "evidence that the industry was unable to achieve" 0.15 mm planarity. *Id*. at 63.

Having considered the evidence, we find there is at most a weak nexus between the claimed invention and Patent Owner's evidence, and therefore, we do not find Patent Owner's alleged objective evidence particularly persuasive of non-obviousness. As explained above, skepticism regarding what standard to adopt does not reflect skepticism at achieving the claimed invention. To the contrary, evidence Patent Owner cites as support actually suggests that 0.15 mm coplanarity would "ultimately be achieved," but that some in the industry were simply "concerned that this effort will add cost without value to each PBGA package." Ex. 1014, 191. In addition, we find persuasive the testimony from Petitioner's expert explaining that hesitancy in adopting a 0.15 mm coplanarity standard related not to the ability to achieve 0.15 mm coplanarity, but to potentially imposing unneeded extra costs on commercial BGA manufacturers. *See* Ex. 1041 ¶¶ 77–79. The test results Patent Owner cites likewise does not support non-obviousness. To the contrary, as explained above, other than one subset of tested chips, all the packages had maximum measured coplanarities below 0.15 mm. *See* Ex. 1024, 4, 6; Ex. 1041 ¶¶ 57–64. Although these test results were apparently "too high for large-scale commercial manufacturing," Ex. 1041 ¶ 64, they do not suggest general skepticism towards achieving 0.15 mm coplanarity for all BGAs.

Weighing Petitioner's evidence and arguments of obviousness against Patent Owner's evidence and arguments of nonobviousness, including alleged secondary considerations, we conclude Petitioner has shown by a preponderance of the evidence that claims 1–8 are unpatentable over the asserted prior art.

III. CONCLUSION

As indicated in the table below, Petitioner has shown by a preponderance of the evidence that claims 1–8 are unpatentable over the asserted prior art.[10]

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1 and 8	103(a)	Pastore, Altman, and Variot	1 and 8	
2	103(a)	Pastore, Altman, Variot, and Engelmaier	2	
3	103(a)	Pastore, Altman, Variot, and Freyman	3	

[10] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
4	103(a)	Pastore, Altman, Variot, and Lau	4	
5 and 6	103(a)	Pastore, Altman, Variot, and JEDEC Standard	5 and 6	
7	103(a)	Pastore, Altman, Variot, and Spanjer	7	
1, 5, 6, and 8	103(a)	Houghten, Altman, and JEDEC Standard	1, 5, 6, and 8	
2	103(a)	Houghten, Altman, JEDEC Standard, and Engelmaier	2	
3	103(a)	Houghten, Altman, JEDEC Standard, and Freyman	3	
4	103(a)	Houghten, Altman, JEDEC Standard, and Lau	4	

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
7	103(a)	Houghten, Altman, JEDEC Standard, and Spanjer	7	
Overall Outcome			1–8	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 1–8 of the ’743 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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