Trials@uspto.gov
Tel: 571-272-7822

Paper No. 24
Entered: January 14, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01566
Patent 6,388,330 B1

Before JON B. TORNQUIST, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

35 U.S.C. § 318 and 37 C.F.R. § 42.73

Micron Technology, Inc. ("Petitioner") challenges the patentability of claims 1, 2, 5–7, and 10 ("the challenged claims") of U.S. Patent No. 6,388,330 B1 (Ex. 1001, "the '330 patent"), assigned to Lone Star Silicon Innovations, LLC ("Patent Owner").[1]

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that the challenged claims of the '330 patent are unpatentable.

I. BACKGROUND

A. Procedural History

Petitioner filed a Petition seeking *inter partes* review. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). We instituted *inter partes* review of all challenged claims of the '330 patent. Paper 8 ("Institution Decision" or "Dec."). Patent Owner's Request for Rehearing (Paper 10) was denied. Paper 11 ("Rehearing Decision" or "Reh'g Dec.")

Patent Owner filed a Response. Paper 14 ("PO Resp."). Petitioner filed a Reply. Paper 16 ("Pet. Reply"). With the Board's prior authorization (Ex. 2014), Patent Owner filed a Sur-Reply addressing limited issues. Paper 17 ("PO Sur-Reply"). Pursuant to the same authorization, Petitioner filed a Sur-Sur-Reply. Paper 21 ("Pet. Sur-Sur-Reply").

[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 18, 1.

With the Petition, Petitioner filed a declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner cross-examined Dr. Fair and filed a transcript of his deposition testimony as Exhibit 2009 with the Patent Owner Response. With the Reply, Petitioner filed a second declaration of Dr. Fair. Ex. 1017.

With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2008. Petitioner cross-examined Dr. Bottoms and filed a transcript of his deposition testimony as Exhibit 1018 with Petitioner's Reply. With its Sur-Reply, Patent Owner filed a third declaration of Dr. Bottoms. Ex. 2015.

Oral argument was held October 11, 2018. A transcript of the oral argument was entered in the record. Paper 23 ("Tr.").

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following pending federal court proceedings involving the '330 patent: *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 18, 2–3. In addition, Patent Owner identifies Federal Circuit Appeal Nos. 2018-1580, 2018-1581, and 2018-1582, in which the defendant-appellees are Renesas Electronics Corp., Nanya Technology Corp., and United Microelectronics Corp., respectively. *Id.*

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following *inter partes* review proceedings involving the '330 patent: *Renesas Electronics Corp. v. Lone Star Silicon Innovations, LLC*, Case

IPR2017-01869 and *Nanya Technology Corp. v. Lone Star Silicon Innovations, LLC*, Case IPR2018-00062. Paper 18, 2.

C. The '330 Patent (Ex. 1001)

The '330 patent is titled "Low Dielectric Constant Etch Stop Layers in Integrated Circuit Interconnects" and was issued May 14, 2002, from Application No. 09/776,012, filed February 1, 2001. Ex. 1001 at (21), (22), (45), (54).

The '330 patent relates to semiconductor technology and, more specifically, to etch stop layers in integrated circuits. *Id.* at 1:6–8. According to the '330 patent, semiconductor devices fabricated in and on a semiconductor substrate may be interconnected using a "damascene" technique of metallization. *Id.* at 1:11–29. A "single damascene" technique forms a single layer of conductive interconnects, and a "dual damascene" technique forms multiple layers of conductive interconnects that are separated by interlayer dielectric layers, including etch stop layers, in vertically separated planes and interconnected by vertical connections or "vias." *Id.* at 1:30–34, 2:30–51. The '330 patent discloses that closely positioned, parallel conductive channels suffer from capacitive coupling effects, which can be reduced by reducing the dielectric constant of the silicon nitride etch stop layers between the channels. *Id.* at 3:32–42, 3:49–60. More specifically, the '330 patent represents that "currently used silicon nitride . . . has a dielectric constant in excess of 7.5" (*id.* at 3:39–41) and discloses that capacitive coupling effects are reduced by using an etch stop layer having a dielectric constant below 5.5 (*id.* at 3:53–54, 3:58–59).

Figure 2 of the '330 patent shows a "prior art" structure, and Figure 3 shows the invention. Ex. 1001, 4:14–20. Figures 2 and 3 of the '330 patent are reproduced below:

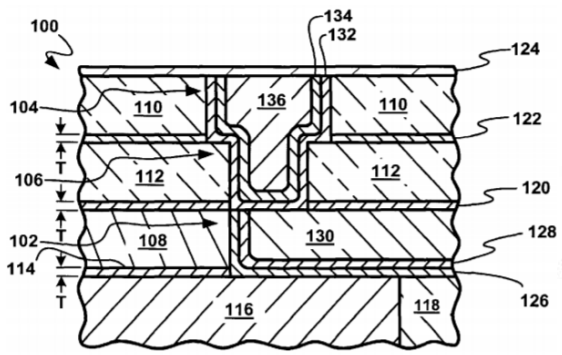


FIG. 2 (PRIOR ART)

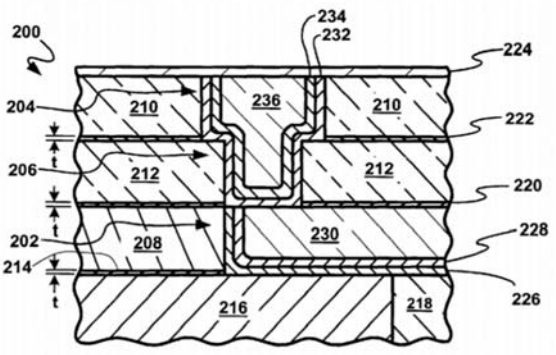


FIG. 3

Figures 2 and 3, above, show semiconductor wafers 100, 200, including dielectric layers 108, 110, 112, 208, 210, and 212; conductor cores 130, 136, 230, 236; and etch stop layers 114, 120, 122, 124, 214, 220, 222, and 224.[2] *Id.* at 4:24–32, 4:42–5:4, 5:21–53. According to the '330 patent, Figure 3 is "similar" to Figure 2, except for the thickness of the etch stop layers, which is shown as "T" in Figure 2 and "t" in Figure 3. *Id.* at 4:18, 5:17–23, 5:66–6:2.

Regarding the etch stop layers, the '330 patent discloses:

> In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.
>
> For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

[2] Structures with 100-series reference numerals are shown in Figure 2, and structures with 200-series reference numerals are shown in Figure 3.

Id. at 5:60–65. The '330 patent discloses processes that can be used to produce etch stop layers with a dielectric constant under 5.5, including successive deposition of multiple layers of silicon nitride, which "eliminates pinholes and produces a denser film." *Id.* at 5:66–6:7.

D. Illustrative Claim

The Petition challenges claims 1, 2, 5–7, and 10, of which claims 1 and 6 are independent. Ex. 1001, 8:57–12:35. Claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An integrated circuit comprising:
>
> a semiconductor substrate having a semiconductor device provided thereon;
>
> a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;
>
> a first conductor core filling the first opening and connected to the semiconductor device;
>
> an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;
>
> a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;
>
> a second conductor core filling the second opening and connected to the first conductor core.

Ex. 1001, 6:54–7:2.

Claim 6 is similar to claim 1, except that it recites an additional dielectric layer (called a via dielectric layer) and an additional etch stop layer (called a channel etch stop layer), and the second conductor core fills openings in both the via and second dielectric layers. *Id.* at 7:15–8:11.

E. Instituted Ground of Unpatentability

We instituted *inter partes* review based on the sole ground of unpatentability asserted in the Petition: whether claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Watatani[3] and Tanaka I.[4] Dec. 20.

II. ANALYSIS

A. Claim Construction

In this *inter partes* review, the '330 patent has not yet expired, and claim terms are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016).[5] Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

---

[3] Watatani, US 6,153,511, filed June 25, 1999, and issued November 28, 2000, Ex. 1005 ("Watatani"). Watatani is asserted as prior art under 35 U.S.C. § 102(e). Pet. 25 n.7.

[4] Masayuki Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1006 ("Tanaka I"). Tanaka I is asserted as prior art under 35 U.S.C. § 102(b). Pet. 27 n.8. Petitioner relies on the Declaration of Peter J. Rolla, an employee of the University of California San Diego Library in La Jolla, California, to establish public accessibility of Tanaka I. Ex. 1009.

[5] A recent amendment to this rule does not apply here, because the Petition was filed before November 13, 2018. *See* "Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board," 83 Fed. Reg. 51,340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42).

In the Institution Decision, we determined it was not necessary to resolve any claim construction disputes for purposes of that decision. Dec. 7–8. Neither party challenges that determination. Patent Owner continues to argue that the phrase "etch stop layer of silicon nitride" is not limited to a layer of pure silicon nitride and allows for the presence of dopants and/or impurities. *Compare* PO Resp. 12–15, *with* Prelim. Resp. 15–20. Petitioner argues there is no controversy in this proceeding to which Patent Owner's proposed construction is relevant. Pet Reply 1. We agree, as Patent Owner does not rely on its proposed claim construction for any patentability argument. In fact, Patent Owner relies on the assertions of Petitioner and Dr. Fair regarding one of the asserted prior art references—Tanaka I (Ex. 1006)—as support for Patent Owner's claim construction. PO Resp. 15. More particularly, Patent Owner concedes that the silicon nitride etch stop layer disclosed in Tanaka I, which contains hydrogen and chlorine impurities, is an "etch stop layer of silicon nitride" within the meaning of claims 1 and 6. *Id.* Under these circumstances, we do not need to provide an express construction for the phrase "etch stop layer of silicon nitride" for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Petitioner bears the burden of proving unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail,

Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In this case, neither party relies on objective evidence of nonobviousness, i.e., secondary considerations.

C. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Fair, testifies that a person of ordinary skill in the art ("POSA") would have had at least a Bachelor of Science degree in electrical engineering, material science, physics, chemistry, or a closely related field, and at least five years of industry experience in the development of semiconductor process technologies and the fabrication of semiconductor devices. Ex. 1003 ¶ 18. Dr. Fair further testifies that an individual with an advanced degree in a relevant field would require less experience in developing process technologies and in fabricating semiconductor devices. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that a POSA would have held a master's degree in physics, electrical engineering, or a related field, and would have had three years or more

experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2008 ¶ 29.

For purposes of our Institution Decision, we accepted the description of a POSA provided by Dr. Bottoms. Dec. 8 (citing Ex. 2001 ¶ 33). Dr. Bottoms testifies that his description does not differ significantly from Dr. Fair's. Ex. 2008 ¶ 29. Dr. Fair testifies that Dr. Bottoms' description of the level of ordinary skill in the art is consistent with the level proposed in his original declaration, and the Board's adoption of that description does not change his opinions. Ex. 1017 ¶ 5.

Consistent with the testimony of Dr. Fair and Dr. Bottoms, we find there is little difference between the descriptions of a POSA, and the outcome of our patentability determinations would be the same, regardless of which description we accept. Therefore, consistent with the Institution Decision, we adopt Dr. Bottoms' description of a POSA. Ex. 2008 ¶ 29. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Dr. Fair and Dr. Bottoms, as set forth in each witness's declaration and curriculum vitae ("CV"), we find that each of these declarants has sufficient education and experience related to the subject matter of the '330 patent to testify from the perspective of a POSA at the time of the invention. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2008 ¶¶ 6–17. *See* Trial Practice Guide Update," 83 Fed. Reg. 38,989 (Aug. 13, 2018), *available at* https://go.usa.gov/xU7GP ("TPG Update"), 3 ("A person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be "qualified in the

pertinent art.'" (quoting *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008))). Regarding the qualifications of Dr. Fair, we find particularly relevant his experience as an acting president, vice president, and director at the Microelectronics Center of North Carolina ("MCNC") from 1981 to 1994, where he directed research on semiconductor processing, including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD (chemical vapor deposition) of thin films, metallization, and anisotropic etching processes, and conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. Ex. 1003 ¶ 9, Ex. 1004, 3. Regarding the qualifications of Dr. Bottoms, we find particularly relevant his experience at Varian Associates from 1976 to 1985, including his experience as Manager of Research and Development, where he was involved in developing tools used to fabricate semiconductor devices including lithography, sputtering, ion implantation, etching, and evaporation processes. Ex. 2008 ¶¶ 9–11; Ex. 2002, 1.

Petitioner argues that we should credit Dr. Fair's testimony and reject Dr. Bottoms' testimony because "Dr. Bottoms' expertise in the field pales in comparison to Dr. Fair's." Pet. Reply 18. Petitioner bases its argument on Dr. Bottoms' response to a deposition question regarding "Fick's laws of diffusion" and a comparison of the number of papers and conference presentations for the period 1984 to 2004 listed on each declarant's CV. *Id.* (citing Ex. 1004, 3–16; Ex. 1018, 9:20–24; Ex. 2002, 6–7). Petitioner's argument does not persuade us to reject Dr. Bottoms' testimony. In our view, Dr. Bottoms' inability to recall a name (Fick) associated with a

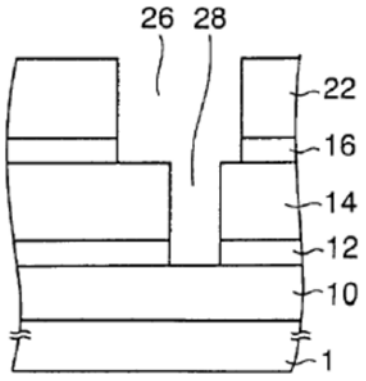
particular scientific principle does not prove a lack of expertise in the technologies relevant to this proceeding. Furthermore, the number of papers and conference presentations listed on Dr. Bottoms' CV is not the sole, or necessarily the best, measure of his level of expertise. The number of such items may depend on the institutional setting in which he worked, e.g., in industry rather than academia. Dr. Bottoms explains that his CV lists selected presentations and publications and omits some data for the relevant time period. Ex. 2015 ¶¶ 2–4. On this record, we find that Dr. Fair and Dr. Bottoms both have sufficient education and experience related to the subject matter of the '330 patent to testify regarding the knowledge and understanding of a POSA at the time of the invention and that, even if he is not a POSA, Dr. Bottoms' testimony is helpful to the Board. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2008 ¶¶ 6–17. *See* TPG Update, 3.

D. Prior Art References

1. Watatani (Ex. 1005)

Watatani discloses a semiconductor device having a multilayer interconnection structure. Ex. 1005 at (54). According to Watatani, Figures 1A–F "show a typical example of the conventional dual damascene process of forming a multilayer interconnection structure . . . ." *Id.* at 1:65–67. Petitioner relies on Watatani Figure 1F, which is reproduced below:

FIG.1F
PRIOR ART



Watatani Figure 1F illustrates a structure resulting from a processing step in a conventional dual damascene process. Ex. 1005, 1:65–67, 2:43–48, 5:32–33. The structures shown in Watatani Figure 1F include silicon (Si) substrate 1, lower interconnection pattern 10 of conductive material such as copper (Cu), etching stopper film 12 of silicon nitride (SiN), first interlayer insulation film 14 of silicon oxide (SiO_2), second etching stopper film 16 of SiN, second interlayer insulation film 22 of SiO_2, interconnection groove 26, and contact hole 28. *Id.* at 2:1–41. According to Watatani, "an insulation film (not illustrated) [is] interposed between the Si substrate 1 and the lower interconnection pattern 10." *Id.* at 2:3–5. Watatani discloses that interconnection groove 26 and contact hole 28 are filled with copper (Cu). *Id.* at 2:42–47.

According to Watatani, the multilayer interconnection structure of Figure 1F "has a drawback, due to the use of SiO_2 having a large dielectric constant, for the interlayer insulation film 14 or 22, in that the interconnection patterns tend to have a large stray capacitance." Ex. 1005, 2:54–58. Watatani discloses that this problem is overcome by using "an organic interlayer insulation film having a characteristically small dielectric constant." *Id.* at 2:61–64. Watatani states, however, that conventional multilayer interconnection structures using an organic interlayer insulation film also suffer from a drawback, namely, that resist pattern misalignments are difficult to correct. Ex. 1005, 3:51–4:41. To address the resist pattern misalignment problem, Watatani discloses a semiconductor fabrication process that includes the steps of forming a first etching stopper film on an organic interlayer insulation film and forming a second, different etching stopper film on the first etching stopper film. *Id.* at 4:48–5:25; *see also id.* at

6:4–10 (disclosing "an etching stopper structure 81, formed of a stacking of two etching stopper layers, . . . a first etching stopper film 80 of SiN . . . and a second etching stopper film 82 of SiO_2"); Fig. 5A.

2. Tanaka I (Ex. 1006)

Tanaka I addresses the problem of parasitic capacitance associated with copper (Cu) interconnects formed by a conventional damascene process that uses high-k SiN film for the etch stopper layers. Ex. 1006, 1-1.[6,7] To solve this problem, Tanaka I discloses a "[n]ew low-k SiN film with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation . . . ." *Id.* at 1-1, 1-2. The film is formed by an ultra-low temperature thermal chemical vapor deposition ("CVD") process using HexaChloroDisilane (HCD, Si_2Cl_6) as a silicon source. *Id.* at 1-1. Tanaka I refers to the new film as "HCD-SiN" and discloses a deposition process and film properties for the new film. *Id.* at 1-1, 1-2, Figs. 2–8.

Figure 1 of Tanaka I is reproduced below:

[6] We cite to Tanaka I and other non-patent references using the page numbers added by Petitioner or Patent Owner followed by a hyphenated suffix ("-1," "-2," or "-3") to indicate the first, second, or third column.

[7] Dr. Fair explains that "[t]he dielectric constant of a material, which is sometimes referred to as its permittivity and which is represented by the letter 'k,' is an intrinsic property of a material . . . ." Ex. 1003, 19 n.2.

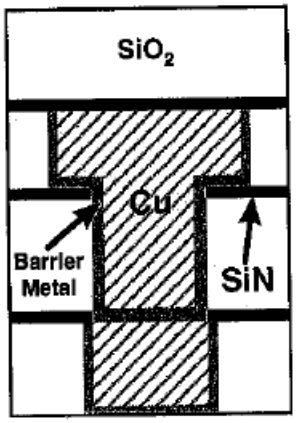


Fig.1 A schematic drawing of Cu interconnects formed by damascene process

Figure 1 of Tanaka I shows copper interconnects formed by a conventional dual damascene process, which requires "plural layers of high-k SiN film for a groove etch stopper and a barrier of Cu diffusion and oxidation . . . ." Ex. 1006, 1-1. As explained above, Tanaka I proposes improving upon this conventional process by using "HCD-SiN as the etch-stop and the barrier layer . . . to realize Cu damascene interconnects for high performance VLSIs."[8] *Id.*

E. Petitioner's Obviousness Ground

Petitioner contends that claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable as obvious in view of Watatani and Tanaka I. Pet. 29–38, 42–53. We address each of the challenged claims below.

1. Claims 1 and 6

Petitioner contends that the conventional dual damascene interconnect structure of Watatani teaches or suggests all elements of independent

[8] The acronym VLSI refers to very large scale integrated devices. *See* Ex. 1013, 1.

claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 29–38, 42–53. Petitioner acknowledges that Watatani does not disclose the dielectric constant of the silicon nitride etch stop layer and relies on Tanaka I for that feature. *Id.* at 35–36, 48, 51. Petitioner contends that a POSA would have been motivated to use Watatani's conventional dual damascene interconnect structure, labeled as a prior art structure, but use Tanaka I's low-k silicon nitride etch stop layers instead of conventional silicon nitride etch stop layers in order to minimize the stray capacitance issue discussed in both references. *Id.* at 29, 36. Petitioner contends that a POSA would have been motivated to combine the teachings of Watatani and Tanaka I and would have had a reasonable expectation of success in doing so. *Id.* at 13–15, 36, 48–49, 51–52, 56–60.

Patent Owner argues that Watatani does not disclose an etch stop layer formed over the first dielectric layer, as recited in the claims. PO Resp. 35. In addition, Patent Owner challenges the sufficiency of the evidence to establish motivation and a reasonable expectation of success for the combination of Watatani's damascene structure with Tanaka I's low dielectric constant silicon nitride. *Id.* at 35–53.

Petitioner directs us to substantial evidence that Watatani's conventional dual damascene structure (Ex. 1005, 1:65–2:47, Figs. 1A–F) discloses all limitations of claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 29–34, 37–38, 42–47, 49–50, 52–53. Patent Owner does not contest that evidence, except to argue that Watatani does not disclose an etch stop layer formed over the first dielectric layer, an argument we address in section II.E.1.a below. *See* PO Resp. 35. We determine Petitioner has shown by a preponderance of the evidence that

all of the uncontested limitations of claims 1 and 6 are disclosed by Watatani and, in some cases, also by Tanaka I. Pet. 29–34, 37–38, 42–47, 49–50, 52–53. The remainder of our analysis focuses on the contested limitations of claims 1 and 6, i.e., "etch stop layer of silicon nitride formed over the first dielectric layer" and "etch stop layer having a dielectric constant below 5.5."

a. "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core"

Petitioner contends that Watatani describes and depicts etching stopper film 12 of silicon nitride formed over first conductor core 10 and the underlying dielectric layer. Pet. 35, 47 (citing Ex. 1005, 2:5–7, Figs. 1A–1F).

Patent Owner argues that Watatani's insulation film (i.e., first dielectric layer) is between substrate 1 and lower interconnection pattern 10, which suggests that "when the etching stopper film 12 is formed on the interconnection pattern 10, it cannot be formed over the insulation film." PO Resp. 35.

We have considered Patent Owner's argument, but are persuaded that Petitioner has met its burden of proof for two alternative reasons advanced by Petitioner. Pet. 35, 47; Pet. Reply 2–5.

First, Petitioner persuades us that its contention is based on the broadest reasonable interpretation of the term "over" and that Patent Owner's argument is based on an unduly narrow construction of that term. Pet. Reply 3–4.

Petitioner relies on the following disclosure in Watatani:

> Referring to FIG. lA, a substrate 1 of Si carries thereon a lower interconnection pattern 10 of a conductive material such as Cu, with an insulation film (not illustrated) interposed between

> the Si substrate 1 and the lower interconnection pattern 10. Further, a first etching stopper film 12 of SiN is formed on the lower interconnection pattern 10 . . . .

Ex. 1005, 2:1–6; Pet. 35, 47; *see also* Ex. 1005, Fig. 1A (showing a sequence of layers from bottom to top: 1, 10, 12, 14, 16, 18). Watatani's etch stop layer 12 is not expressly described as being formed *on* the first dielectric layer (insulation film). Nonetheless, Petitioner persuades us that the broadest reasonable construction of "over" does not require that the etch stop layer be formed directly "on," or in contact with, the first dielectric layer. Pet. Reply 3–4.

The Specification of the '330 patent uses both terms, "over" and "on," when describing the relationship between various layers. *See, e.g.*, Ex. 1001, 3:51–54 ("[a] dielectric layer is on the semiconductor substrate" and "an etch stop layer [is] over the first dielectric layer and conductor core"). Claims 1 and 6, however, recite an "etch stop layer of silicon nitride formed *over* the first dielectric layer and the first conductor core" (emphasis added), not an etch stop layer formed *on* the first dielectric layer. Patent Owner does not direct us to any intrinsic evidence supporting an express definition or disclaimer that would restrict the meaning of "over" to require direct contact between the etch stop layer and the first dielectric layer. Petitioner, on the other hand, directs us to a description in the Specification where the term "over" is used to describe layers that are not necessarily in direct contact with underlying layers. Pet. Reply 4 (quoting Ex. 1001, 3:4–9 ("The capping layer may be an etch stop layer and may be processed farther for placement of additional levels of channels and vias over it.")). Accordingly, Petitioner persuades us that the term "over," as used in the '330 patent, is broad enough to encompass a structure in which the etch stop

layer is formed over the first dielectric layer, with a first conductor core (lower interconnection pattern 10) between the etch stop layer and the first dielectric layer, as Patent Owner acknowledges is disclosed by Watatani. PO Resp. 35.

Petitioner also persuades us that Watatani teaches or suggests an "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core," even under Patent Owner's narrow construction of the term "over." Pet. Reply 4 (citing Ex. 1003 ¶¶ 22–35; Ex. 1005, 2:1–5; Ex. 1007,[9] 1 (Fig. 1)).

Watatani discloses that silicon nitride etch stop layer 12 is formed on lower interconnection pattern 10. Ex. 1005, 2:5–6. Watatani's interconnection pattern 10 is a *pattern* of conductive material, not a continuous layer of conductive material. According to Watatani, when the conductive material is copper, such an interconnection pattern is generally formed by a dual damascene process in which a pattern of interconnection grooves and contact holes is formed in an insulation film followed by deposition of a copper layer, which fills the interconnection grooves and contact holes. *Id.* at 1:34–43; *see also* Ex. 1003 ¶ 28 (describing "damascene" technique for copper metallization). The damascene process produces a pattern in which copper is "inlaid" into interconnection grooves and contact holes that have been etched into an insulating film. Ex. 1003 ¶ 28; Ex. 1005, 1:34–43; Ex. 1007, 1 (Figure 1 showing dual damascene

[9] Robert L. Jackson et al., *Processing and Integration of Copper Interconnects*, Solid State Technology, March 1998, pages 49–50, 54, 56, 59 ("SST 1998").

process, including step 1: SiN deposition on copper interconnect (Metal 1) pattern).

The layer identified by reference numeral 10 in Watatani Figures 1A–1F is described as a "Cu interconnection pattern 10," which means the layer comprises a pattern of copper conductors inlaid within an insulating film. Ex. 1003 ¶¶ 27, 28; Ex. 1005, 1:34–43, 2:1–5; *see also* PO Resp. 39 (illustrating "typical" damascene structure in which parallel conductors are separated by insulating material "in the same metal level"). Watatani discloses that silicon nitride etch stop layer 12 is formed "on" interconnection pattern 10, i.e., *on both the conductors and the insulation film of the interconnection pattern*. Ex. 1005, 2:5–6.

Accordingly, Petitioner has shown by a preponderance of the evidence that Watatani discloses an "etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core," as recited in claims 1 and 6, even if the term "over" is construed to mean "on," as Patent Owner implicitly contends. PO Resp. 35.

b. "etch stop layer having a dielectric constant below 5.5"

There is no dispute that Tanaka I discloses a silicon nitride etch stop layer having a dielectric constant below 5.5. Ex. 1006, 1-1 (disclosing "[n]ew low-k SiN film, with permittivity of 5.4" as an etch stop layer for copper damascene interconnects); Pet. 35–36, 48, 51; PO Resp. 28. Dr. Bottoms testifies that "[p]ermittivity as used in Tanaka I means relative permittivity and is synonymous with dielectric constant." Ex. 2001 ¶ 98; *see also* Ex. 1003, 19 n.2 (explaining that the dielectric constant of a material is sometimes referred to as its permittivity and is represented by the letter "k").

There is also no dispute that Watatani discloses a conventional dual damascene structure having silicon nitride etch stop layers. Ex. 1005, 2:5–6 ("a first etching stopper film 12 of SiN"); *id.* at 2:9–11 ("a second etching stopper film 16 of SiN"); *id.* at Figs. 1A–1F (illustrating a conventional dual damascene process, including silicon nitride etch stop layers 12 and 16); Pet. 35, 47, 50; PO Resp. 20.

The parties dispute whether Petitioner has established a motivation and a reasonable expectation of success for the combination of Watatani's conventional dual damascene interconnect structure and Tanaka I's low dielectric constant silicon nitride etch stop layer. For the reasons that follow, we are persuaded that Petitioner has met its burden of proof in this regard. Pet. 13–15, 36, 48–49, 51–52, 56–60.

Petitioner relies on the testimony of Dr. Fair that "[a] person of ordinary skill in the art would have been motivated to use Tanaka's low-k silicon nitride etch stop layer instead of the conventional silicon nitride etch stop layer in the dual damascene structure of Watatani in order to reduce the problem of stray capacitance discussed in both Watatani and Tanaka." Ex. 1003 ¶ 95; *see also id.* ¶ 152 (same); Pet. 36, 48–49, 51–52. We find that Dr. Fair's testimony is credible and supported by the express teachings of Watatani and Tanaka I. Watatani acknowledges the problem of stray capacitance in conventional multilayer interconnect structures and discloses substituting a low dielectric constant insulation film for a conventional insulation film having a large dielectric constant as a solution to the stray capacitance problem. Ex. 1005, 1:23–33, 2:54–64. Tanaka I teaches a similar solution to the same problem, namely, using a "low-k SiN film" as an etch stop layer in an interconnect structure formed by a conventional

copper damascene process. Ex. 1006, 1-1, Fig. 1. These disclosures of Watatani and Tanaka I support Dr. Fair's testimony that a POSA would have been motivated to use Tanaka's low-k silicon nitride etch stop layer in Watatani's conventional dual damascene structure in order to address the problem of stray capacitance. Ex. 1003 ¶¶ 95, 152.

Petitioner relies on the undisputed testimony of Dr. Fair that a POSA "knew long before the filing date of the 330 Patent that one way to reduce the capacitance between two metal lines, and improve interconnect performance, is to reduce the dielectric constant of the materials between those lines." Ex. 1003 ¶ 42; Pet. 13–14. We find that Dr. Fair's testimony is credible and supported by the mathematical formula he provides for calculating the capacitance between two parallel metal plates. Ex. 1003 ¶ 42 (capacitance can be represented by the formula: $C = k\varepsilon_0 A/d$, where k is the dielectric constant of the material between the plates). This equation shows that capacitance is directly proportional to the dielectric constant of the material between the plates. Dr. Bottoms agrees that "capacitance is directly proportional to the area of the conductors and to the relative permittivity or dielectric constant of the dielectric material between the conductors of the capacitor." Ex. 2008 ¶ 37. Dr. Bottoms quotes Dr. Fair's testimony, relying on the same capacitance equation to show "what one of ordinary skill in the art would expect." *Id.* ¶ 153. The known relationship between capacitance and dielectric constant reinforces that a POSA would have been motivated to use a low dielectric constant etch stop layer as a way to reduce stray capacitance between adjacent conductors.

We also credit Dr. Fair's testimony that "a person of ordinary skill in the art would have had a reasonable expectation of success in using

Tanaka's low-k silicon nitride etch stop layers in place of Watatani's conventional silicon nitride etch stop layers in Watatani's conventional dual damascene structure." Ex. 1003 ¶ 153; *see* Pet. 36, 48–49, 51–52, 59. Dr. Fair's testimony is supported by the express disclosures of Tanaka I and Watatani. Tanaka I's low-k silicon nitride film is used for the same purpose as the silicon nitride film in Watatani, namely, as an etch stop layer in a conventional dual damascene copper interconnect structure that uses a silicon oxide insulation film. Ex. 1005, 2:5–6 ("a first etching stopper film 12 of SiN"); *id.* at 2:10–11 ("second etching stopper film 16 of SiN"); *id.* at Figs. 1A–1F (illustrating conventional dual damascene process of forming a multilayer interconnect structure that uses an SiO_2 interlayer insulation film); Ex. 1006, 1-1, Fig. 1 (disclosing new low-k SiN film as the etch stop layer for conventional Cu damascene interconnects with an SiO_2 insulating layer). We find Petitioner's combination would have had a reasonable expectation of success because Tanaka I teaches an improvement to the same type of prior art device described by Watatani as needing improvement—a conventional dual damascene interconnect structure. *In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) ("[T]he strength of the correlation between the references gives rise to a reasonable expectation of success from combining them.").

Petitioner directs us to express disclosures in Tanaka I that support a finding that Petitioner's proposed combination would have had a reasonable expectation of success. For example, Petitioner relies on Tanaka I's disclosure: "New low-k SiN film, with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation, has been *successfully developed*." Ex. 1006, 1-1, 1-2 (emphasis added); Pet. Reply 10. Petitioner also relies on

Tanaka I's conclusion that the low-k film, with a permittivity of 5.4, "should be the solution to realize Cu damascene interconnects for high performance VLSIs." Ex. 1006, 1-1, 1-2; Pet. 59. As noted by Petitioner, Tanaka I summarizes the results of various experiments by stating "superior process results and film properties" for its low-k silicon nitride layer are presented. Ex. 1006, 1-1; Pet. 58. From the results of etch rate selectivity tests, for example, Tanaka I concludes that the disclosed low-k silicon nitride film has "enough ability for etching stopper." Ex. 1006, 1-2; *see* Pet. Reply 16. Petitioner persuades us that these disclosures would have provided a POSA with a reasonable degree of confidence that Tanaka I's low-k silicon nitride film would function as an etch stop in Watatani's conventional dual damascene interconnect structure. Pet. 58–59; Pet. Reply 10–11, 15–17.

We now turn to Patent Owner's arguments contesting motivation to combine and a reasonable expectation of success.

Patent Owner begins by focusing on Watatani, arguing it "does not teach that silicon nitride etch stops are a source of stray capacitance" and "offers no motivation related to etch stop layers having a low dielectric constant." PO Resp. 36, 37. We have considered Patent Owner's argument, but are nevertheless persuaded by Petitioner's reliance on Watatani as evidence of a motivation to combine. As Petitioner persuasively argues, Watatani is concerned with the same problem addressed by Tanaka I and the '330 patent, namely, the problem of stray capacitance in conventional dual damascene interconnect structures. Pet. 56–57; Ex. 1001, 3:32–42; Ex. 1005, 1:23–33; Ex. 1006, 1-1. Watatani recognizes the relationship between stray capacitance and the dielectric constant of layers used to make a multilayer interconnect, and addresses the problem of stray capacitance in

a manner similar to Tanaka I and the '330 patent, namely, by replacing a high dielectric constant film with a low dielectric constant film. Ex. 1005, 2:54–64. It is true that Watatani's solution pertains to a different material layer than either Tanaka I or the '330 patent—the silicon oxide interlayer insulation film, rather than the silicon nitride etch stop layer. *Id.* But Watatani nevertheless supports and is fully consistent with Petitioner's contention that a POSA would have been motivated to address the problem of stray capacitance by replacing a high dielectric constant material with a lower dielectric constant material, such as by replacing a high dielectric constant etch stop layer with a low dielectric constant etch stop layer.

Next, Patent Owner argues there is no evidence that a POSA would have been motivated to adopt Tanaka I's solution either "in lieu of" or "in addition to" Watatani's solution, which uses a low dielectric constant organic insulation film to reduce parasitic capacitance. PO Resp. 37–38, 44. Patent Owner's argument misconstrues Petitioner's obviousness contention, which is based on Watatani's conventional dual damascene interconnect structure that uses conventional inorganic insulating films, not Watatani's proposed improvements to that conventional structure that use lower dielectric constant organic insulating films. *See, e.g.*, Pet. 35 (referencing the conventional dual damascene structure shown in Watatani Figures 1A–1F). *See In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) ("The use of patents as references is not limited to what the patentees describe as their own inventions." (internal quotations omitted)).

Patent Owner's argument also misconstrues Petitioner's burden. Petitioner's obviousness case is not undermined by Watatani's disclosure of alternative techniques for reducing stray capacitance. *See* Pet. 59–60

(discussing Watatani's disclosure of organic insulating layers). To prove its case, Petitioner needs to show that a POSA "would have seen a benefit" from improving Watatani's conventional dual damascene interconnect structure with Tanaka I's low-k silicon nitride etch stop layer. *See KSR*, 550 U.S. at 424 (in assessing obviousness, the "proper question" is whether a person of ordinary skill in the art "would have seen a benefit" to upgrading a known device with another feature known in the art in the manner claimed by patentee).

Obviousness may be shown even if Petitioner's combination of Watatani and Tanaka I would have been less effective at reducing stray capacitance than Watatani's embodiments having an organic insulation film. *See, e.g.*, *Slot Speaker Techs., Inc. v. Apple Inc.*, 680 F. App'x 932, 940 (Fed. Cir. 2017) ("It is irrelevant whether Tomonori and Sadaie together would be less effective than Sadaie alone at avoiding the absorption of certain low frequencies."). Petitioner's burden is to show that the claimed invention would have been obvious to a POSA at the time of the invention, not that it was the best option available to a POSA. *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) ("[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.").

Next, Patent Owner argues that "reducing the dielectric constant of etch stop layers . . . might have limited impact" on reducing parasitic capacitance, and reducing the dielectric constant of other layers "might outweigh the effect of reducing the dielectric constant of etch stop layers." PO Resp. 38. According to Patent Owner, the dielectric constant of etch stop layers has "little or no effect" on capacitive coupling, which Patent

Owner asserts is more significant than stacked capacitance as a source of parasitic capacitance. *Id.* at 38–41 (citing Ex. 2008 ¶¶ 124, 125, 127; Ex. 2009, 65:12–66:8; Ex. 2010,[10] 3, Figs. 2, 5; Ex. 2011,[11] 3, Fig. 8).

Again, Patent Owner's argument misconstrues Petitioner's burden, which does not require proof that the benefit of Petitioner's combination outweighs the benefit of other available options, such as reducing the dielectric constant of other layers. *Slot Speaker*, 680 F. App'x at 940; *Mouttet*, 686 F.3d at 1334. We agree with Petitioner that Patent Owner's argument is contrary to the teachings of Tanaka I, which states that low-k silicon nitride etch stop layer "should be the solution" to the "parasitic capacitance" problem caused by the "high permittivity of [conventional] SiN." Ex. 1006, 1-1; Pet. Reply 5–6.

Although Patent Owner relies on Igarashi (Ex. 2010) and Lecarval (Ex. 2011) (*see* PO Resp. 38–41; Ex. 2008 ¶¶ 125–127), Petitioner persuades us that these references do not support Patent Owner's position. Pet. Reply 7. As noted by Petitioner, Tanaka I cites Igarashi and Lecarval as support for Tanaka I's statement that the "high permittivity of [conventional] SiN" contributes to the performance degradation of copper damascene structures due to "parasitic capacitance." Ex. 1006, 1; Pet. Reply 7. We give greater weight to Tanaka I's 1999 interpretation of Igarashi and Lecarval than to Dr. Bottoms' *post hoc* opinion that reducing the dielectric

[10] M. Igarashi, et al., *The Best Combination of Aluminum and Copper Interconnects for a High Performance 0.18μ CMOS Logic Device*, IEEE International Electron Devices Meeting, 829–32 (1998) ("Igarashi").

[11] G. Lecarval, et al., *Advanced Interconnect Scheme Analysis: Real Impact of Technological Improvements*, IEEE International Electron Devices Meeting, 837–40 (1998) ("Lecarval").

constant of etch stop layers "might have limited impact" on parasitic capacitance. Ex. 2008 ¶ 124.

Moreover, Petitioner directs us to disclosures in Igarashi and Lecarval that contradict Patent Owner's argument. Pet. Reply 6–7 (discussing Ex. 2010, 1-2; Ex. 2011, Fig. 8). For example, Igarashi teaches "it is not desirable for the interconnects to contain such a high Si_3N_4 [silicon nitride] film with a 'high-k' dielectric, because the effective dielectric constant clearly increases." Ex. 2010, 1-2. Similarly, based on the comparison in Figure 8, Lecarval concludes that "[f]or damascene [structures], the low-k material slightly improves" the cross-talk sensitivity. Ex. 2011, 3-1.[12] Lecarval characterizes the effect of low dielectric constant materials as an improvement, even though "the impact of the materials remains low." *Id*.

Next, Patent Owner argues there is no evidence "that replacing conventional silicon nitride etch stops would cause a meaningful reduction in parasitic capacitance, relative to Watatani's low dielectric constant spin-on glass damascene structure." PO Resp. 42. Again, Patent Owner's argument misconstrues Petitioner's burden, which does not require proof that Petitioner's combination of Watatani and Tanaka I is an improvement

[12] Lecarval's conclusion is based on Figure 8, which compares cross-talk sensitivity, X, as a function of metallization layer thickness for three different structures at two different pitches (0.4 μm and 0.6 μm): (1) a non-damascene structure with an Al metallization layer and a low-k dielectric; (2) a "Cu SiO_2" damascene structure having etch stop layers with a permittivity of 7 and thicknesses of 0.04 μm and 0.12 μm and a dielectric layer with a permittivity of 4; and (3) a "Cu low k" damascene structure having etch stop layers with a permittivity of 4 and thicknesses of 0.04 μm and 0.04 μm and a dielectric layer with a permittivity of 3. Ex. 2011, 1-2, 2-1, 3-1 (Table 1, Figs. 3 and 8).

relative to Watatani's embodiments that use organic spin-on glass ("SOG") film. *Slot Speaker*, 680 F. App'x at 940; *Mouttet*, 686 F.3d at 1334. *See* Ex. 1005, 3:4–14, 5:61–66, 6:1–3 (disclosing SOG embodiments).

Next, Patent Owner identifies various parameters, such as etch stop layer thickness, that are not disclosed by Watatani and asserts, because these parameters are unknown, a POSA "would have no basis to conclude" that stray capacitance would be reduced by modifying Watatani's device to incorporate Tanaka I's low dielectric constant silicon nitride etch stop layer. PO Resp. 42–44 (citing Ex. 2008 ¶ 130; Ex. 1013,[13] Fig. 17). We disagree. Patent Owner's argument does not adequately account for the express teachings of Watatani and Tanaka I and the known relationship between dielectric constant and capacitance, which Petitioner has persuasively relied upon to show that a POSA would have been motivated to use a low dielectric constant silicon nitride etch stop layer to reduce stray capacitance. *See* pages 20–21, *supra*.

Next, Patent Owner argues that replacing Watatani's conventional silicon nitride etch stop layer with Tanaka I's low dielectric constant etch stop layer "may require increasing the thickness of the etch stop layer by an amount that would cause an overall increase in stray capacitance." PO Resp. 43 (citing Ex. 2008 ¶ 130; Ex. 2009, 70:6–71:12). We find Patent Owner's argument is speculative and not supported by the record as a whole. Although Patent Owner and Dr. Bottoms make vague references to etch selectivity (PO Resp. 42; Ex. 2008 ¶ 129), on this record, it would be

[13] Masayuki Tanaka, et al, *Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia*, Journal of The Electrochemical Society, 147 (6) 2284–89 (2000) ("Tanaka II").

entirely speculative to find that a thicker layer would be required for purposes of etch selectivity. We are persuaded by Petitioner's arguments and Dr. Fair's testimony directing us to disclosures in Tanaka I and Tanaka II that use of low-k silicon nitride would have permitted a thinner-than-conventional etch stop layer. Pet. Reply 7–8; Ex. 1017 ¶ 18 (both quoting Ex. 1006, 1; Ex. 1013, 6).

Next, Patent Owner asserts that the presence of chlorine in Tanaka I's HCD-SiN material would have driven a POSA away from using Tanaka I's approach because chlorine was known to corrode copper interconnects. PO Resp. 44 (citing Ex. 2008 ¶¶ 101, 104). We are persuaded by Petitioner's response to Patent Owner's assertion, which relies on Dr. Fair's detailed analysis, supported by citations to Tanaka I, explaining why a POSA would not have been concerned about the presence of chlorine in Tanaka I's silicon nitride etch stop material. Pet. Reply 8–9; Ex. 1017 ¶ 19 (citing and quoting Ex. 1006, title, 1-2, Fig. 8). For example, Petitioner and Dr. Fair rely on Tanaka I's tests showing stability of chlorine in low-k films. Pet. Reply 8; Ex. 1017 ¶ 19; Ex. 1006, 1-2. In contrast, Dr. Bottoms' opinions regarding chlorine corrosion of copper interconnects is unsupported by citations to Tanaka I or other evidence. Ex. 2008 ¶¶ 101, 104. In fact, Dr. Bottoms admits "*[t]here is no data* on . . . corrosion of Cu in the metallization." *Id.* ¶ 139 (emphasis added). Patent Owner had the opportunity to cross-examine Dr. Fair's reply testimony and submit observations or to request a sur-reply on this topic, but declined to do so. Under these circumstances, we find that Dr. Fair's testimony regarding chlorine corrosion of copper interconnects to be more credible than Dr. Bottoms' testimony on this topic.

Turning to the issue of reasonable expectation of success, Patent Owner argues that Tanaka I provides "insufficient information" to suggest that Tanaka I's HCD-SiN films "would work as etch stop layers in Watatani's process or that such etch stop layers could be made thin enough in Watatani's process to ultimately lower the device capacitance." PO Resp. 45 (citing Ex. 2008 ¶ 132). Patent Owner asserts that Tanaka I "omits critical characteristics of the HCD-SiN material, making its suitability as an etch stop speculative at best." *Id.*

We agree with Petitioner that Patent Owner's arguments do not accurately characterize Tanaka I, which states that the HCD-SiN film "has been successfully developed" and discloses tests designed to show that HCD-SiN will work as an etch stop layer in copper damascene metallization structures like Watatani's. Pet. Reply 10–11; Ex. 1006, 1, Fig. 1; Ex. 1017 ¶¶ 22, 23. In our view, Patent Owner's arguments demand more of the prior art than is provided by the sparse disclosure of the '330 patent. *See* Pet. 19 ("the 330 Patent sets forth few details on how to accomplish the reduction [in dielectric constant] or implement the methods"). Most of the information Patent Owner contends is missing from Tanaka I is not disclosed by the '330 patent. For example, the '330 patent does not disclose etch chemistries, etch selectivity, or the thickness of the dielectric layers being etched. *Cf.* PO Resp. 48 (listing etch chemistry and relative thickness of the materials as factors affecting suitability as an etch stop); *id.* at 49 (asserting that Tanaka I does not disclose etch selectivity between SiO_2 and HCD-SiN). Nor does the '330 patent disclose any information regarding the barrier property of silicon nitride etch stop layers. *Cf.* PO Resp. 50–52 (asserting that barrier property is a necessary characteristic of an etch stop and the disclosure of

Tanaka I is deficient in this regard). Tanaka I provides at least as much, if not more, information than the '330 patent regarding suitability of low dielectric constant silicon nitride as an etch stop layer. Ex. 1006, 1-2, 2-2, Fig. 6 ("Selectivity of RIE etching rate versus TEOS"). The '330 patent's sparse disclosure, as compared with Tanaka I's more detailed disclosure, persuades us that Tanaka I's disclosure is sufficient to provide a reasonable expectation of success of achieving the claimed invention. *See Trustees of Columbia Univ. in City of New York v. Illumina, Inc.*, 620 F. App'x 916, 929 (Fed. Cir. 2015) (relying on disclosure of challenged patent as substantial evidence sufficient to support PTAB's finding of a reasonable expectation of success in combining prior art references and synthesizing the claimed nucleotide).

Patent Owner faults Petitioner for not presenting evidence of a commercial product that uses Tanaka I's HCD-SiN as an etch stop layer. PO Resp. 47. We agree with Petitioner, however, that commercial success of the prior art is not a requirement for proof of obviousness. Pet. Reply 12. *In re Wright*, 569 F.2d 1124, 1128 (C.C.P.A. 1976) (obviousness should be measured against the nearest prior art, even if it is not "the commercial standard"). Patent Owner argues that later research "likely served as a deterrent that prevented adoption" of Tanaka I's HCD-SiN material. PO Resp. 47 (citing Ex. 2008 ¶ 134; Ex. 2012,[14] 2, 4, Fig. 7; Ex. 2013,[15] 1)). As

[14] Masayuki Tanaka et al., *Suppression of SiN-Induced Boron Penetration by Using SiH-Free Silicon Nitride Films Formed by Tetraschlorosilane and Ammonia*, 49 IEEE Transactions in Electron Devices 1526–31 (2002) ("Tanaka III").

[15] N. Mise, et al., *Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact*

noted by Petitioner, however, both references relied upon by Patent Owner were published after the filing date of the '330 patent, which means they are not relevant to determining whether there would have been a reasonable expectation of success. Pet. Reply 12 n.4. *Bristol-Myers Squibb Co. v. Teva Pharm., Inc.*, 752 F.3d 967, 976 (Fed. Cir. 2014) ("the skilled artisan's reasonable expectation of success is measured 'as of the date of the invention'" (quoting *Amgen Inc. v. Hoffman-La Roche*, 580 F.3d 1340, 1362 (Fed. Cir. 2009)). Furthermore, neither Patent Owner nor its expert explains how the later research (Exs. 2012, 2013) relates to a reasonable expectation of success for HCD-SiN film as an etch stop layer in copper damascene interconnect structures.

Relying on Dr. Fair's testimony about a need for further investigation, Patent Owner argues that a POSA would have recognized "a degree of uncertainty" when using Tanaka I's HCD-SiN material as an etch stop layer. PO Resp. 49 (citing Ex. 2009, 55:6–16, 77:22–78:1, 83:12–84:5). But Patent Owner does not argue that undue experimentation would be required, agreeing with Dr. Fair that any necessary experimentation would be "standard." *Id.* Petitioner directs us to the testimony of Dr. Fair and disclosures in Tanaka I, which persuade us that implementing Tanaka I's HCD-SiN material as an etch stop layer would have been within the level of skill in the art at the relevant time. Pet. Reply 14; Ex. 1003, ¶ 35; Ex. 1006, 1-1; Ex. 2009, 55:6–16, 77:9–78:10, 78:19–79:22. Moreover, Patent Owner's argument regarding "a degree of uncertainty" is inconsistent with the legal standard for a reasonable expectation of success. *Medichem, S.A. v.*

---

on Scaled MOSFETs, Extended Abstracts of the 2007 Int'l Conf. on Solid State Devices and Materials, Tsukuba, 724–35 (2007) ("Mise").

Rolabo, S.L., 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("certainty of success" is not required).

In the same vein, Patent Owner relies on Tanaka I's data regarding etch selectivity and Auger profiles to argue that a POSA would have recognized a "risk of over etching" and "doubted" the barrier ability and long-term stability of Tanaka I's HCD-SiN film. PO Resp. 50–52 (citing Ex. 2008 ¶¶ 138, 139); *see also* PO Sur-Reply (data in Tanaka I "raise[s] questions that would need investigation"). We agree with Petitioner that Patent Owner's arguments are contradicted by the express disclosures of Tanaka I, including its statements that HCD-SiN "is concluded to have enough ability for etching stopper," has the "same RIE etching resistance as conventional LPCVD SiN," and has "higher barrier ability for Cu diffusion than plasma-SiN." Pet. Reply 15–16; Ex. 1006, 1-1, 1-2. Moreover, Patent Owner's arguments regarding "risk," "doubt[]," and "questions" (PO Resp. 50–52) are inconsistent with the legal standard for a reasonable expectation of success. *In re Kubin*, 561 F.3d 1351, 1360 (Fed. Cir. 2009) ("Obviousness does not require absolute predictability of success . . . all that is required is a reasonable expectation of success." (citing *In re O'Farrell*, 853 F.2d 894, 903–04 (Fed. Cir. 1988))); *Medichem*, 437 F.3d at 1165.

Similarly, Patent Owner argues that the dielectric constant of HCD-SiN material would be affected by the deposition rate and would "likely" be affected by other parameters, such as deposition pressure, temperature, and layer thickness. PO Resp. 52–53 (asserting that "achieving a practical deposition rate . . . would require a corresponding increase in the dielectric constant" (citing Ex. 2008 ¶ 140)); PO Sur-Reply 2 ("Forming an etch stop layer with a dielectric constant of less than 5.5 . . . was uncertain."). Again,

Patent Owner's arguments are inconsistent with the legal standard for a reasonable expectation of success, which does not require manufacturability at practical rates, nor absolute certainty of success. *In re Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165. Regardless, Petitioner presents credible, unrebutted testimony of Dr. Fair that a POSA would have understood that slower deposition rates provide advantages over faster rates. Pet. Reply 13; Ex. 1017 ¶ 25.

After considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that a POSA would have been motivated to combine Watatani's conventional dual damascene interconnect structure with Tanaka I's low dielectric constant silicon nitride etch stop layer and would have had a reasonable expectation of success of achieving the claimed subject matter.

Accordingly, we are persuaded Petitioner has established by a preponderance of the evidence that claims 1 and 6 of the '330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

2. Claims 2 and 7

Claim 2 depends from claim 1 and recites "wherein the etch stop layer is a multilayer structure." Ex. 1001, 7:3–4. Claim 7 depends from claim 6 and recites "wherein the via and channel etch stop layers are a multilayer structure." *Id.* at 8:12–13.

Petitioner contends that "Watatani expressly describes an etch stop layer that includes 'three or more layers' of silicon nitride." Pet. 39, 54 (citing Ex. 1005, 7:54–55). Petitioner also contends that it was well known in the prior art to form multilayer silicon nitride films. *Id.* at 15, 20, 39, 54. Petitioner contends that a POSA would have been motivated to use a

multilayer approach because it would improve the uniformity of the etch stop film and improve its dielectric properties by avoiding pinholes. *Id.* at 16, 20, 40–41, 55.

In the Institution Decision, we rejected Petitioner's contention that Watatani describes an etch stop layer that includes three or more layers of silicon nitride. Dec. 17–18. Nevertheless, we instituted review on the basis of Petitioner's contentions that multilayer silicon nitride layers were known in the art and that a POSA would have known of the advantages of a multilayer approach and would have been motivated to use that approach in view of its advantages. *Id.* at 18–19. In the Rehearing Decision, we rejected Patent Owner's argument that the Institution Decision introduced a new ground not asserted in the Petition. We stated: "even though SST 1987[16] is necessary to establish *prima facie* obviousness, there is no abuse of discretion or prejudice to Patent Owner because the Petition and the Decision each independently put Patent Owner on notice of the reference and the way in which it is relied upon by Petitioner and the Board." Reh'g Dec. 4.

Patent Owner argues that Watatani does not disclose a multilayer silicon nitride etch stop and that, by relying on SST 1987, the Institution Decision improperly expanded the ground of unpatentability asserted in the Petition. PO Resp. 54–60. In addition, Patent Owner challenges the sufficiency of the evidence to establish motivation and a reasonable expectation of success for forming Tanaka I's HCD-SiN etch stop as a multilayer structure. *Id.* at 60–68.

---

[16] *Continuous Process CVD System*, Solid State Technology, October 1987, Ex. 1008 ("SST 1987").

Patent Owner does not dispute Petitioner's contention that multilayer silicon nitride layers were known in the prior art. Pet. 15–16, 20, 39, 54 (citing Ex.1003 ¶¶ 45–47, 105–107; Ex. 1008, 1-1, 2-1, Fig. 2; Ex. 1010[17]). Petitioner directs us to persuasive evidence, including Dr. Fair's testimony that a POSA "would have long known of equipment and techniques to deposit silicon nitride layers using a multilayer deposition technique." Ex. 1003 ¶ 45 (citing Ex. 1008, 1). Dr. Fair relies on SST 1987, which describes the Novellus Concept One Chemical Vapor Deposition (CVD) system. Ex. 1008, 1-1. According to SST 1987, the process chamber of the Concept One has eight stations, seven of which are used for depositing films on a wafer. *Id.* SST 1987 discloses that the Concept One enables "a new approach to chemical vapor deposition, in which every wafer that cycles through the system stops at each of the seven deposition stations to receive one seventh of its preprogrammed film thickness." *Id.* Petitioner's contention is also supported by Wang, which discloses a multilayer silicon nitride deposition method and a multilayer silicon nitride layer. Ex. 1010, title, 11:8–18.

Dr. Bottoms agrees that SST 1987 "discloses depositing SiN films using seven consecutive deposition steps." Ex. 2008 ¶ 163. Dr. Bottoms does not dispute Dr. Fair's testimony that the Concept One tool was widely used in the semiconductor industry in the 1980s and 1990s. Ex. 1003 ¶ 45. In fact, Dr. Bottoms testifies that he is familiar with multi-station deposition systems, including the Novellus Concept One, and managed a group that developed a precursor machine that was "introduced in the early 1980's" and

[17] Wang et al., US 6,017,791, issued January 25, 2000 ("Wang").

"designed to sputter deposit films in a multi-station vacuum chamber." Ex. 2008 ¶ 148 (discussing the Varian 3180).

Petitioner and Dr. Fair direct us to substantial evidence that it was known in the art to use multilayer silicon nitride layers as an etch stop layer in copper damascene interconnect structures. Pet. Sur-Sur-Reply 3; Ex. 1017 ¶ 33; Ex. 1023 (Yota),[18] 1-2. Yota discloses silicon nitride films for use as etch stop layers in copper damascene architectures and compares films deposited by high-density plasma ("HDP") CVD with films deposited by plasma-enhanced CVD ("PECVD"). *Id.*, Title, Abstract. Yota reports the results of experiments in which "[t]he PECVD films were deposited in a six-station deposition system." *Id.* at 1-2. Dr. Fair testifies that "Yota . . . is prior art for the use of multilayer silicon nitride films as etching stoppers." Ex. 1017 ¶ 33.[19]

Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use a multilayer approach, as taught by SST 1987, when forming a low dielectric constant silicon nitride etch stop layer, as taught by Tanaka I, and would have had a reasonable expectation of

---

[18] J. Yota, et al., *Comparison between HDP CVD and PECVD Silicon Nitride for Advanced Interconnect Applications*, Proc. of the IEEE 2000 Int'l Interconnect Tech. Conf. (2000) ("Yota"). Yota was submitted with Petitioner's Reply. Patent Owner requested and received the opportunity to file a sur-reply and declaration testimony responding to Yota. PO Sur-Reply 6–7; Ex. 2014, 2; Ex. 2015 ¶¶ 16–18.

[19] In view of our finding that multilayer silicon nitride etch stop layers were known in the prior art, as evidenced by Dr. Fair's testimony, Dr. Bottoms' testimony, SST 1987, and Yota, it is unnecessary to address Petitioner's contention that Watatani discloses an etch stop layer that includes three or more layers of silicon nitride. Pet. 39, 54; Pet. Reply 19–20.

success in achieving the subject matter of claims 2 and 7. Pet. 16, 20, 40–41, 55 (citing Ex. 1003 ¶¶ 46, 47, 106–109, 143; Ex. 1008, 2-2; Ex. 1010, 11:8–18); *see also* Ex. 1003 ¶¶ 156, 157. Petitioner's evidence shows two motivations for a multilayer structure: (1) improved film uniformity, and (2) improved dielectric properties by avoiding pinholes. Pet. 40–41. We discuss each of these motivations below:

First, Petitioner presents the undisputed testimony of Dr. Fair establishing that a POSA would have known that forming silicon nitride layers in a multi-layer fashion was advantageous because this approach produced more uniform thin films. Ex. 1003 ¶¶ 46, 106, 108, 143, 156 (citing Ex. 1008, 2-1). Dr. Fair's testimony is supported by 1987 SST, which describes uniformity as an "inherent benefit[]" of a multilayer deposition process using the Novellus Concept One CVD tool. Ex. 1008, 2-1. The article explains: "Within wafer *uniformity is improved* because deposition anomalies at any individual [deposition] station are averaged out, while at the output end wafer-to-wafer variations are significantly reduced because of the overall averaging effect of the process." *Id.* (emphasis added). The undisputed testimony of Dr. Fair further establishes that "[s]uch film uniformity is important in an etch stop layer, as non-uniform thin regions are prone to unintended 'punch through.'" Ex. 1003 ¶ 46. Patent Owner and Dr. Bottoms do not disagree that a POSA "would have been motivated to 'improve the uniformity' of etch stop layers by using the Novellus Concept One system described in the SST 1987 article" to deposit multiple layers of the same material. PO Resp. 63; Ex. 2008 ¶ 149.

Second, Petitioner presents credible testimony of Dr. Fair establishing that a desire for improved dielectric properties would have motivated the use

of a multilayer silicon nitride film. Ex. 1003 ¶¶ 47, 107, 108, 156 (citing Ex. 1010, 11:8–18). According to Dr. Fair, "it was known in the prior art that forming a multilayer silicon nitride layer comprising at least two layers of silicon nitride on which a silicon oxide layer is formed, one could avoid 'pinholes formed completely through the silicon nitride/silicon oxide (NO) layer,' which avoids 'degraded dielectric properties' of the dielectric layers." Ex. 1003 ¶ 47 (quoting Ex. 1010, 11:8–18).

Dr. Fair's testimony is supported by Wang, which discloses forming a multilayer silicon nitride layer by CVD on a silicon oxide layer, which is then thermally oxidized to form a silicon nitride/silicon oxide (NO) layer. Ex. 1010, 10:5–48, 11:8–35, 11:46–56, Fig. 2. Wang discloses an advantage of multilayer deposition as follows:

> [W]hen employing the multilayer silicon nitride layer formed from the first silicon nitride layer 36a and the second silicon nitride layer 36b to subsequently form from the multilayer silicon nitride layer a silicon nitride/silicon oxide (NO) layer through a thermal oxidation method, there is avoided pinholes formed completely through the silicon nitride/silicon oxide (NO) layer, which pinholes would otherwise contribute to degraded dielectric properties of the silicon nitride/ silicon oxide (NO) dielectric layer . . . .

Id. at 11:8–18. Although Wang does not relate to etch stop layers, Dr. Fair testifies that pinholes are undesirable in etch stop layers, explaining that pinholes can "function as localized defects that can alter the etch rate at individual points of an etch stop layer." Ex. 1003 ¶ 156. Dr. Fair's testimony is consistent with SST 1998, which shows that the absence of pinholes is important for silicon nitride etch stop layers for copper damascene interconnect structures. SST 1998 teaches that silicon nitride

etch stop layers must be "pinhole-free so that its diffusion barrier properties are not compromised." Ex. 1007, 2-1.

Turning to the issue of reasonable expectation of success, Petitioner directs us to the following testimony of Dr. Fair, which we find persuasive:

> A person of ordinary skill in the art would also have had a reasonable expectation of success in depositing Tanaka's low-k silicon nitride film as a series of multiple layers in the prior art dual damascene structure of Watatani, because devices designed to create multilayer etch stops were available in the prior art, and the use of a multilayer silicon nitride etch stop for this purpose was widely known in the prior art.

Ex. 1003 ¶ 109 (citing Ex. 1010, 11:8–18); *see* Pet. 41; *see also* Ex. 1003 ¶ 157 ("Because the multilayer deposition technique and its benefits was widely known in the prior art, and because the Novellus Concept One was broadly available commercially, a person of ordinary skill in the art would have had a reasonable expectation of success in depositing Tanaka's low-k silicon nitride film as a series of multiple layers in the prior art dual damascene structure of Watatani." (citing Ex. 1008, 2, Fig. 2)). Dr. Fair's testimony is supported by SST 1987, which discloses a seven-station CVD system for sequentially depositing multiple layers of a dielectric film, such as silicon nitride. Ex. 1008, 1-1. Dr. Fair's testimony is consistent with Yota, which discloses depositing a silicon nitride etch stop layer using a six-station sequential deposition system. Ex. 1023, 1-2; *see* Pet. Sur-Sur-Reply 3 (citing Ex. 1023, 1-2).

We are also persuaded by Dr. Fair's testimony that "a person of ordinary skill in the art would have had a reasonable expectation of success at keeping the dielectric constant below 5.5 when employing a multilayer silicon nitride etch stop." Ex. 1017 ¶ 34; *see* Pet. Reply 26 (citing Ex. 1017

¶ 34); *see also* Pet. Sur-Sur-Reply 4 (discussing Dr. Fair's testimony regarding dielectric constant of multilayer silicon nitride film). Dr. Fair provides a credible technical explanation for his opinion: "when stacking very thin layers to form a multilayer film, the dielectric constant can remain lower than a single layer film of the same overall thickness because of the interactions of the interfacial layers and the bulk properties of the thin layers." *Id.* ¶ 35. As further discussed below, Dr. Bottoms provides no credible rebuttal to Dr. Fair's opinion, which is consistent with Dr. Bottoms' testimony regarding a POSA's understanding about the relationship between multiple thin layers, density, and dielectric constant. Ex. 2008 ¶ 40.

We turn now to Patent Owner's arguments, starting with the procedural challenge to our Institution Decision. PO Resp. 56–60.[20] Patent Owner is correct that the Petition controls the scope of an *inter partes* review. PO Resp. 56 (citing *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348 (2018) and 35 U.S.C. § 311(a)); *see also Sirona Dental Sys. GmbH v. Institut Straumann AG*, 892 F.3d 1349, 1356 (Fed. Cir. 2018) ("It would . . . not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory."). We have complied with that requirement. Our Institution Decision (and this final decision) rely on SST 1987 in the *same way* as it was relied upon in the Petition: as evidence that multilayer silicon nitride layers were known in the prior art. Dec. 18–19. We disagree with Patent Owner's assertion that "Petitioner relies exclusively on teachings of

[20] Because we do not rely on Watatani to teach a multilayer silicon nitride etch stop layer, we do not need to address Patent Owner's argument that this feature is not disclosed by Watatani (PO Resp. 54–56) or Patent Owner's related arguments regarding lack of motivation (*id.* at 61, 63) and defeating the purpose of Watatani's structure (*id.* at 67–68).

Watatani to disclose the multilayer silicon nitride etch stop structure required by claims 2 and 7." PO Resp. 57. The Petition plainly relies on SST 1987 (in addition to Watatani) for this teaching. Pet. 15–16, 20, 39–41, 53–55. Petitioner's arguments regarding motivation and reasonable expectation of success apply to "the multilayer approach," including the multilayer deposition technique of SST 1987. Pet. 40–41, 55. We agree with Petitioner that the statements in the Petition regarding the benefits of a multilayer silicon nitride etch stop "are clearly not in reference to Watatani's specific approach (to the extent it is different), but to the general understanding in the art of using a multilayer etch stop as evidenced by, e.g., the SST 1987 reference." Pet. Reply 23 (citing Pet. 40–41). The fact that SST 1987 was not listed alongside Watatani and Tanaka I in the summary of the ground (Pet. 4) or section heading (Pet. 29) does not mean it was not part of the ground of unpatentability asserted in the Petition. Patent Owner's counterargument elevates form over substance.

Patent Owner relies on *In re NuVasive, Inc.*, 841 F.3d 966 (Fed. Cir. 2016)—*see* PO Resp. 60—but that case is distinguishable. In *NuVasive*, the court held that patent owner was not given an adequate notice and opportunity to respond to the Board's assertions of fact regarding a prior art reference. 841 F.3d at 970–73 (citing the Administrative Procedure Act ("APA"), 5 U.S.C. § 706). The reference in *NuVasive* was relied upon for a particular claim element for the first time in petitioner's reply, and patent owner was not given an opportunity to file a sur-reply or even to address the point in the oral hearing. *Id.* at 973. In contrast to *NuVasive*, Patent Owner in this case was given notice and an opportunity to respond to Petitioner's and the Board's assertions of fact regarding SST 1987. Notice was given in

the Petition, the Institution Decision, and the Rehearing Decision, all of which expressly rely upon SST 1987 to teach multilayer silicon nitride layers, and all of which were filed before the Patent Owner Response. Pet. 15–16, 20, 39–41, 53–55; Dec. 18–19; Reh'g Dec. 3–4. Moreover, Patent Owner concedes that it had adequate notice and an opportunity to respond to Petitioner's arguments based on SST 1987 and the Novellus Concept One CVD system. Tr. 25:15–24. Accordingly, there is no APA concern here, and *NuVasive* is not applicable.

Next, Patent Owner challenges the sufficiency of Petitioner's evidence of motivation and reasonable expectation of success, arguing "Wang does not provide any certainty that a multilayered structure would eliminate pinholes in the claimed device." PO Resp. 62. Patent Owner's argument is inconsistent with the legal standard for a reasonable expectation of success, which does not require certainty of success. *In re Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165. In addition, we agree with Petitioner that Patent Owner's argument is contrary to the express disclosures of Wang and Dr. Fair's testimony that the benefit of reducing pinholes was well known in the art. Pet. Reply 24 (citing Ex. 1010, 11:8–25; Ex. 1003 ¶¶ 106–108).

Next, Patent Owner argues that Wang's multilayer deposition method requires a purge step that is not described by SST 1987 and, "given this difference in the process," the multilayer structure of the Novellus Concept One might not eliminate pinholes. PO Resp. 62. We agree with Petitioner that the express teachings of one reference do not need to be reiterated by all references in order to show motivation. Pet. Reply 24–25. Even if the advantages described by Wang and SST 1987 were mutually exclusive, they

each independently provide a motivation for a multilayer structure. Ex. 1008, 2-1 (improved uniformity); Ex. 1010, 11:8–18 (avoiding pinholes).

Next, Patent Owner argues that Petitioner does not establish that the dielectric constant of Tanaka I's HCD-SiN material would remain below 5.5 if it was deposited as a series of multiple layers. PO Resp. 64. As support for this argument, Patent Owner directs us to Dr. Fair's admittedly erroneous testimony regarding Figure 17 of Tanaka II and what it shows about the relationship between thickness and dielectric constant for silicon nitride layers. *Id.* at 64–65 (citing Ex. 1003 ¶¶ 44, 55, 109, 156; Ex. 1013, 5, Fig. 17; Ex. 2009, 16:7–25, 17:11–18:7, 19:6–21, 21:20–22:18). In our view, Dr. Fair's admitted error does not support Patent Owner's argument, nor does it warrant discrediting Dr. Fair's testimony about reasonable expectation of success. Dr. Fair corrected his testimony in response to Patent Owner's deposition questions (Ex. 2009, 16:7–22:18), and, according to Patent Owner, "Dr. Bottoms agrees with Dr. Fair's deposition testimony." PO Resp. 65 (citing Ex. 2008 ¶ 152). The experts agree that, in Tanaka II Figure 17, the dielectric constant was the same (5.4) or assumed to be the same for all reported thicknesses of HCD-SiN. Ex. 2008 ¶ 152; Ex. 2009, 17:16–18:7. The experts' agreement on this point does not undermine Dr. Fair's opinion that a POSA "would have had a reasonable expectation of success at keeping the dielectric constant below 5.5 when employing a multilayer silicon nitride etch stop." Ex. 1017 ¶ 34.

Next, Patent Owner argues that applying thin layers of Tanaka I's HCD-SiN may allow hydrogen and chlorine impurities to diffuse out of the HCD-SiN, resulting in an increased dielectric constant. PO Resp. 66. As it

pertains to hydrogen impurities, that argument is not persuasive in view of the inconsistent positions taken by Patent Owner and Dr. Bottoms regarding the effects of hydrogen impurities on the dielectric constant of SiN films. On the one hand, Patent Owner and Dr. Bottoms assert that diffusion of hydrogen and chlorine out of Tanaka I's HCD-SiN material would increase the dielectric constant of the material because hydrogen and chlorine "impurities are likely a reason for the *decreased* dielectric constant" of Tanaka I's HCD-SiN material. *Id.* (emphasis added); Ex. 2008 ¶ 163 (same). On the other hand, Patent Owner and Dr. Bottoms assert that, "[r]educing hydrogen can have the effect of lowering the dielectric constant of silicon nitride because hydrogen impurities in silicon nitride can *increase* the dielectric constant of the material." *Id.* at 14 (emphasis added); Ex. 2008 ¶ 60 (same). We thus agree with Petitioner that Patent Owner "contradicts itself." Pet. Reply 25.

We also agree with Petitioner that Patent Owner's argument, as it pertains to chlorine impurities, is contradicted by Tanaka I, which discloses that "Cl was not detected over the detection limit up to 1000 C, and is concluded to be thermally stable." Ex. 1006, 1-2; Pet. Reply 25–26 (citing Ex. 1017 ¶ 34). There is no persuasive rebuttal to the cited testimony of Dr. Fair that a POSA "would have understood that chlorine would not diffuse out as alleged by Dr. Bottoms." Ex. 1017 ¶ 34. Moreover, aside from the unsubstantiated and speculative opinion of Dr. Bottoms (Ex. 2008 ¶ 163), Patent Owner does not direct us to persuasive evidence that hydrogen or chlorine impurities would diffuse out of silicon nitride when applied as thin layers.

Next, Patent Owner argues that "it would be understood that depositing multiple layers would increase the density of the film" and "[b]y increasing the density, the dielectric constant of the resulting film might be increased." PO Resp. 66 (citing Ex. 2008 ¶ 163). Patent Owner's argument is persuasively rebutted by Dr. Fair's testimony that a multilayer film can have a lower dielectric constant than a single layer film of the same overall thickness. Ex. 1017 ¶ 35; *see* Pet. Reply 26 (relying on Dr. Fair's testimony). As noted by Petitioner, Patent Owner's argument is inconsistent with Patent Owner's assertion in the '330 patent that multilayer deposition is one way to reduce the dielectric constant of a silicon nitride etch stop layer. Pet. Sur-Sur-Reply 4; Ex. 1001, 5:63–6:7.

Patent Owner's argument is also contradicted by Dr. Bottoms' testimony regarding a POSA's understanding of the '330 patent's teachings about multilayer depositions. The '330 patent teaches that "multi-layer depositions . . . eliminates pinholes and produces a *denser film*." Ex. 1001, 6:3–4 (emphasis added). Dr. Bottoms testifies that, as understood by a POSA, "this means that the material overall may be *less dense* because it includes voids or chemical impurities." Ex. 2008 ¶ 40 (emphasis added). In other words, Dr. Bottoms testifies that a POSA would understand the '330 patent to teach that multilayer deposition produces a film that is less dense overall than single layer deposition. Patent Owner's argument that depositing multiple layers would increase the density of the film (PO Resp. 66) is thus contradicted by Dr. Bottoms' testimony about how a POSA would understand the teachings of the '330 patent (Ex. 2008 ¶ 40).

Patent Owner's argument is also contradicted by the teachings of Yota, and Dr. Bottoms' interpretation of those teachings. Yota discloses that

a multilayer PECVD deposition process produced a lower density silicon nitride film than a single layer HDP CVD deposition process. Ex. 1023, 1-1, 1-2, 2-2, 3-2 (showing a multilayer PECVD process produced a less dense film than the HDP CVD process); *see also* Ex. 2015 ¶ 16 (Yota's HDP CVP silicon nitride process "would be understood to form a single layer of material"); *id.* ¶ 17 ("Yota reports a lower dielectric constant for the multi-layered PECVD film.").

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 2 and 7 of the '330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

3. Claims 5 and 10

Claim 5 depends from claim 1 and recites "wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof." Claim 10 depends from claim 6 and recites "wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof."

Petitioner directs us to substantial evidence that Watatani discloses the limitations of claims 5 and 10 by disclosing conductor cores comprising copper. Pet. 41–42, 56 (citing Ex.1005, 2:1–5, 2:42–47). Patent Owner does not contest that evidence and submits no arguments regarding claims 5 and 10 separately from its arguments regarding claims 1 and 6. We determine that Petitioner has demonstrated by a preponderance of the evidence that the limitations of claims 5 and 10 are disclosed by Watatani.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 5 and 10 of the '330 patent are unpatentable as obvious in view of Watatani and Tanaka I.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 1, 2, 5–7, and 10 of the '330 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01566
Patent 6,388,330 B1

PETITIONER:

Jeremy Jason Lang
Jared Bobrow
ORRICK, HERRINGTON & SUTCLIFFE LLP
PTABDocketJJL2@orrick.com
PTABDocketJ3B3@orrick.com

PATENT OWNER:

Timothy P. Maloney
Nicholas T. Peters
David Gosse
FITCH, EVEN, TABIN & FLANNERY LLP
tim@fitcheven.com
ntpete@fitcheven.com
dgosse@fitcheven.com