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Paper 31
Entered: February 13, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2017-00116
Patent 7,334,150 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–3, 5, 6, and 8–11 ("challenged patents") of U.S. Patent No. 7,334,150 B2 (Ex. 1001, "the '150 Patent"). Paper 2

("Pet."). In support of its Petition, Petitioner proffers a Declaration of Dr. Vivek Subramanian. Ex. 1011. Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Upon consideration of the parties' contentions and supporting evidence, we instituted an *inter partes* review pursuant to 35 U.S.C. § 314, as to claims 1–3, 5, 6, and 8–11 of the '150 Patent. Paper 9 ("Dec.").

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 17, "PO Resp."). In support of its Patent Owner Response, Patent Owner proffers the Declaration of Dr. Joseph Bernstein. Ex. 2019. Petitioner filed a Reply to Patent Owner's Response (Paper 20, "Pet. Reply"). On December 6, 2017, we held an oral hearing. Paper 30 ("Tr.").

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3, 5, 6, and 8–11 of the '150 Patent are unpatentable.

A. Related Matters

The parties state that the '150 Patent is the subject of a pending lawsuit in the Central District of California, i.e., *Polaris Innovations Ltd. v. Kingston Tech. Co.*, Case No. 8:16–cv-300 (C.D. Cal.),[1] and the lawsuit includes assertions against Petitioner. Pet. 2; Paper 3 (Patent Owner's Mandatory Notices), 1; Paper 16 (Patent Owner's Supplemental Mandatory Notices).

[1] This lawsuit is referred to herein as the "companion district court lawsuit."

B. The ’150 Patent

The ’150 Patent is directed to a semiconductor memory module that includes a register circuit and a clock signal regeneration circuit. Ex. 1001, 1:9–16. Figure 2 is reproduced below.

FIG 2

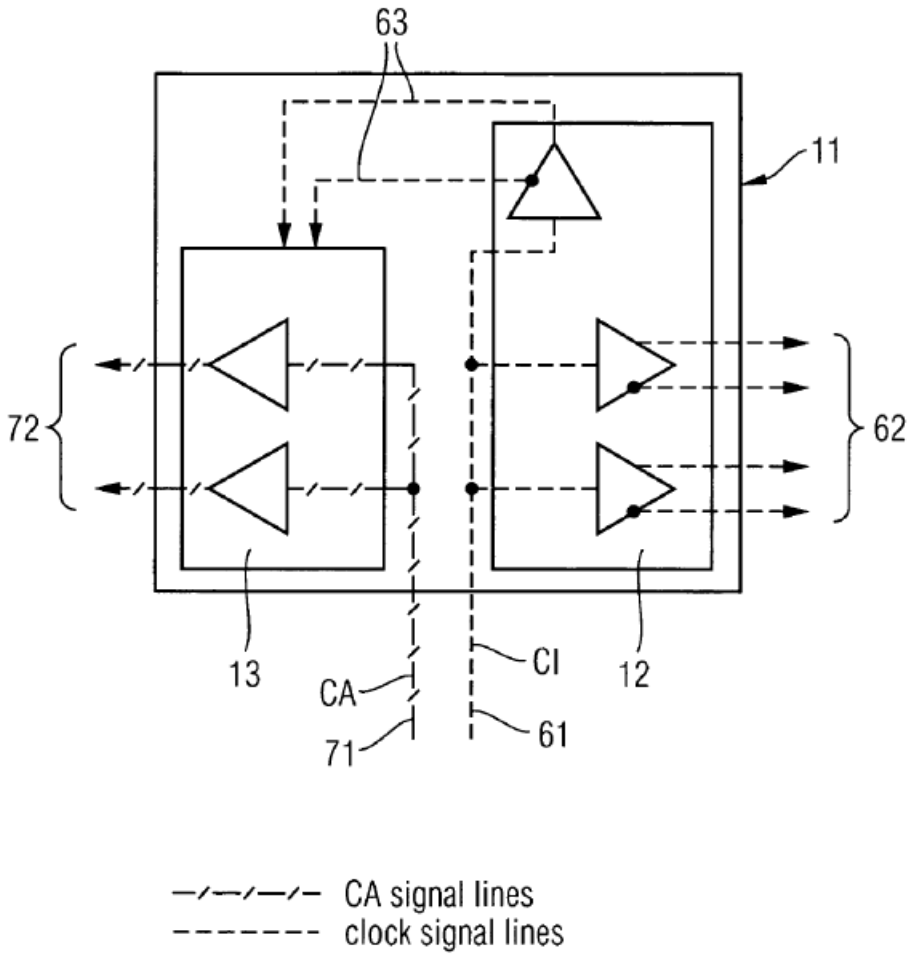

Figure 2 shows a top view of a clock signal regeneration circuit and register circuit in a common chip packing.

As shown in Figure 2 above, chip packing 11 contains clock signal regeneration circuit 12 and register circuit 13. Ex. 1001, 4:30–33. Differential clock signal input line 61 supplies clock signal Cl to common chip packing 11. *Id.* at 4:41–43. Line section 71 supplies command and address input signals "CA." *Id.* at 4:43–45. Differential clock signal lines 62 from clock signal regeneration circuit 12 supply the conditioned clock signal to memory chips 4 and 4*a*. *Id.* at 4:49–53. Differential clock signal lines 63 supply the conditioned clock signal to register circuit 13. *Id.* at 4:54–56. From register circuit 13, temporarily stored command and address signals are supplied by differential command and address signal lines 72 to memory chips 4 and 4*a*. *Id.* at 4:56–60.

C. Illustrative Claim

Petitioner challenges claims 1–3, 5, 6, and 8–11 of the '150 Patent. Claim 1 is an independent claim. Claims 2, 3, 5, 6, and 8–11 depend directly from claim 1. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory module comprising:
>
> a plurality of memory chips arranged on the memory module;
>
> a plurality of bus signal lines operable to supply an incoming clock signal and incoming command and address signals to at least the memory chips;
>
> a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having a same frequency as the incoming clock signal; and
>
> a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock

> signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

Id. at 7:1–25.

D. Instituted Grounds of Unpatentability

Petitioner asserts that claims 1–3, 5, 6, and 8–11 are unpatentable based on the following grounds (Pet. 4):

Reference(s)	**Basis**	**Challenged Claim(s)**
Lee[2]	§ 103(a)	1, 2, 5, 6, and 8–10
Lee and Keeth	§ 103(a)	3 and 11
Dodd[3]	§ 103(a)	1, 2, 5, 6, and 8–10
Dodd and Keeth[4]	§ 103(a)	3 and 11

We instituted on all of the asserted grounds of unpatentability above. Dec. 33.

[2] U.S. Patent No. 6,898,726 B1, issued May 24, 2005 (Ex. 1008) ("Lee").
[3] U.S. Patent No. 6,530,006 B1, issued Mar. 4, 2003 (Ex. 1003) ("Dodd").
[4] U.S. Patent No. 7,123,046 B2, issue Oct. 17, 2006 (Ex. 1016) ("Keeth").

II. DISCUSSION

A. Overview

A patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Person of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art had a Master's degree in Electrical Engineering and at least 2 years' experience working in the field of semiconductor memory design. Pet. 7 (citing Ex. 1011 ¶¶ 17–19). Patent Owner counters that the person of ordinary skill in the art "would only have had a Bachelor's degree, or the equivalent, in the art of semiconductor memory module design." PO Resp. 4–5 (citing Ex. 2019 ¶¶ 24–30).

The dispute centers on Patent Owner's contention that a person of ordinary skill would have lacked familiarity with components of memory modules and technical differences between RDIMMs and other memory modules, and further would have had ordinary creativity that "coexisted" with "his or her status" as a "junior member of the team." *Id.* Patent Owner's contention regarding the lack of familiarity of the skilled artisan with prior art teachings, e.g., technical differences between RDIMMs and other memory modules, is contrary to legal precedent that a person of ordinary skill in the art is presumed to be aware of all pertinent prior art. *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 454 (Fed. Cir. 1985).

Regarding the level of skill, we consider the level of skill implied by the disclosures of the prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of skill in the art). For the reasons given below, upon consideration of the Petition, the Patent Owner Response, the Petitioner's Reply, and the evidence cited therein, we adopt Petitioner's proposed level of skill as consistent with the evidence of record. We credit Dr. Subramanian's testimony regarding level of skill as consistent with the evidence of record, including the disclosures of the prior art references and the level of skill implied by these disclosures. We, however, note that based on the complete trial record, our findings and conclusion would be the same under either proposal.

C. Claim Construction

Petitioner provides proposed constructions for certain terms. Pet. 12–17. In Patent Owner's Preliminary Response, Patent Owner countered and presented additional contentions regarding claim construction. *See, e.g.*,

Prelim. Resp. 4–32. In our Institution Decision, we determined that neither "clock signal regeneration circuit" nor "a register . . . configured to . . . generate a plurality of copies of the incoming command and address signals" invokes § 112 ¶ 6.[5] Dec. 7–9. We further determined that no express interpretation was necessary of these phrases. *Id.* We also were not persuaded that Petitioner should be held to previous arguments in the companion district court lawsuit that claim 6 is indefinite. *Id.* at 9. The parties do not challenge the determinations in the Institution Decision. *See e.g.*, PO Resp 43–62; Pet. Reply 14–22. Based on the entire trial record before us, we see no need to change these determinations.

In our Institution Decision, we also made determinations regarding the terms "having a same frequency" and "RDIMM." *Id.* at 10–12. Patent Owner's disputes in its Patent Owner Response implicitly pertain to the construction of these terms, so we provide further analysis regarding construction of these terms below.

1. "having a same frequency"

In the Petition, Petitioner contends that "having a same frequency" means "with no intended modification from the frequency of the incoming signal." Pet. 13–16. In the Institution Decision, we considered Patent Owner's contention that "intended" interjects a vague term and should be

[5] Section 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA") re-designated 35 U.S.C. § 112 ¶ 6, as 35 U.S.C. § 112(f). Because the '150 Patent has a filing date before September 16, 2012, the effective date of § 4(c) of the AIA, we will refer to the pre-AIA version of 35 U.S.C. § 112.

removed from Petitioner's proposed construction. Dec. 10–12 (citing Prelim. Resp. 28–31).

At the institution stage, we did not adopt the proposal of either party. We noted that "same frequency" is within larger phrases recited in independent claim 1. Dec. 11–12. We declined to construe the phrase "having a same frequency" such that both the generated copies and the copies supplied are required to be at the same frequency as the incoming signals. We explained that our determination was based on embodiments set forth in the '150 Patent Specification. *Id.* (citing Ex. 1001, 2:57–59, 3:61–63). We further determined no other express construction of the term "same frequency" is needed to resolve a dispute between the parties.

In its Patent Owner Response, Patent Owner contends "Lee's WCLK/2 signal operates at a different frequency from WCLK, so it cannot be a 'copy' of the WCLK having the same frequency as WCLK, as claimed." PO Resp. 45. Patent Owner's contentions in its Patent Owner Response pertain to only the "signal WCLK/2" that is supplied to register 45. *Id.* at 43–47. In particular, claim 1 recites "a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and *configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit*." Ex. 1001, 7:14–18 (emphases added). Patent Owner's contentions are premised on "one of *the copies of the incoming clock signal*" having antecedent basis in "the copies of the incoming clock signal having a same frequency as the incoming clock signal." *Id.*

Petitioner contends that the "clock signal regeneration circuit" limitation requires only the copies supplied to the memory chips to "hav[e] a

same frequency as the incoming clock signal," and that the omission of that language from the "register circuit" limitation indicates that the copy of the incoming clock signal that the register circuit is configured to receive need not have the same frequency as the incoming clock signal. Reply 15–16. According to Petitioner, "each and every one of the 'same frequency' copies that are generated by the clock signal regeneration circuit are supplied to the memory chips." Reply 15; Pet. 43–48. Petitioner further contends that "the register simply needs to be 'configured to,' i.e., able to receive a copy of the clock signal" and, "[a]s long as the register is so configured, the claim limitation is met regardless of whether the copy of incoming signal sent to the register has the same frequency or not." Reply 16–17.

Upon consideration, consistent with Petitioner's proposal, we are persuaded that the "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips" must have the same frequency as the incoming clock signal. We are not persuaded that the "one of the copies" that the register circuit is configured to receive must have the same frequency as the incoming clock signal as argued by the Patent Owner. Our determination is consistent with the express recitations in claim 1 and the intrinsic evidence. For instance, the recitation of "having a same frequency" in claim 1 immediately follows the supply of signals to the memory chips.

> a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and *to supply the copies* of the incoming clock signal *to the memory chips*, the copies of the incoming clock signal *having a same frequency* as the incoming clock signal; and
>
> a register circuit arrange[d] on the memory module in a common chip packing with the clock regeneration circuit and

> configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and *supply the copies* of the incoming command and address signals *to the memory chips*, the copies of the incoming command and address signals *having a same frequency* as the incoming command and address signals.

Ex. 1001, 7:8–25 (emphases added).

Importantly, if we were to adopt Patent Owner's proposal, then the claim would require "one of the copies of the incoming clock signal from the clock regeneration circuit" received by the register circuit also be supplied to at least one of the memory chips. Upon consideration of the contentions of both parties, we are not persuaded that such an interpretation is consistent with the express language of claim 1 or the intrinsic evidence, including the '150 Patent Specification.

Furthermore, based on the entire trial record, the intrinsic evidence, including the '150 Patent Specification, supports that the "one of the copies of the incoming clock signal from the clock regeneration circuit" need not have the same frequency as the incoming clock signal. Petitioner contends (Pet. 13–15) and Patent Owner does not dispute (Prelim. Resp. 28–31; PO Resp. 43–47) that the phrase "having the same frequency" did not appear in the Specification or claims as filed, but was added by amendment. Neither party points us to disclosure in the '150 Patent Specification requiring that "having the same frequency" pertains to "one of the copies of the incoming clock signal from the clock regeneration circuit."

Additionally, as we explained in the Institution Decision (Dec. 11–12), in embodiments set forth in the '150 Patent Specification, including a

preferred embodiment, "[t]he register and clock signal regeneration circuits are, preferably, designed such that they each multiply the clock signal and the command and address signal by a factor of 1:2" (Ex. 1001, 3:61–63) such that "several" copies "can be provided to *several DRAM branches or channels*" (*id.* at 2:57–59 (emphasis added).) Additionally, the Detailed Description of the '150 Patent also describes multiplying these signals so as to supply chip-groups.

> [I]ncoming clock signal C1 is conditioned and the incoming command and address signals CA are temporarily stored in order to multiply these signals by a factor of 1:X and *to supply the conditioned clock signal C1 and the temporarily stored command and address signals CA to X semiconductor memory chip groups* that are arranged on the semiconductor memory module.

Ex. 1001, 5:67–6:6 (emphasis added).

Relying on the testimony of Dr. Bernstein and Dr. Subramanian, Patent Owner contends "when the '150 Patent states that signals are 'multiplied,' a POSITA would understand that to mean that copies of the signal are made." PO Resp. 15 n.3 (citing Ex. 2019 ¶ 65), 45 (citing Ex. 1011 ¶ 23; Ex. 2019 ¶ 66). More specifically, Dr. Bernstein testifies

> The '150 Patent makes numerous references to multiplying a signal by a factor of 1:X. *See id.* at 2:46, 2:47–51, 2:58, 6:19, 6:31. As one of ordinary skill in the art, I understand this terminology to mean that the signal is copied "X" number of times. This is clear given the overall focus of the '150 Patent on avoiding sending multiple copies of the CA signal. "Since the CA signals are multiplied by a factor of 1:X, several CA copies can be provided to several DRAM branches or channels." *Id.* at 2:57–59. The '150 Patent also uses this convention and fills in the "X" with the number "2" to describe an embodiment where two copies of signals are generated. *See id.* at 5:28–38 (describing Figure 3 illustrating two copies of by the CA line and

> the CL line). The fact that this terminology is referring to copying the incoming signal is made most evident by the statement that the register stores the CA signals "in order to multiply these signals by a factor of 1:X and to supply the conditioned clock signal Cl and the temporarily stored command and address signals CA to X semiconductor memory chip groups arranged on the semiconductor memory module." *Id.* at 6:2–6. This confirms that "X" in this notation means the number of copies that need to be made in order to send the signal to "X" groups of semiconductor chips. To be clear I find no suggestion that 1:X refers to multiplying the frequency of the signal X.

Ex. 2019 ¶ 66.[6]

As set forth above, Dr. Bernstein testifies that the '150 Patent Specification describes multiplying signals, which means that the signals are copied, so as to supply signals to "several DRAM branches or channels" or "to supply the conditioned clock signal Cl and the temporarily stored command and address signals CA to X semiconductor memory chip groups arranged on the semiconductor memory module." *Id.* (citing Ex. 1001, 2:57–59, 6:2–6). These embodiments (*id.*), however, are consistent with Petitioner's contentions regarding the scope of claim 1 (Reply 15; Pet. 43–48). Patent Owner does not point us to testimony of Dr. Bernstein indicating that claim 1 does not encompass these embodiments. Dr. Bernstein's testimony regarding finding "no suggestion that 1:X refers to multiplying the

[6] Patent Owner includes only cursory statements and a citation to this testimony by Dr. Bernstein. *See* PO Resp. 15 n.3 (citing Ex. 2019 ¶ 65), 45 (citing Ex. 1011 ¶ 23; Ex. 2019 ¶ 66 ("Dr. Subramanian and Dr. Bernstein agree that when the '150 Patent states that signals are "multiplied," a POSITA would understand that to mean that copies of the signals are made.") The Patent Owner Response must include "a detailed explanation of the significance of the evidence." *See* 37 C.F.R. §§ 42.22, 42.23, 42.120. Such detailed explanation is not provided.

frequency of the signal" immediately follows and pertains to his testimony regarding sending or supplying signals "to 'X' groups of semiconductor chips." Ex. 2019 ¶ 66. We find Dr. Bernstein's testimony consistent with our determination in the Institution Decision that only "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips" must have the same frequency as the incoming clock signal.

Patent Owner also relies on the declaration testimony and deposition testimony of Dr. Subramanian. PO Resp. 43–45 (citing Ex. 1011 ¶ 23; Ex. 2018, 126:1–23). We do not find either supports Patent Owner's position. Dr. Subramanian's deposition testimony in this regard refers to "the limitation above" and does not include further explanation. Ex. 2018, 126:1–23. The limitation above recites the "clock signal regeneration circuit configured to . . . supply the copies of the incoming clock signal to the memory chips." Ex. 1001, 7:8–18. Additionally, Dr. Subramanian's declaration testimony is based on his analysis of the intrinsic evidence, including the '150 Patent Specification. *See, e.g.*, Ex. 1011 ¶¶ 23, 29, 30, 72–80. As discussed further below, Dr. Subramanian discusses the intrinsic evidence and claim construction and concludes that Lee discloses the register circuit "configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit." Ex. 2018, 126:1–23.

For this Decision, we discern no reason to modify our analysis or our claim construction determination set forth in the Institution Decision regarding "having a same frequency." Based on the entire trial record, we determine that only "the copies of the incoming clock signal" that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory

chips" must have the same frequency as the incoming clock signal. We, however, determine that the broadest reasonable interpretation of the "register circuit" limitation does not require that the "one of the copies of the incoming clock signal from the clock regeneration circuit" received by the register circuit has the same frequency as the incoming clock signal.

2. "RDIMM"

Petitioner contends that "RDIMM" stands for registered dual in line memory module. Pet. 17. Dr. Subramanian testifies that although "[t]he term 'RDIMM' appears twice" in the '150 Patent Specification, neither of these uses "defines or limits the meaning of the term 'RDIMM.'" Ex. 1011 ¶ 31. Dr. Subramanian also testifies that a RDIMM "is 'a Dual In-Line Memory Module that has register circuitry to buffer control signals.'" *Id.* ¶ 32.

Patent Owner agrees that "RDIMM" stands for registered dual in line memory module and, further, agrees that RDIMM's were known prior art devices. Prelim. Resp. 48; PO Resp. 10–14, 61. Patent Owner, however, contends "RDIMMs are a well-known commercial DIMM type, which, among other things, buffers its C/A [command and address] signals, but not its data signals." PO Resp. 61 (citing a printout of a Dell Support webpage titled "PowerEdge: What are the different types of memory DIMMS for servers?" (Ex. 2034) ("**Registered DIMM**: RDIMM, buffers add, control, clock lines but does not buffer data I/O lines")). Dr. Bernstein testifies "RDIMMs feature a design that addresses performance issues . . . by putting a register between the memory controller and the memory devices on *only the command/address line*." Ex. 2019 ¶ 55 (emphasis added). Additionally, Patent Owner points to Dr. Subramanian's testimony that traditionally a

fully buffered DIMM provides buffering for control signals and data signals. PO Resp. 12 (citing Ex. 2018, 19:7–11).

As an initial matter, a Web Page from Dell's Web Site with a print date of July 10, 2017, and a last modified date of May 31, 2017, is less probative than a definition or usage contemporaneous with the filing date of December 3, 2004 of the '150 Patent. Ex. 2034. Regarding the declaration and deposition testimony identified by the parties (Ex. 1011 ¶¶ 31–32; Ex. 2019 ¶ 55; Ex. 2018, 19:7–11), we need not make a determination regarding the broadest reasonable interpretation of RDIMM because based on the entire trial record, for the reasons set forth *infra* in Section II.D.3, we are persuaded that Petitioner shows sufficiently that Lee teaches an "RDIMM" even if we were to adopt Patent Owner's proposal that RDIMM stands for registered dual in line memory module, which buffers control signals, but not data signals. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Obviousness over Lee alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee. Pet. 41–52. Petitioner also contends that claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Lee and Keeth. Pet. 52–54.

1. Overview of Lee

Lee is directed to a method for transmitting a command signal and an address signal, which includes buffering and then transmitting in response to

a clock signal and a select signal. Ex. 1007, Abstract. Figure 4 is reproduced below.

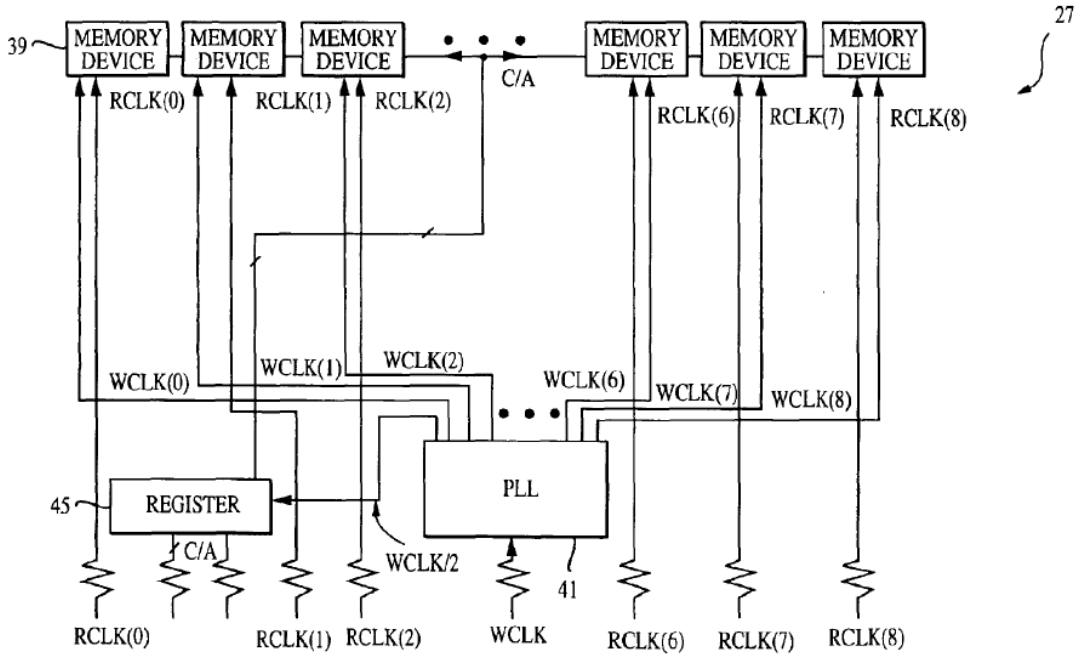

FIG. 4

Figure 4 illustrates Memory Subsystem 27

As shown in Figure 4 above, memory subsystem 27 includes write clock (WCLK) regeneration circuit 41, which is a phase lock loop (PLL) and provides WCLK (0) to WCLK (8) signals to each of individual DRAM memory devices 39. *Id.* at 7:26–30. Memory subsystem 27 also includes register 45, which receives a WCLK/2 signal from WCLK regeneration circuit 41 and command and address data (C/A). *Id.* at 7:34–41.

2. Overview of Keeth

Keeth is directed to adaptively adjusting a transition threshold of a data receiver using differential clock signals and a reference voltage. Ex. 1016, Abstract. According to Keeth, Double Data Rate Dynamic Random Access Memory (DDR DRAM) devices use differential signaling for clock

signals at clock pins of a device package. *Id.* at 1:22–30. DDR DRAM devices use non-differential signaling for data signals input on the device data pins. *Id.* at 1:35–37.

3. Discussion of Claim 1

a. The Petition—Claim 1

We begin our analysis with independent claim 1. Claim 1 is directed to a memory module comprising memory chips and bus lines operable to supply incoming clock and command and address signals to the memory chips. Ex. 1001, 7:1–7. Petitioner points to teachings relating to memory module 27. Pet. 41–48 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 69–71). Consistent with Petitioner's contentions (*id.*), Lee teaches that memory module 27 comprises memory chips 39 and bus lines (Ex. 1008, Figs. 1, 3, 4). Dr. Subramanian testifies that Lee's memory module 27 has a plurality of bus signal lines to supply incoming clock signal (WCLK) and incoming command and address signals (C/A) to memory chips 39. Ex. 1011 ¶ 71. We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (Pet. 41–48; Ex. 1011 ¶¶ 69–71), for example, because in Lee's memory system, 9 buses send signals, e.g., command and address signals and clock signals, to a plurality of memory modules 27 (Ex. 1008, 4:1–14, Figs. 1, 4). Each memory module 27 may be implemented as a DIMM. *Id.* at 6:6–21, 7:26–27. These contentions are not contested by Patent Owner. PO Resp. 43–56.

Claim 1 also recites "a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having the same frequency as the incoming clock

signal." Ex. 1001, 7:8–13. Relying on the testimony of Dr. Subramanian, Petitioner contends that Lee's PLL 41 of memory module 27 generates a plurality of copies of incoming clock signal CLK, i.e., WCLK (1–8), and supplies the copies to memory chips 39. Pet. 43 (citing Ex. 1008, 6:51–55; Fig. 4; Ex. 1011 ¶¶ 72–73). We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (*id.*) that Lee's clock signal regeneration circuit (PLL 41) generates a plurality of copies of the incoming clock signal and supplies the copies of the incoming clock signal to the memory chips because Petitioner's showing and Dr. Subramanian's testimony are consistent with Lee's teachings (*see, e.g.*, Ex. 1008, Fig. 4). Patent Owner does not dispute Petitioner's contentions that Lee's clock signal regeneration circuit (PLL 41) generates a plurality of copies of the incoming clock signal and supplies the copies of the incoming clock signal to the memory chips. PO Resp. 43–56.

Regarding the remainder of the recitation, i.e., "the copies of the incoming clock signal having a same frequency as the incoming clock signal" (Ex. 1001, 7:11–12), we discuss this recitation in connection with the next recitation of "a register circuit" that is

> configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

Id. at 7:18–25.

As discussed *supra* Section II.C.1 with respect to claim construction, in each of these phrases, we determine that the "copies of the incoming command and address signals" that the register circuit is "configured . . . to

generate . . . and supply . . . to the memory chips" must have the same frequency as the incoming signal. We, however, are not persuaded that the "one of the copies of the incoming clock signal from the clock regeneration circuit" must have the same frequency as the incoming clock signal.

Notwithstanding Patent Owner's contentions regarding this limitation, discussed further below, we are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony that Lee teaches (1) the clock signal regeneration circuit supplying copies of the incoming clock signal having a same frequency as the incoming signals; and (2) the register circuit supplying copies of the command and address signal having the same frequency as the incoming command and address signals. Pet. 43, 46–48 (citing Ex. 1008, 6:51–55, 7:35–42, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 73, 79–80). We are persuaded by Petitioner's showing and credit Dr. Subramanian's testimony (*id.*) because they are consistent with the evidence cited therein including, for example, Figure 4 of Lee reproduced below.

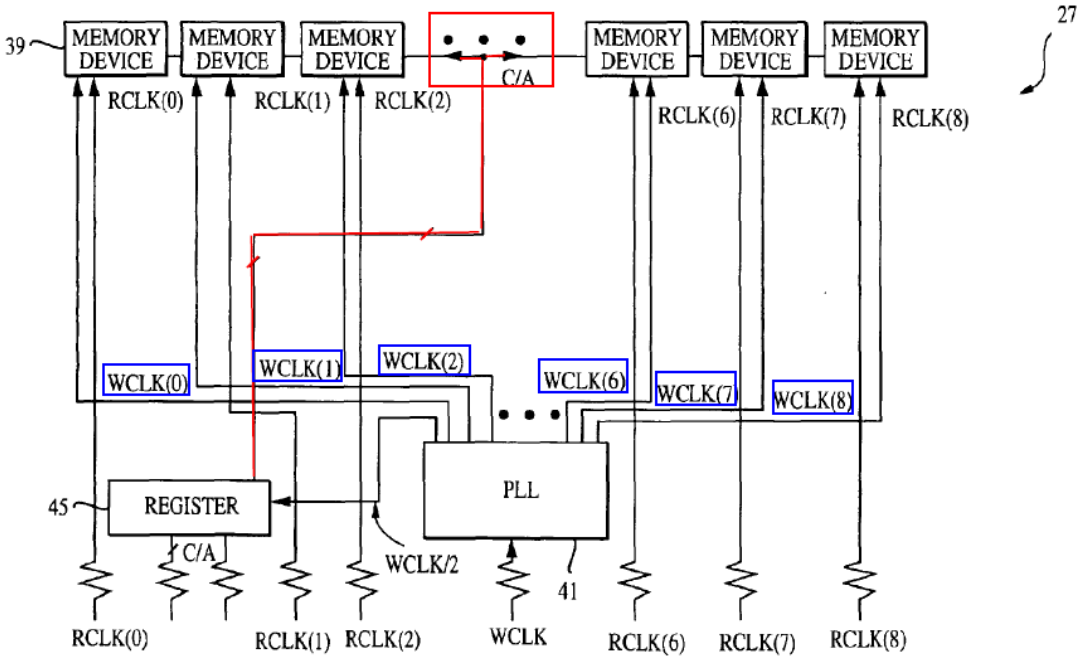

FIG. 4

Figure 4 illustrates Memory Subsystem 27 with Annotations by the Board

In the annotated version of Lee's Figure 4 reproduced above, we have added blue annotations showing copies of the incoming clock signal, i.e., WCLK(0) through WCLK (8) leaving PLL41 and red annotations showing copies of the command and address signal, i.e., C/A leaving register 45. Regarding the recitation in claim 1 of the "clock signal regeneration circuit" supplying "copies of the incoming clock signal" "having a same frequency" as the incoming signals (Ex. 1001, 7:8–12), Dr. Subramanian testifies that Lee teaches that PLL 41 generates copies of incoming clock signal, namely WCLK 1–8, and supplies those copies to memory chips 39 and that each of the copies have the same phase as input clock WCLK. Ex. 1011 ¶¶ 72, 73 (citing Ex. 1008, 6:51–55, Fig. 4). We credit Dr. Subramanian's testimony (*id.*) because it is consistent with Lee's Figure 4 illustrating PLL 41

generating WCLK (0) through WCLK (8) (shown in blue annotations in Figure 4 above) and Lee's teaching that "[p]referably the clock regeneration circuit is formed as a zero delay phase lock loop (PLL)" so as to ensure "the regenerated WCLK signals having substantially the same phase as one another and as the phase of the WCLK signal on line 19." Ex. 1008, 6:51–55, Fig. 4. Additionally, Lee teaches "the clock regeneration circuit" "receives the WCLK signal" and "provides a plurality of regenerated WCLK signals to the respective memory devices e.g., DRAMS 39, provided within memory subsystem 27" (*id.* at 6:47–55). Lee further "illustrates the WCLK regeneration circuit 41 as a (PLL) phase lock loop," which "provides the respective WCLK signals WCLK(0) . . . WCLK(8) to each of the individual DRAM memory devices 39." *Id.* at 7:26–34.

Regarding recitation in claim 1 of the "register circuit" supplying "copies of the incoming command and address signals" having the "same frequency" as the incoming command and address signals (Ex. 1001, 7:21–25), Petitioner points to Lee's teachings relating to register 45 temporarily storing command and address signals and then supplying copies of these signals to chips 39 under control of the WCLK signal. Pet. 46–48 (citing Ex. 1008, 7:35–41, 11:29–37, Fig. 4; Ex. 1003, Fig. 1; Ex. 1011 ¶¶ 78–80). Dr. Subramanian testifies that copies of the command and address signals are provided to exemplary memory devices on the left and exemplary memory devices on the right such that the supplied command and address signals have the same frequency as the incoming ones. Ex. 1011 ¶¶ 79–80 (citing *e.g*, Ex. 1008, 7:35–42, 11:29–37, Fig. 4). We credit Dr. Subramanian's testimony (*id.*) because it is consistent with Lee's teachings illustrated in Figure 4 of command and address signals, depicted as "C/A"

(shown in red annotations in Figure 4 above) being supplied to memory devices to the left and memory devices to the right. Patent Owner does not dispute Petitioner's showing, except with respect to the recitation of "to generate a plurality of copies," which we discuss below.

Claim 1, additionally, recites a register circuit arranged on the memory module in a common chip packing with the clock regeneration circuit and configured to receive copies of the clock signal from the clock regeneration circuit. Ex. 1001, 7:14–18. Petitioner points to Lee's teachings relating to module 27, comprising register 45 and PLL 41. Pet. 44–45 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76). Consistent with Petitioner's contentions (*id.*), Lee teaches that memory module 27 may be implemented as a DIMM (Ex. 1008, 6:6–21, 7:26–27) and that memory module 27 includes register 45 and PLL 41 (*id.* at Fig. 4). Patent Owner does not dispute that Lee teaches a register circuit arranged on the memory module. PO Resp. 43–56.

b. Patent Owner's Contentions—Claim 1

We turn now to Patent Owner's contentions. Patent Owner makes three arguments regarding obviousness of claim 1 over Lee as follows: (1) Lee does not teach a copy of the clock having the same frequency going to the register circuit (PO Resp. 43–47); (2) Lee does not teach a register circuit and clock circuit in a common chip packing (*id.* at 47–52); and (3) Lee does not teach a plurality of copies of the command and address signals (*id.* at 52–56).

We start with Patent Owner's first contention that Lee does not teach a copy of the clock signal having a same frequency going to the register circuit. PO Resp. 43–47. Patent Owner contends that because Figure 4 of

Lee shows a "WCLK/2" input to register 45 and "WCLK/2" is "a ***factor of two*** different from that of the incoming clock signal WCLK," Lee fails to teach that the one of the copies of the clock signal received by the register circuit has the same frequency as the incoming clock signal. PO Resp. 44–46.

Patent Owner's contention is premised on its narrow interpretation of claim 1 requiring that the "one of the copies of the incoming clock signal" that the register circuit is "configured to receive" has a same frequency as the incoming clock signal. As we discussed *supra* Section II.C.1, we reject Patent Owner's construction as inconsistent with the recitations in claim 1, in which "having a same frequency" modifies only those copies of the incoming clock signal that the clock signal regeneration circuit is "configured . . . to supply . . . to the memory chips." Additionally, we are not persuaded that Patent Owner's construction is mandated by the embodiments of the '150 Patent Specification, which instead describe multiple copies sent to multiple branches or chip-groups. Lee's teaching relied upon by Petitioner (Pet. 45) is similar to the description in the '150 Patent Specification encompassed by claim 1 as in both cases copies of signals are made to supply copies to multiple branches or groups of semiconductor chips. *Compare* Ex. 1001, 2:57–59, 3:61–64, 5:67–6:6 *with* Ex. 1008, Fig. 4.

Furthermore, Petitioner presents persuasive contentions and evidence that claim 1 is obvious over Lee even under Patent Owner's proposed interpretation. Pet. 45–48 (citing *e.g.*, Ex. 1008, 7:35–41, Fig. 4; Ex. 1011 ¶¶ 77–80). For instance, Dr. Subramanian testifies that Lee teaches regenerating a local clock signal to control capture of the command and

address signals. Ex. 1011 ¶¶ 77, 80 (citing Ex. 1008, 7:35–42, 11:29–37, Fig. 4). We credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein. For instance, Lee teaches "*regenerating an additional data write clock signal from said received data write clock signal*, and using said additional regenerated data write clock signal to control the capture of command and address data within said register." Ex. 1008, 11:29–37. Importantly, as we noted in the Institution Decision (Dec. 27–28), Lee teaches that the frequency of that additional data write clock signal may be at a frequency of "X/N where X is the frequency of said received data write clock signal and N is an integer" (*id.* at 11:38–41). We further noted with respect to the last of these that because "1" is an integer, when "N" is "1" the same frequency is used.

Patent Owner relies upon claim 31 of Lee, which recites "the frequency of said additional data write clock signal is at a frequency of X/N where X is the frequency of said received data write clock signal and N is an integer." PO Resp. 47. Patent Owner, however, does not respond to our analysis in the Institution Decision regarding when "N" is "1" ("an integer") the same frequency is used. *Id.* Instead, Patent Owner asserts without explanation that this teaching "helps confirm that WCLK/2 and WCLK of Lee's Figure 4 are not the same frequency." *Id.*

Patent Owner's conclusory attorney argument is unavailing. We find that Lee's disclosure that the frequency of the additional data write clock signal may be at a frequency of "X/N where X is the frequency of said received data write clock signal and N is an integer" (*id.* at 11:29–41) teaches or at least suggests receipt by the register of a copy of the incoming clock signal from the clock regeneration circuit, as recited in claim 1, that

has the same frequency as the incoming clock signal (i.e., when "N" equals "1" (an integer)).

Additionally, we are persuaded by Petitioner's contentions (Pet. 45–48 (citing *e.g.*, Ex. 1008, 7:35–41, 11:29–37, Fig. 4; Ex. 1011 ¶¶ 77–80)) and credit Dr. Subramanian's testimony that Lee teaches that register 45 is configured to receive a regenerated clock signal so as "to control capture of the command and address signals on the command address (C/A) signal lines 15." Ex. 1008, 7:35–41. Lee's register 45 is configured to receive the regenerated local WCLK signal from PLL 41 *e.g.*, via one or more signal lines to clock in the command and address data. *Id.* at 7:35–41, Fig. 4. Such a regenerated local WCLK signal may include a clock signal having the same frequency as the incoming clock signal. *See, e.g.*, *id.* at 7:35–41, 11:29–41. Thus, even assuming Patent Owner is correct that the recited "one of the copies of the incoming clock signal" must have the same frequency as the incoming clock signal and that Lee's WCLK/2 operates at half the frequency of WCLK, Lee's register 45 would nevertheless still be "configured to receive one of the copies of the incoming clock signal" because receiving the full frequency signal would not require register 45 to be "configured" any differently than as taught in Lee. Reply 16–17.

Furthermore, Dr. Subramanian testifies that the number of buses or branches exiting register 45 is a "design choice" among a number of limited number of alternatives. *See, e.g.*, Ex. 1011 ¶ 79. We credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein, including Lee's teachings discussed above. Ex. 1008, 7:35–41, 11:29–41, Fig. 4. We also find that Dr. Subramanian's testimony regarding why one having ordinary skill in the art would have modified Lee's teachings, for

example, such that two buses are used to deliver two signals (rather than a single bus that branches into two pieces), provides sufficient articulated reasoning with rational underpinning to support the legal conclusion of obviousness. Ex. 1011 ¶ 79 ("One of ordinary skill in the art would have been motivated to use a known dual bus design at least to reduce the drive strength per bus needed.")

Patent Owner relies on Dr. Bernstein's testimony only as evidence supporting that the WCLK/2 signal has a different frequency from the WCLK signal, i.e., different by a factor of two. PO Resp. 43–47 (citing Ex. 2019 ¶ 105). However, even crediting Dr. Bernstein's testimony, we remain persuaded by Petitioner's contentions and evidence because Patent Owner's contentions are not commensurate with the scope of the claim. We further are persuaded by Petitioner's contentions and evidence, even under Patent Owner's proposed construction, because we find that other disclosures of Lee teach or suggest the recitation, as set forth immediately above. Ex. 1008, 7:35–41, 11:29–41; Ex. 1011 ¶¶ 79, 80.

Patent Owner also contends "[b]oth Petitioner and Patent Owner agree that . . . copies of the incoming clock signal cannot operate at multiples of the frequency of the incoming clock signal." PO Resp. 45. Patent Owner further contends "[t]hus, it is undisputed that in the invention, copies of the incoming clock signal must have the same frequency as the incoming clock signal." *Id.* Petitioner, however, has shown that Lee's copies of the incoming clock signal, i.e., the copies generated and supplied to the memory chips, have the same frequency as the incoming clock signal. For instance, as discussed above with respect to annotated Figure 4, we credit Dr. Subramanian's testimony as it is consistent with the evidence cited therein

that Lee teaches that PLL 41 generates copies of incoming clock signal, namely WCLK 0–8, and supplies those copies to memory chips 39 and that each of the copies have the same frequency as input clock WCLK. Ex. 1011 ¶¶ 72, 73 (citing Ex. 1008, 6:51–55, Fig. 4).

Patent Owner's dispute (PO Resp. 43–47) pertains to only the clock signal received by register 45 that is set to provide a copy of the signals to the three exemplary memory devices on the left and a copy of the signals to the exemplary memory devices on the right. Ex. 1011 ¶ 79. To the extent that Patent Owner argues that Lee is not enabling, such argument is misplaced because there is a rebuttable presumption that the disclosure in a prior art patent, as here, is enabled. *See Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003); *see also In re Antor Media Corp.*, 689 F.3d 1282, 1287−88 (Fed. Cir. 2012) (holding that prior art publications and patents are presumed to be enabled).

We turn to Patent Owner's second contention that Lee does not teach a register circuit and clock signal regeneration circuit in a common chip packing (PO Resp. 47–52). Relying on the testimony of Dr. Subramanian, Petitioner contends that it would have been obvious to one of ordinarily skill in the art to include the register (Register 45) and the clock signal regeneration circuit (PLL 41) in a single chip packing and integrated on one chip. Pet. 44–45, 48 (citing Ex. 1008, Fig. 4; Ex. 1011 ¶¶ 74–76, 82). As indicated above, Patent Owner does not dispute (PO Resp. 43–56) that Lee teaches that the register circuit is arranged on the memory module with the clock regeneration circuit. Ex. 1008, 7:26–27 ("FIG. 4 illustrates in greater detail a memory subsystem 27, which as noted, may be a DIMM [dual in-

line memory module] memory device."), Fig. 4 (illustrating memory module 27 having "REGISTER" 45 and "PLL" 41).

Patent Owner contends that the Petition's assertion is insufficiently supported because Dr. Subramanian's testimony is based on vague statements in Lee that do not suggest putting Lee's register and PLL in a common chip packaging. PO Resp. 47–48. Dr. Subramanian testifies that it would have been obvious to include the register (Register 45) and the clock signal regeneration circuit (PLL 41) in a common chip packing and integrated on a common chip because Lee teaches flexible packaging options, including the option to package constituent components together. Ex. 1011 ¶¶ 75, 82 (citing Ex. 1008, 8:25–28). We credit Dr. Subramanian's testimony because it is consistent with Lee's teaching of "a one-chip memory controller or a chip set or may be a separate processor or part of a processor." Ex. 1008, 8:25–28. Patent Owner contends that Lee's teaching pertains to "other elements." PO Resp. 48. However, we credit Dr. Subramanian's testimony because consistent with his explanation (Ex. 1011 ¶¶ 75, 82), Lee's teachings pertain to memory controller 11, which like Register 45 and PLL 41 provides control for the memory devices. Ex. 1008, 8:25–28.

Patent Owner contends "[i]n the alternative" Petitioner asserts that "this limitation is a mere 'design choice[] for packaging these components,'" but merely stating that a particular placement of an element is a design choice does not make it obvious. PO Resp. 48-49 (citing *Cutsforth, Inc. v. Motivepower, Inc.*, 636 Fed. App'x 575, 578 (Fed. Cir. 2016) (nonprecedential)). In the instant proceeding, contrary to Patent Owner's contention, Petitioner's obviousness contention (Pet. 41–45) does not

involve a rearrangement of parts. Patent Owner also contends an "unnumbered possibilities negate motivation to pick any particular possibility." PO Resp. 49 (citing *Insite Vision Inc. v. Sandoz, Inc.*, 783 F.3d 853, 860–61) (Fed. Cir. 2015)). We, however, credit Dr. Subramanian's testimony, for example, because he points to Lee's teachings regarding "one-chip memory" or "a chip set" as evidence supporting his testimony that these two design choices (i.e., packaged either together or separately) would have been known alternatives to a person of ordinary skill in the art. *Id.* at 8:26–27 (cited in Ex. 1011 ¶ 75).

Patent Owner also disputes Petitioner's design choice contentions on the basis that the common packaging was an unexpected solution to stated problems in the '150 Patent Specification. PO Resp. 50 (citing Ex. 1001, 2:47–67, 3:1–29). Patent Owner further argues its contentions are supported by extrinsic evidence showing that the register and PLL "were not combined in a common chip until DDR3 RDIMMs" and the earlier generation DDR2 RDIMM used two discrete chips. PO Resp. 50–52 (citing Ex. 2019 ¶¶ 120–22; Ex. 2029; Ex. 2031, 2).

Upon consideration of the parties' contentions and evidence, we are persuaded by Petitioner's contentions and we credit Dr. Subramanian's testimony as consistent with the evidence of record. Dr. Subramanian testifies it would have been obvious to consolidate register 45 and PLL 41 because "the industry trend both at the time the 150 was filed and now is to consolidate circuits within fewer chip packages, as this reduces costs and facilitates manufacturing of systems with the packages." Ex. 1011 ¶ 76. Dr. Bernstein testifies "there was much discussion around moving the register and PLL to a single chip when DDR3 was developed in the late 2000s." Ex.

2019 ¶ 121 (citing Ex. 2032, 2); *see also* Ex. 2032, 2 ("DDR2 employs at least one register and a PLL instead of two separate components; DDR3 employs a single monolithic-IC chip, which integrates the register and PLL.")

Dr. Bernstein's testimony is consistent with Dr. Subramanian's testimony that the industry trend was to integrate the register and PLL. *Compare* Ex. 2019 ¶ 121 *with* Ex. 1011 ¶ 76. The dispute pertains to the timing of this trend. Ex. 1011 ¶ 76; Ex. 2019 ¶ 121. Dr. Bernstein's testimony that "there was much discussion around moving the register and PLL to a single chip when DDR3 was developed in the late 2000s" identifies as support an article entitled "Evolving to DDR technology" dated May 28, 2009. Ex. 2019 ¶ 121 (citing Ex. 2032). That article refers to "[t]he *latest* DDR3-memory standard, JEDEC JESD79-3A" and also refers to a "DDR3 SDRAM Specification" dated September 2007. Ex. 2032, 1, 5. The references to the standards "3A" and "3B" may be indicative that these are not the first of the DDR3 standards. *Id.* Dr. Bernstein also testifies "DDR2 RDIMMs had their PLLs and registers on separate chips on the module and this did not change until years after the '150 Patent." Ex. 2019 ¶ 120 (citing Exs. 2029–2031). This testimony of Dr. Bernstein and evidence cited therein (*id.*) pertain to commercial availability of DDR systems, not when it would have been obvious to one of ordinary skill in the art to integrate a PLL and register on a common chip and in a common chip packaging and the testimony is vague with respect to "years after" (*id.*).

Upon consideration of the parties' contentions regarding this limitation and the evidence of record, we credit Dr. Subramanian's testimony regarding the timing and give it substantial weight because Dr.

Subramanian's testimony that it would have been obvious to one of ordinary skill in the art to consolidate the register in a common chip packing and integrated on a common chip with the clock regeneration circuit is consistent with the evidence of record. Ex. 1011 ¶ 76. In comparison, we give Dr. Bernstein's testimony regarding the timing little to no weight because it is inconsistent with the evidence of record. Ex. 2019 ¶ 121. Lee, for example, describes that memory controller 11, which has PLL 13 (Ex. 1008, Fig. 1), "can be a one-chip memory controller or a chip set" (*id.* at 8:24–26). As an additional example, the '150 Patent Specification describes "DDR3" in the Background and indicates that DDR technology was known, i.e., "*[p]resen*t memory systems (DDR1; DDR2; *DDR3*)." Ex. 1001, 1:20 (emphases added); *see also id.* at 1:33–35 (describing a consideration for "successor technologies of the DDR3 system, for example for DDR4.").[7] This is consistent with Dr. Subramanian's testimony and not Dr. Bernstein's testimony because the evidence supports Dr. Subramanian's testimony (Ex.

[7] Patent Owner provides additional contentions (PO Resp. 56–58) for dependent claim 5, which recites the further recitation that "the clock signal regeneration circuit and the register circuit are integrated on a common chip" (Ex. 1001, 7:36–38), which we have considered in full, as we discuss below. Although not necessary for our determination, contrary to those Patent Owner contentions (PO Resp. 56–58), as further extrinsic evidence that it was known to integrate on a common chip a clock signal and an address and command register, consistent with Petitioner's contentions (Pet. 26), Dodd teaches clock circuit 300 and clock driver 310 embedded in ADDR/CMD buffer 122. Ex. 1003, 3:51–65, 5:57–6:11, Fig. 3; Ex. 1011 ¶ 19, 44, 79, 82. Also, consistent with Petitioner's contentions (Pet. 25) Dodd teaches that "a PLL is utilized to implement the clock circuit 300 for performing synchronization" (Ex. 1003, 5:6–32, Fig. 4) and ADDR/CMD 122 is a buffer or register (*id.* at 2:39–3:3).

1011 ¶ 76) that the industry trend at the time the '150 Patent was filed was to consolidate circuits within fewer chips.

We turn to the third of Patent Owner's contentions, i.e., that Lee does not teach a plurality of copies of the command and address signals. PO Resp. 52–56. Patent Owner contends Lee does not disclose making multiple copies of the command and address signals because Figure 4 illustrates "multiple lines labeled C/A coming into register **45** and only one line labeled C/A coming out of it." *Id.* at 53.

We, however, are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that making copies of the incoming command and address signals would have been obvious over Lee's teachings because Petitioner's contentions and Dr. Subramanian's testimony are consistent with the evidence cited therein, including Lee's teachings. Pet. 46–48 (citing e.g., Ex. 1011 ¶¶ 78–80). For instance, contrary to Patent Owner's contention that "one line" comes out of register 45 (PO Resp. 53), consistent with Petitioner's contentions (*see, e.g.*, Pet. 46–47; Reply 19), Lee illustrates hash marks on the line exiting register 45, which indicate that multiple lines, e.g., a bus, exiting register 45. Ex. 1008, Fig. 4.

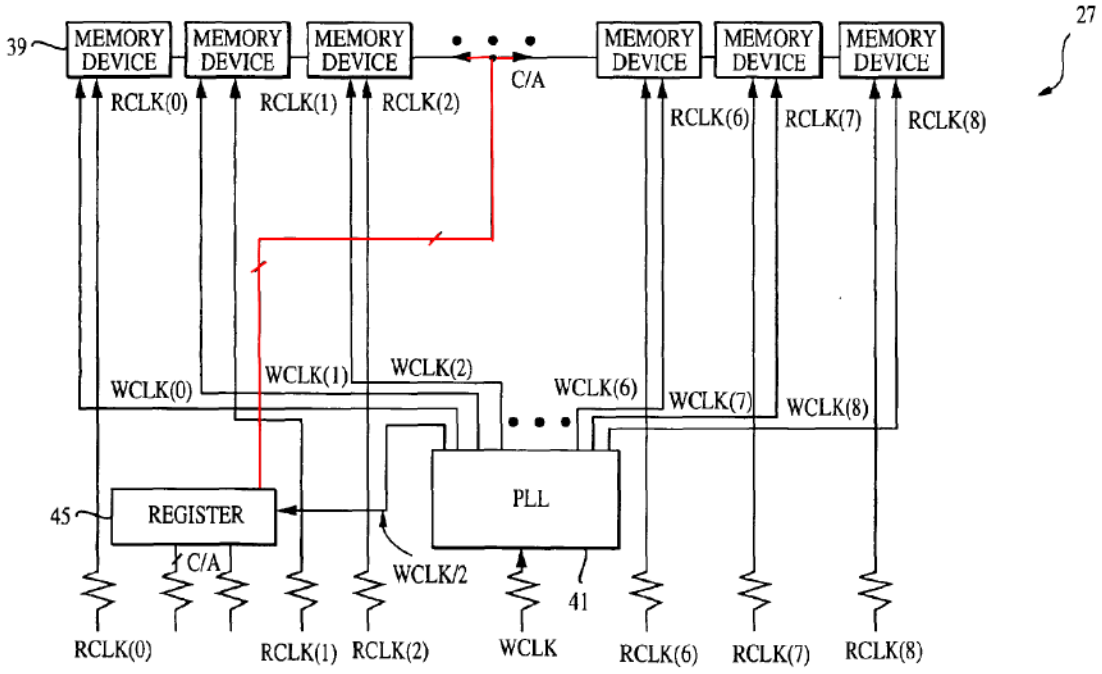

FIG. 4

Figure 4 illustrates Memory Subsystem 27 with Annotations by the Board

Figure 4 of Lee reproduced above has been annotated in red to show the line with hash marks leaving register 45 carrying command and address signals. Dr. Subramanian testifies that it would have been obvious in view of Lee's teaching, for example, to supply multiple copies of the incoming command and address signals. Ex. 1011 ¶ 79. We credit Dr. Subramanian's testimony because it is consistent with Lee's teaching of command and address signals being sent from register 45 to multiple memory devices 39, including the memory devices on the left and the memory devices on the right, as well as other evidence cited. *See*, *e.g.*, Ex. 1008, Fig. 4; Ex. 1003, Fig. 1 (illustrating two buses carrying command and address signals). Supplying command and address signals to two groups of memory devices, e.g., memory devices on the left and memory devices on the right is similar

to embodiments described in the '150 Patent Specification, which for the reasons discussed above *supra* in Section II.C.1, we determine are encompassed in the scope of claim 1. *Compare* Ex. 1001, 2:57–59 (providing "several" copies "to *several DRAM branches or channels*") *with* Ex. 1008, Fig. 4; *see also* Ex. 1001, 5:57–6:9 (describing providing command and address signals to "two semiconductor memory chip groups."). Furthermore, Petitioner's contentions also are consistent with the deposition testimony of Dr. Bernstein regarding the hash marks illustrated in Figure 4 of Lee "I think it's generally understood that when we see a hash it's representing many lines in parallel representing . . . [a] parallel set of connections." Ex. 1020, 111:17–24.

Patent Owner also argues that a branch does not make a copy. PO Resp 54 (citing Ex. 2019 ¶¶ 67, 113; Ex. 2018, 115:22–23). Patent Owner further argues that Lee shows "that the outgoing C/A signals are ***branched*** off the incoming signals." *Id.* Patent Owner's contentions, however, do not apply to Petitioner's argument and Dr. Subramanian's testimony that it would have been obvious in view of Lee's teachings for copies to be made by register 45, e.g., by using a dual-bus architecture. Ex. 1011 ¶¶ 79, 80 (citing, *e.g.*, Ex. 1008, Fig. 4; Ex. 1003, Fig. 1). Additionally, to the extent that Patent Owner's contentions imply that branching results in fewer signals, the contentions are not consistent with the evidence of record. For instance, Dr. Subramanian testifies: "A branch does not make a copy. It provides the same signal to everything." Ex. 2018, 115:22–24. Dr. Bernstein's testimony regarding the distinction between branching and copying pertains to electrical characteristics of the signal. *See, e.g.*, Ex. 2019 ¶ 113. Furthermore, Lee teaches multiple memory devices 39 (six

exemplary devices illustrated) receiving command and address signals. Ex. 1008, Fig. 4.

Relying on the testimony of Dr. Bernstein, Patent Owner, additionally, argues that "'[i]n contrast to the multiple WCLK signals ("WCLK(0)–WCLK(8)") that emanate from the PLL 41, this one C/A line in Lee would clearly suggest to a POSITA that no copies are made at the Register 45." PO Resp. 54 (citing Ex. 2019 ¶ 111). However, the "one C/A line" (*id.*) is the line with hash marks that Dr. Bernstein acknowledged represents "many lines in parallel" (Ex. 1020, 111:17–24), and this contention does not pertain to Petitioner's contentions and Dr. Subramanian's testimony regarding obviousness. Additionally, register 45 need not have eight lines exiting it to teach "a plurality of copies" recited in claim 1. Claim 9, which depends from claim 1 and is not contested by Patent Owner, further recites "wherein the clock signal regeneration circuit and the register circuit respectively generate *two copies* of the clock signal and the *command and address signals* for distribution to the memory chips." Ex. 1001, 8:1–5 (emphases added). Additionally, Lee's teaching is similar to embodiments described in the '150 Patent Specification, which for the reasons discussed above *supra* in Section II.C.1, are encompassed in the scope of claim 1, describing only two lines exiting. *Compare* Ex. 1001, 5:57–6:9 (describing providing command and address signals to "two semiconductor memory chip groups") *with* Ex. 1008, Fig. 4.

Again, relying on the testimony of Dr. Bernstein, Patent Owner argues because Lee has "multiple C/A signals entering the register," Lee does not teach copying the signals and a person having ordinary skill in the art would not have a reason to modify Lee to add this limitation. PO Resp. 54–56

(citing *e.g.*, Ex. 2019 ¶¶ 112–16). Dr. Bernstein testifies "Lee has more than one C/A line entering register 45," which is "what the '150 Patent was designed to avoid." Ex. 2019 ¶ 115–16 (citing Ex. 1001, 1:29–32). However, the '150 Patent Specification illustrates multiple incoming command address ("CA") signal lines, again depicting hash marks. Ex. 1001, Figs. 1–5; *see also id.* at 5:30–38 ("as was the case in the first embodiment . . . command and address *signals* CA that are supplied to the module 100 via *CA lines 71*") (emphases added), 5:38–41 ("In the second embodiment . . . the differential command and address *signals* CA are supplied via the input CA *lines* 71") (emphases added), 5:62–66 ("the invention proposes to arrange . . . a clock signal regeneration circuit and a register circuit . . . and to connect them to *bus signal lines 61, 71* supplying the command and address *signals*") (emphases added). Lee's teaching of a bus (the line to the left with the hash mark) and a single line (to the right) providing incoming signals to register 45 is substantially the same as the embodiments depicted in the '150 Patent Specification of using a bus to receive command and address signals, for example, line 71 with hash marks denoted "CA signal lines," for example in Figure 2. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Figs. 1–5.

Additionally, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 56; Ex. 2019 ¶¶ 115–16) pertain to a different modification than that set forth in Petitioner's contentions and Dr. Subramanian's testimony (Pet. 46–47; Ex. 1011 ¶ 79). In particular, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 56; Ex. 2019 ¶¶ 115–16) assume an "increased number of pins" for incoming command/address signals, whereas Petitioner's contentions and Dr.

Subramanian's testimony pertain to generating copies, rather than receiving the copies (Pet. 46–47; Ex. 1011 ¶ 79).

Furthermore, even if multiple copies were received, Patent Owner's contentions and Dr. Bernstein's testimony (PO Resp. 54–56 (citing *e.g.*, Ex. 2019 ¶¶ 112–16) are not commensurate with the scope of claim 1, which does not prohibit more than one incoming line and recites that the register circuit is "configured to temporarily store the incoming command and address *signals*." Ex. 1001, 7:18–20. Claim 1 also is directed to a memory module "comprising" the various elements recited. *Id.* at 7:2. The term "comprising" is a term of art used in claim language, which means that the named elements are essential, but other elements also may be included to constitute additional components within the scope of the claim. *See Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997).

Upon consideration of Dr. Subramanian's testimony that it would have been obvious over Lee's teachings "to generate a plurality of copies of the incoming command and address signals," by register 45, for example, by using two buses to provide copies of the incoming command and address signals to memory devices 39 (one bus for devices on the left and one bus for devices on the right) (Ex. 1011 ¶ 78–80) and Dr. Bernstein's testimony (Ex. 2019 ¶¶ 110–16), we credit and give substantial weight to Dr. Subramanian's testimony because we find it consistent with the teachings of the art cited therein. In contrast, we give Dr. Bernstein's testimony little or no weight. Ex. 2019 ¶¶ 110–16. Regarding the evidence of record, Lee, for instance, teaches that register 45 "capture[s]" the incoming command and address signals and "clocks in the command and address data." Ex. 1008, 7:34–41. Patent Owner does not dispute that Lee's register 45 temporarily

stores the incoming command and address signals. PO Resp. 43–56. Lee's Figure 4 also illustrates register 45 then providing copies of the incoming command and address signals to memory devices 39 via the line with hash marks . Ex. 1008, Fig. 4; Ex. 1011 ¶ 79. Furthermore, Figure 4 of Lee also includes a "C/A" label at the top of Figure 4 illustrating providing command and address signals to three memory devices on the left-hand side and three memory devices on the right-hand side. *Id.* at Fig. 4. We are persuaded that it would have been obvious in view of these teachings, for example, to use the dual bus design with two copies leaving register 45, as testified by Dr. Subramanian. Ex. 1011 ¶¶ 79, 80; *see also* Ex. 1020, 111:17–24 (Dr. Bernstein testifies "I think it's generally understood that when we see a hash it's representing many lines in parallel representing . . . [a] parallel set of connections.") Additionally, Lee is directed to "a clocking system and method for effecting high speed data transfers" (*id.* at 1:10–12) and specifically teaches providing command and address (C/A) signals to a plurality of memory storage devices via a register (*id.* at 4:1–14, 7:34–41, 11:4–41, Fig. 4).

Patent Owner's argument fails to recognize that "[w]hat a prior art reference discloses or teaches is determined from the perspective of one of ordinary skill in the art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1361 n.3 (Fed. Cir. 2008). A prior art reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994); *see also*; *DeGeorge v. Bernier*, 768 F.2d 1318, 1323 (Fed. Cir. 1985) (superseded on other grounds by statute, Patent Law Amendments Act of 1984, 35 U.S.C. §§ 135, 141–46) (holding that a reference "need not, however, explain every

detail since [it] is speaking to those skilled in the art"); *In re Preda*, 401 F.2d 825, 826 (CCPA 1968) (explaining that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom").

We further are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that it also would have been obvious to one having ordinary skill in the art to modify Lee's teachings to use two buses and deliver the plurality of copies of the command and address signals over those buses because sufficient reason is given for this modification. Pet. 46–48 (citing *e.g.*, Ex. 1011 ¶¶ 78–80). For instance, Dr. Subramanian testifies "one of ordinary skill in the art would have understood that the choice between using a single bus that branches into two pieces to deliver two signals or to use two buses was a simple design choice." Ex. 1011 ¶ 79 (citing *e.g.*, Ex. 1003, Fig. 1). We credit Dr. Subramanian's testimony because he testifies that using two buses was a design choice among a number of limited number of alternatives, e.g., using a single bus that branches or two buses. We also credit Dr. Subramanian's testimony that using two buses was a design choice that would have been known because it is consistent with the evidence cited therein including, for example, Figure 1 of Dodd (Ex. 1003), which illustrates a single input into ADDR/CMD buffer 122 and two buses (denoted with hash marks) exiting ADDR/CMD buffer 122. Ex. 1003, Fig. 1. The buses exiting ADDR/CMD buffer 122 carry copies of the incoming address and command signals, the top bus carrying signals to memory devices 130 and 140 and the bottom bus carrying signals to memory devices 135 and 145. *Id.* We find that Dr. Subramanian's

testimony also provides a motivation to use the dual bus design. *See, e.g.*,Ex. 1011 ¶ 79 ("One of ordinary skill in the art would have been motivated to use a known dual bus design at least to reduce the drive strength per bus needed.") Accordingly, we find that Dr. Subramanian's testimony provides sufficient articulated reasoning with rational underpinning to support the legal conclusion of obviousness.

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 1 are obvious over Lee.

c. Conclusion—Claim 1

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 1 is unpatentable under § 103(a) as obvious over Lee.

4. Discussion of Claims 2, 5, 6, and 8–10

Each of claims 2, 5, 6, and 8–10 depends directly from independent claim 1. We have reviewed Petitioner's showing (Pet. 48–52) with respect to dependent claims 2, 5, 6, and 8–10 and the teachings of Lee.

a. Claim 2

Claim 2 recites "wherein the clock signal regeneration circuit comprises a phase locked loop (PLL) circuit." Ex. 1001, 7:26–28. We are persuaded by Petitioner's contentions (Pet. 48) because Lee teaches that the clock regeneration circuit is PLL 41. *See, e.g.*, Ex. 1008, Fig. 4. Patent Owner does not contest separately Petitioner's showing for claim 2. Based on the entirety of the record before us, we are persuaded by and adopt as our

own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 2 are obvious over Lee.

b. Claim 5

Claim 5 recites "wherein the clock signal regeneration circuit and the register circuit are integrated on a common chip in the common chip packing." Ex. 1001, 7:36–38. Petitioner relies on its contentions for claim 1. Pet. 48; Reply 20. Patent Owner also relies on its contentions for claim 1, but, additionally, contends that "it is far from straightforward" to integrate on a common chip PLL 41, which is an analog device and register 45, which is a digital device. PO Resp. 57–58 (citing *e.g.*, Ex. 1003, 5:40–43; Ex. 2019 ¶¶ 118, 119, 122). Dr. Bernstein testifies that "[i]t is difficult and expensive to integrate analog and digital systems on a single chip" relying on Dodd's teachings. Ex. 2019 ¶ 118 (citing Ex. 1003, 5:40–43). Although Dodd indicates "in a digital system such as memories, a PLL having analog characteristics may introduce analog design complications in a mainly digital design" (Ex. 1003, 5:40–43), Dodd also teaches "[a]s compared to using a DLL, the advantages of using a PLL, is that the PLL is more accurate" (*id.* at 5:36–37). Additionally, consistent with Petitioner's contentions (Pet. 26), Dodd teaches an embodiment in which clock circuit 300 and clock driver 310 are embedded in ADDR/CMD buffer 122. Ex. 1003, 3:51–65, 5:57–6:11, Fig. 3; Ex. 1011 ¶ 19, 44, 79, 82. Also, consistent with Petitioner's contentions (Pet. 25) Dodd teaches that "a PLL is utilized to implement the clock circuit 300 for performing synchronization" (Ex. 1003, 5:6–32, Fig. 4) and ADDR/CMD 122 is a buffer or register (*id.* at 2:39–3:3). Dr. Bernstein also testifies regarding other

complexities (*see, e.g.*, Ex. 2019 ¶ 119), but as Dr. Bernstein testifies, these complexities were overcome (*id.* ¶¶ 120, 121).

Upon consideration of all Patent Owner's contentions, including those presented for both claims 1 and 5, we are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony for the same reasons discussed *supra* Section II.D.3 with respect to claim 1. Indeed, throughout our discussion of claim 1, we referred to "common chip packing" in connection with "integrated on a common chip" as both parties' contentions for claim 1 and "common chip packing" pertain to whether the clock signal regeneration circuit and the register circuit are both in "common chip packing" and also "integrated on a common chip." We, again, note that our finding that Petitioner's contentions are persuasive and our crediting of Dr. Subramanian's testimony is based, for example, on Lee's express teaching of employing on "a one-chip memory or a chip set" memory controller 11, having a PLL and which communicates digital data to and from memory devices 39. Ex. 1008, 8:24–29, Fig. 1.

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 5 are obvious over Lee.

c. Claim 6

Claim 6 recites "wherein the common chip packing is arranged essentially at a central position on the memory module." Ex. 1001, 7:39–41. Petitioner contends it would have been obvious to one having ordinary skill in the art to arrange the common chip packing at a central position on the memory module. Pet. 48–49 (citing *e.g.*, Ex. 1011 ¶¶ 83–84). Dr. Subramanian testifies that Lee teaches locating the common chip packaging

in essentially a central position on the memory module because Lee discloses PLL 41 located in a central position. Ex. 1011 ¶ 83. Dr. Subramanian also testifies one of ordinary skill in the art would have known that the PLL and register circuit should be placed in a central location and would have had reasons to do so including that such placement would have been known to simplify the design. *Id.* ¶¶ 83, 84 (citing Ex. 1008, Fig. 4; Ex. 1010, Fig. 2).

For claim 6, relying on the testimony of Dr. Bernstein, Patent Owner contends that Lee's Figure 4 does not illustrate a physical arrangement because it is a circuit diagram and "so the same reasoning discussed with respect to Dodd in Section IV.C, *supra*, also applies here to Lee." PO Resp. 60 (citing Ex. 2019 ¶ 124). In addition to testifying regarding Lee, Dr. Bernstein testifies "the statements I made in ¶¶ 89–97, *supra*, for Dodd are equally applicable to Lee." For the most part, Patent Owner's contentions and Dr. Bernstein's testimony regarding Dodd, however, apply particularly to Dodd and not to Lee. PO Resp. 29–39; Ex. 2019 ¶¶ 89–97. The Patent Owner Response must include "a detailed explanation of the significance of the evidence." *See* 37 C.F.R. §§ 42.22, 42.23, 42.120. Such a detailed explanation is not provided. To the extent contentions or testimony are reasonably understood to apply to both Lee and Dodd, we provide a response. We decline, however, to try to ascertain what Patent Owner might have argued with respect to Lee.

We now turn to Patent Owner's contention and Dr. Bernstein's testimony that Lee's Figure 4 does not illustrate a physical arrangement because it is a circuit diagram. PO Resp. 60; Ex. 2019 ¶ 124. Dr. Bernstein testifies "Lee is a circuit diagram that shows how different circuit elements

are connected, rather than a layout diagram that shows where the circuit elements are physically located on a module." Ex. 2019 ¶ 124. Dr. Bernstein testifies that Dr. Subramanian agrees. *Id.* ¶ 90 (citing Ex. 2018. 129:24–130:2, 130:13–18). Dr. Bernstein testifies that his "conclusion" "is reinforced by the fact that the register **45** is located in the bottom left corner of the diagram." *Id.* ¶ 124. Dr. Bernstein also testifies "Petitioner also states that it would be obvious to place the register circuit and clock regeneration circuit at a central position of the memory module," but "Petitioner does not cite to any evidence in Lee to support this contention." Ex. 2019 ¶ 124 (citing Pet. 49).

> Dr. Subramanian testifies
>
> Q. On what way is a circuit diagram is different from a layout diagram?
>
> A. The way a circuit diagram is drawn is intended to emphasize the electrical structure and essentially establish the electrical functional relationships between components. The way a layout is drawn, it's intended to emphasize the special structure. However, it turns out it is possible to go from one to the other and back. *So, in other words from a circuit diagram you can calculate a layout or generate a layout and from a layout you can back circuit what the circuit diagram is*. So they're essentially -- they contain similar information with different things emphasized.
>
> Q. How can you calculate a layout diagram from a circuit diagram?
>
> A. *If you have a circuit diagram you can generate a layout that would correspond to that circuit, which will specify the wiring, will specify the component placement, etcetera*. In fact, today a lot of that is automated and it has been automated for awhile.

Ex. 2018, 130:13–131:10 (emphases added). Additionally, Dr. Subramanian testifies that "in Figure 4 [of Lee], the PLL chip is disclosed to be located in a central position on the module." Ex. 1011 ¶ 83.

Upon consideration of Dr. Subramanian's testimony (*see, e.g.*, Ex. 1011 ¶¶ 83–84, Ex. 2018, 129:8–131:10) and Dr. Bernstein's testimony (*see, e.g.*, Ex. 2019 ¶¶ 90, 124), we credit Dr. Subramanian's testimony and give it substantial weight (*see, e.g.*, Ex. 1011 ¶¶ 83–84, Ex. 2018, 129:8–131:10), whereas we give Dr. Bernstein's testimony (see, e.g., Ex. 2019 ¶¶ 90, 124) little to no weight because we find that Dr. Subramanian's testimony is consistent with the evidence cited therein. As an initial matter, we decline to discount Dr. Subramanian's testimony and the evidence that he relies on because the diagrams in the patents are not expressly identified as layout diagrams. It is well settled that things patent drawings show clearly are not to be disregarded. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972).

Consistent with Dr. Subramanian's testimony (Ex. 1011 ¶ 83), Lee illustrates PLL 41 located in a central position in Figure 4. Dr. Subramanian also testifies one of ordinary skill in the art would have known that the PLL and register circuit should be placed in a central location and would have had reasons to do so including that such placement would have been known to simplify the design. *Id.* ¶¶ 83, 84 (citing Ex. 1008, Fig. 4; Ex. 1010, Fig. 2). Regarding Dr. Bernstein's testimony that "the register **45** is located *in the bottom left corner of the diagram*" (Ex. 2019 ¶ 124), consistent with Dr. Subramanian's testimony (Ex. 1011 ¶¶ 75, 76 82–84) we find that register 45 is placed to the left, and alongside, PLL 41, indicating that the two components should be located together, *e.g.*, side-by-side. Ex. 1008, Fig. 4.

Regarding Dr. Bernstein's testimony that "Petitioner also states that it would be obvious to place the register circuit and clock regeneration circuit at a central position of the memory module," but "Petitioner does not cite to any evidence in Lee to support this contention" (Ex. 2019 ¶ 124 (citing Pet. 49)), we are persuaded by Petitioner's contentions supported by Dr. Subramanian's testimony and the other evidence cited therein. Pet. 44–45, 48–49 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1010, Fig. 2; Ex. 1011 ¶¶ 75–76, 82–84); Reply 20–21 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1010, Fig. 2). For instance, the PLL 41 is shown in Figure 4 of Lee in an essentially central location similar to that illustrated in embodiments in the '150 Patent Specification. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Figs. 1, 3 (illustrating a placement near, but not exactly at the center). Additionally, we credit Dr. Subramanian's testimony (Ex. 1011 ¶¶ 75, 76 82–84), for example, because we find it is consistent with Lee's teaching that a control element such as register 45 and PLL 41 "can be a one-chip memory controller or a chip set, or may be a separate processor, or part of a processor" (Ex. 1008, 8:25–27) taken together with the illustration in Figure 4 of PLL 41 in a central location (*id.* at Fig. 4). Furthermore, although not necessary for our determination, we also credit Dr. Subramanian's testimony (Ex. 1011 ¶ 84), for example, because it is consistent with the illustration of register 210 and PLL 212 in an essentially central location in registered memory module 200 in Figure 2 of Exhibit 1010.[8]

[8] Exhibit 1010 is U.S. Patent Application Publication 2004/0143773 A1 and was published July 22, 2004.

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 6 are obvious over Lee.

d. Claim 8

Claim 8 recites "wherein the bus signal lines of the command and address signals comprise a fly-by bus structure." Ex. 1001, 7:45–47. We are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony that Lee teaches the further recitation of claim 8 because Petitioner's contentions and Dr. Subramanian's testimony are consistent with the evidence cited therein. Pet. 50–51 (citing *e.g.*, Ex. 1008, Fig. 4; Ex. 1001, Fig. 5; Ex. 1011 ¶¶ 85–86). For instance, we find that Figure 4 of Lee illustrates address/command buses that fly by multiple memory devices. Ex. 1008, Fig. 4. Additionally, Figure 4's fly-by structure is similar to that shown in Figure 5 of the '150 Patent, which is described as being "a schematic layout view of the [ ] semiconductor memory module with fly-by bus structure with two copies of the clock signal and command address signal bus," (Ex. 1001, 4:23–26) which is encompassed in the scope of claim 8. *Compare* Ex. 1008, Fig. 4 *with* Ex. 1001, Fig. 5.

Patent Owner does not contest separately Petitioner's showing for claim 8. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 8 are obvious over Lee.

e. Claim 9

Claim 9 recites "wherein the clock signal regeneration circuit and the register circuit respectively generate two copies of the clock signal and the

command and address signals for distribution to the memory chips." Ex. 1001, 8:1–5. We are persuaded by Petitioner's contentions and credit Dr. Subramanian's testimony for the same reasons discussed *supra* in Section II.D.3 with respect to claim 1. Pet. 51 (citing Ex. 1011 ¶ 87).

Patent Owner does not contest separately Petitioner's showing for claim 9. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 9 are obvious over Lee.

f. Claim 10

Claim 10 recites "wherein the memory module comprises an RDIMM module." Ex. 1001, 8:6–7. As we discussed with respect to claim construction *supra* in Section II.C.2, we need not make a determination regarding the broadest reasonable interpretation of "RDIMM" because we are persuaded that Petitioner shows sufficiently that Lee teaches an "RDIMM" based on Patent Owner's proposed construction. Accordingly, for the purpose of this Decision, RDIMM means "registered dual in line memory module, which buffers control signals, but not data signals."

Relying on the testimony of Dr. Subramanian, Petitioner contends that Lee's memory subsystem 27 teaches an RDIMM. Pet. 52 (citing Ex. 1008, 7:25–27, Fig. 4; Ex. 1011 ¶ 88). Dr. Subramanian testifies that Lee discloses an R-DIMM because the DIMM (shown in Figure 4) includes register 45. Ex. 1011 ¶ 88.

Patent Owner contends "[t]he Petition[er] offers little explanation of how Lee supposedly meets this limitation." PO Resp. 61. Patent Owner further contends "Figure 4 does not show—and Lee does not specify—

whether or what, buffering occurs on the data lines so it is impossible to tell if it discloses a RDIMM or FB-DIMM." *Id.* at 62, n.11.

Patent Owner contends "Dr. Subramanian states that 'if there is a DIMM that provides buffering for control signals and also data signals,' then 'traditionally that would be an FBDIMM.'" PO Resp. 12, n. 2 (citing Ex. 2018, 16:20–25, 19:7–11). Dr. Subramanian, additionally, testifies that Lee discloses an R-DIMM. Ex. 1011 ¶ 88 (citing e.g., Ex. 1008, 7:25–27, Fig. 4). We credit Dr. Subramanian's testimony that Lee discloses an R-DIMM because, consistent with his testimony, Lee teaches that memory subsystem 27 "may be a DIMM [dual in-line memory module] device." Ex. 1008, 7:25–28; *see also id.* at 6:6–7 ("[E]ach of the memory subsystems 27 is constructed as a [ ] dual in-line memory module (DIMM.")). Additionally, according to Patent Owner, Dr. Subramanian agrees with Patent Owner's proposed construction. Furthermore, Figure 4 of Lee illustrates *only* Register 45, PLL 41, and memory devices 39, as well as clock and command and address signal lines, as discussed above in various previous sections. Ex. 1008, Fig. 4. Consistent with Patent Owner's proposed construction of "RDIMM" i.e., "registered dual in line memory module, which buffers control signals, but not data signals" (PO Resp. 61), Lee illustrates controlling capture of command and address signals without buffering data signals (Ex. 1008, 7:34–40, Fig. 4). Accordingly, we find that Petitioner has shown sufficiently that Lee teaches "wherein the memory module comprises an RDIMM module," recited in claim 10 and RDIMM means "registered dual in line memory module, which buffers control signals, but not data signals."

Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claim 10 are obvious over Lee.

g. Conclusion—Claims 2, 5, 6, and 8–10

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2, 5, 6, and 8–10 are unpatentable under § 103(a) as obvious over Lee.

5. Discussion of claims 3 and 11

We next turn to dependent claims 3 and 11, each of which depends directly from independent claim 1. Petitioner asserts that the combination of Lee and Keith teaches all elements of claims 3 and 11 and provides a rationale for combining the teachings of Lee and Keeth. Pet. 52–54.

a. Claims 3 and 11

Claim 3 recites "wherein the incoming clock signal and the copies of the incoming clock signal are each supplied via differential clock signal lines." Claim 11 recites "wherein the memory chips comprise DDR-DRAM memories." Petitioner contends that differential signaling was well-known and points to Keeth's teachings of memory devices using differential signaling for clock signals in DDR DRAM devices. Pet. 52–54 (citing *e.g.*, Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 89–91). Relying on the testimony of Dr. Subramanian, Petitioner asserts it would have been obvious to one of ordinary skill in the art to have used differential signaling for the clocks signals and the command and address signals due to its more precise timing, higher speed capability, and greater signal/noise ratios and performance. *Id.* Again relying on the testimony of Dr. Subramanian, Petitioner also asserts

that one of ordinary skill would have used differential signaling with Lee to increase the speed of the memory, increase its bandwidth, and to comply with industry standards and practice. *Id.*

We are persuaded that Petitioner has accounted sufficiently for the limitations of claims 3 and 11. Additionally, relying on the testimony of Dr. Subramanian, Petitioner has articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Lee's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals. Pet. 52–54 (citing *e.g.*, Ex. 1016, 1:25–44; Ex. 1011 ¶¶ 89–91).

We credit Dr. Subramanian's testimony that the combination of Lee and Keeth teach all limitations recited in claims 3 and 11 and we credit his testimony providing articulated reasoning with a rational underpinning as to why one of ordinary skill in the art would have modified Lee's system so as to apply Keeth's teachings of DDR DRAM devices and using differential signaling for clock signals because his testimony is consistent with the evidence cited therein. Ex. 1011 ¶¶ 89–91 (citing e.g., Ex. 1016, 1:25–44). For instance, Keeth teaches that DDR DRAM "transfers data at both the rising and falling edge of a clock signal," which is "unlike traditional SDRAM, which transfers data only on the rising edge of a clock signal," thereby increasing the speed of the memory. Ex. 1016, 1:25–44. Keeth also teaches that such memory devices use "differential signaling for clock signals," for example, because differential signaling "reduces sensitivity to common mode voltages to enable the production of a stable internal timing reference," and provides "good signal integrity from which a balanced

receive can be built that maintains good duty cycle performance internally." *Id.*

Patent Owner does not argue for the separate patentability of claims 3 and 11 with respect to this challenge. PO Resp. 43–62. Based on the entirety of the record before us, we are persuaded by and adopt as our own, Petitioner's analysis and Dr. Subramanian's supporting testimony that all of the limitations of claims 3 and 11 are obvious over Lee and Keeth.

b. Conclusion—Claims 3 and 11

Based on the entire trial record, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 3 and 11 are unpatentable under § 103(a) as obvious over Lee and Keeth.

E. Obviousness of Claims over Dodd alone or with Keeth

Petitioner contends claims 1, 2, 5, 6, and 8–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Dodd.[9] Pet. 4, 18–39. Petitioner also contends claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Dodd and Keeth. *Id.* at 4, 39–41. In light of our unpatentability determinations based on Lee, we take no position on whether these same claims are also obvious over Dodd alone or with Keeth.

F. Patent Owner's Listing of Improper Reply Arguments and Evidence

Patent Owner filed a Listing of Improper Reply Arguments and Evidence (Paper 26) and Petitioner filed a Response (Paper 29). Patent Owner lists several portions of Petitioner's Reply and evidence allegedly

[9] Although claim 11 is listed in the section heading for this ground (Pet. 18), the analysis of claim 11 is found within only the next section (*id.* at 39–41).

beyond the scope of what can be considered appropriate for a reply. *See* Paper 26. We have considered Patent Owner's listing, but disagree that the cited portions of Petitioner's Reply and reply evidence are beyond the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response. *See Idemitsu Kosan Co., LTD. v. SFC Co. LTD*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arkane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.").

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has established by a preponderance of the evidence that claims 1, 2, 5, 6, and 8–10 of the '150 Patent are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee. Additionally, we determine that Petitioner has established by a preponderance of the evidence that claims 3 and 11 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Lee and Keeth.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–3, 5, 6, and 8–11 of the '150 Patent have been shown to be unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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